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Present status of buried contact solar cell research in Samsung advanced institute of technology (SAIT)

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SAIT에서의 전극함몰형 태양전지에 관한 최근 연구동향

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Abstract The present buried contact (BC) solar cell research at SAIT includes the development of a processing sequence suitable for the production of the single sided (SS) BC solar cells. This paper presents some results for large area (45 cm^2) SSBC cells fabricated on FZ and CZ silicon substrates. Cell efficiencies in excess of 18 % fabricated on FZ, p-type, 0.5 ohm-cm, and over 16 % on CZ p-type, 10~20 ohm-cm, wafers have been demonstrated. Both the FZ and CZ wafers were chemically textured. These results are preliminary and the exploration of double sided (DS) sequence, which is the future BC structure would lead to over 17 % and 20 % efficiency cells on CZ and FZ substrates respectively. The cost of solar cells can be reduced further if the many high temperature steps can be reduced to only one. This would be very advantageous to very poor quality substrates such as the CZ grown wafers.

요 약 이 논문은 현재 삼성종합기술원에서 연구개발이 진행중인 태양전지의 현황을 소개하고, 미래의 연구를 예측해 보기위한 리뷰성 논문이다. 전극함몰형 태양전지의 공정결과를 기판별로 특성을 조사하고, 보다 저가 공정인 전극함몰형 양면 태양전지의 공정과 비교함으로서, 그 제작 가능성을 분석하였다. 양면 태양전지는 루프 타일형에 가장 적합한 것으로 사료되며, 변환효율은 18~20 %로 예상된다.

1. Introduction

The BC technology which was developed at the University of New South Wales (UNSW) in 1985 provides the most feasible approach for transferring the improvements in the laboratory cell performance into commercial production.

This is because the processing sequence does not require photolithography, no expensive anti-reflection coatings and avoids the use of expensive metallization schemes. The first pilot production of the single sided (SS) BC silicon solar cells (Fig. 1) with energy conversion efficiencies over 18 % using thick, low resistivity and p-type substrates had been reported [1]. The evaluation of this sequence showed that, the costs per unit area for the cells are not greatly different from those of the conventional screen-printed cells [2].

The BC cell processing in SAIT started with the development of a low cost processing sequence for the production of 45-100 cm^2 SSBC cells with energy conversion efficiencies in the range 18~20 % on FZ and CZ substrates. Also, to supply such cells in large quantities at a lower cost than is presently available anywhere else to the systems section of the company for module fabrication. However, this objective has not been realized due to the very high surface recombination velocities associated with the rear of the SSBC cells. The rear metal-semiconductor alloy contributes the major component to the dark saturation current density and thus limits the fabrication of the cells to only low resistivity substrates.

The rear effect of the SSBC structure can be overcome by redesigning the rear metallization scheme to reduce the recombination effects. Thus the new structure, double sided (DS) BC cells (Fig. 2). This structure has been shown to give very good results, especially the open circuit voltages, on small area cells [3]. Thus the future of the buried contact solar cell research lies in developing a processing sequence suitable to make over 20 % efficient DSBC solar cell on both FZ and CZ substrates. Also, of great importance is the development of a processing sequence capable of reducing the cost of solar

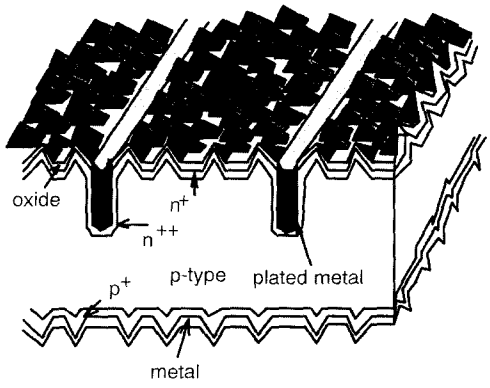

Fig. 1. Schematic of SSBC cell.

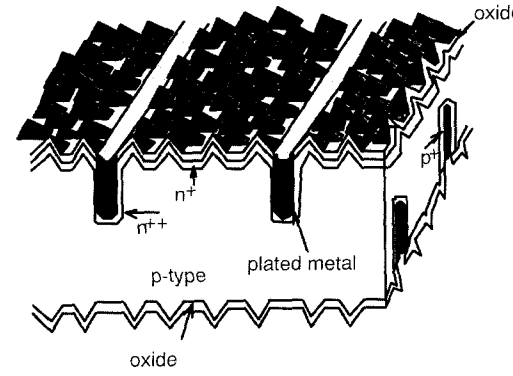

Fig. 2. Schematic of DSBC cell.

cells even more than the present sequence.

This paper reports on the present status of SSBC solar cell. Based on the present results of SSBC with the high recombination velocity, the future prediction on energy efficiency conversion of DSBC structure has been made. Also, a proposed new sequence to reduce cost on thermal budget while maintaining the high efficiency capabilities of the DSBC structure is discussed.

2. Comparison of SSBC and DSBC structures

It is of interest to compare the two structures of buried contact solar cells based on the processing sequence, performance advantage and applications.

2.1. Processing sequence

The processing sequence for the two structures is given in Table 1.

2.2. Performance advantages of DSBC over SSBC cells

The advantages of DSBC over SSBC include: Simplicity and lower cost - The elimination of the long sintering step and vacuum evaporator and the plating of lower metal surface than the SSBC cells.

Higher open circuit voltage capability - The deliberate diffusion of phosphorus to the front and rear surfaces followed by the growth of a good quality oxide results in a double passivation of both the front and rear surfaces. This reduces surface recombination to values well below the Al-sintered rear of the back surface field cells.

Higher conversion efficiency - The DSBC cells are capable of achieving a 10 % relative advantage in conversion efficiency over the SSBC, primarily because of the relatively low rear surface recombination velocity. It also offers improved energy collection in the field due to its ability to respond to light incident on the rear surface. Short circuit current densities measured from the rear illumination of DSBC cells have been only marginally lower than those measured when illuminated from front. Thus it is possible to design modules with transparent rear surfaces allowing them to collect primarily diffuse light on the module rear. Also, the effective concentration ratio obtained from stationary (non-tacking) concentrators can be significantly increased for a cell responsive to light from both surfaces.

Substrate resistivity independence - The DSBC cell does not depend on substrate resistivity for its performance making it suitable for a wider range of substrate resistivities than SSBC structure whose poor rear surface gives a bias towards lower substrate resistivities for improved performance [3].

2.3. Applications

The DSBC finds its application in static concentrators, roof tiles, space as well as general requirement for solar cell generated

electricity. Whereas, the SSBC cells can never be used with the roof tiles because it will require the bonding of two cells together which would be less efficient and more expensive.

3. Cell fabrication

The SSBC cells have been fabricated at SAIT using the processing sequence outlined in Table 1. As a check, two wafer types were processed - CZ and FZ, p - type substrates. The fabricated cells were characterized and the results are presented in Table 2.

4. Results and discussion

As noted in Table 2, the substrates are of two types, the FZ and CZ. The resistivities are 10~20 ohm - cm and 0.5 ohm - cm for CZ and FZ substrates respectively. The choice of the CZ substrates resistivity was due to cost and availability. However, the results would be discussed based on the substrate resistivity i.e. low and high resistivities.

4.1. Low resistivity FZ substrates

The spectral response of one of the cells (sc95 - 7 - 3) is presented in Fig. 3. This near 100 % internal quantum efficiency for short wavelength light in the cell indicates that

Table 1
Processing sequences of SS and DSBC cells

SSBC processing sequence	DSBC processing sequence
Wafer selection ($< 1\Omega$cm)	Wafer selection any resistivity
Surface texturing	Surface testuring
Wafer cleaning	Wafer cleaning
Top diffusion	Top diffusion
Oxidation	Oxidation
Front grooving	Rear grooving
KOH etch + cleaning	KOH etch + cleaning
Heavy phosphorus groove diffusion	Heavy boron rear groove diffusion
Aluminum rear evaporation	Rear groove masking oxide growth
Aluminum sintering	Front groove scribing
Metallization	KOH etch + cleaning
Edge isolation	Heavy phosphorus front groove diffusion
Test	Metallization
	Test

Table 2
The electrical output characteristics for 45 cm^2 SSBC cells measured under AM 1.5 g, 100 mW/cm^2 and 25℃ (These parameters are as measured by Samsung with reference cell traceable to Sandia national laboratories)

Cell ID.	V_{oc} (mV)	J_{sc} (mA/cm^2)	Filling factor (%)	Efficiency (%)	Substrate type
sc95-7-1	643	36.6	79	18.6	FZ
sc95-7-2	642	36.9	79	18.7	FZ
sc95-7-3	641	36.6	79	18.5	FZ
sc95-7-4	649	36.0	80	18.7	FZ
sc95-7-5	649	36.0	78	18.2	FZ
sc95-7-6	591	36.5	74	16.0	CZ
sc95-7-7	608	35.8	74	16.1	CZ

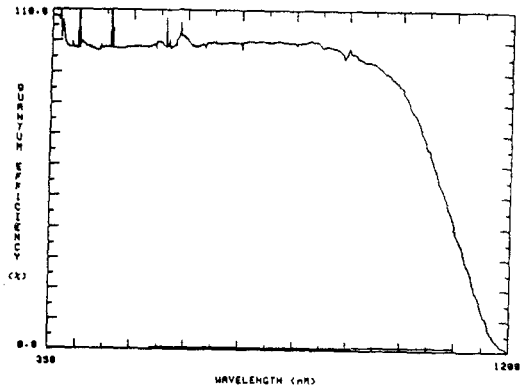

Fig. 3. Internal quantum efficiency measurement for cell sc95-7-3.

the lightly diffused emitter in conjunction with high quality oxide provide good surface passivation. It should be noted that the performance of these cells are similar to UNSW large area cells fabricated on the same substrate resistivity. The rear contribution to the dark saturation current density for cell sc95-7-3 is estimated as 0.2 pA/cm^2 by the use PC-1D simulation program [4]. The series and shunt resistances for cell sc95-7-3 were also obtained as 0.4 ohm-cm^2 and 1.4 Mega-ohm/cm^2 respectively. These values are within the range for good solar cells of similar energy conversion efficiencies [5].

4.2. High resistivity CZ substrates

The open circuit voltage (V_{oc}) of 608 mV is commensurate with the processing sequence, substrate resistivity and growth type. The CZ and the FZ cells were processed in the same batch using the high temperature (over 1000℃) processing sequence. The high temperature sequence degrades the minority carrier lifetime in case of CZ wafers while the high temperature is beneficial to the FZ substrates. However, the best open circuit voltage reported to date for SSBC cell fabricated on FZ, p-type, 10~20 ohm-cm substrate is 634 mV [6]. This means that with the development of a low tempera-

ture sequence suitable for the CZ processing, the open circuit voltages similar to those on the FZ substrates appear feasible.

In general, the fill factor for all the cells are somewhat lower than the usual value. This may be attributed to metallization step which is yet to be optimized. The plating, especially the electroless copper was very fast. This might have caused the non-filling of the grooves which would normally lead to lower fill factor.

These results would be greatly improved when most of the advantages of the DSBC cells are incorporated into processing. The PC-1D modeling of DSBC cells using the same substrate resistivities as in table 1 indicate that over 17 % and 20 % efficiencies are feasible for CZ and FZ substrates respectively. This improvement will be due to higher open circuit capabilities of DSBC cells. The DSBC cells are capable of giving very high open circuit voltages than its SSBC counterpart irrespective of substrate resistivity [3]. This is mainly due to the reduced rear surface recombination associated with the aluminum alloyed region.

5. One high temperature processing sequence

It would be of great importance to reduce the many high temperature steps from the present four to at most two. Thus, the following processing sequence which is based on spin-on processing is proposed.

1. Wafer selection
2. Surface texturing
3. Emitter/silicon oxide spin-on + baking in nitrogen ambient at 150℃
4. Rear surface silicon oxide/back surface spin-on + baking at 150℃
5. Front and rear groove scribing + KOH etch
6. Front groove phosphorus spin-on + baking
7. Rear Groove boron spin-on + baking
8. Drive-in of front and rear groove dopants at 1020℃ for 1 ~ 1.5 hours
9. Metallization
10. Edge isolation
11. Test.

The above processing sequence should be capable of giving higher energy conversion efficiencies than the present values on CZ and FZ substrates.

6. Conclusion

The preliminary results for BC solar cell research at SAIT include the demonstration of close to 19 % on FZ substrates and over 16 % on CZ wafers using the same high temperature processing sequence. The PC-1D modeling has shown that, over 17 % and 20 % efficiencies on a production line can be maintained with the DSBC cells fabricated on CZ and FZ wafers respectively. This is confirmed by the higher open circuit voltage capabilities of DSBC structure. The slightly lower fill factor for the cells may be blamed on the non-optimized metallization, especially the copper plating. Of importance is a fur-

ther reduction in the production cost of the solar cell to bring the cost of the generated electricity from this structure. Thus the proposal towards only one high temperature processing sequence.

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