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# Bonding and Etchback Silicon-on-Diamond Technology

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The fabrication process of silicon-on-diamond (SOD) structure wafer were studied. Microwave plasma chemical vapor deposition (MWPCVD) and annealing technology were used to synthesize diamond film with high resistivity and thermal conductivity. Bonding and etchback silicon-on-diamond (BESOD) were utilized to form supporting substrate and single silicon thin layer of SOD wafer. At last, a SOD structure wafer with 0.3~1 μm silicon film and 2 μm diamond film was prepared. The characteristics of radiation for a CMOS integrated circuit (IC) fabricated by SOD wafer were studied.

***Key words :*** Diamond film, SOD, Radiation hardness, Integrated circuit

## I. Introduction

Silicon on diamond (SOD) wafer is a developing technology from silicon on insulator (SOI) wafer technology in that polycrystalline diamond is used as an insulation instead of oxide such as $SiO_2$ and sapphire. Because of the excellent electrical insulation and thermal conductivity characteristics of diamond film, SOD wafer is more suitable to fabricate integrated circuits (ICs) with characteristics of radiation-hardness, high-power, high-temperature and greater packing density.[1] The key process in fabricating SOD structure is that synthesized high quality diamond film is used as buried insulator and high quality single crystal silicon layer is used as top device layer. Good interface properties between silicon and diamond is required. Specially, diamond film in SOD structure should have characteristics of high resistivity and thermal conductivity. In the other paper, we have discussed the factors influencing thermal conductivity in diamond film, thermal conductivity of diamond film synthesized in a fine condition is higher than 12 W/K·cm, which 3 times of copper's and 8 times of intrinsic silicon's.[2]

## II. SOD Wafer Processing

Before the synthesis of diamond film, a very thin (20~30 nm) adhesion layer of $SiO_2$ with high quality was deposited on prime silicon wafer by thermal oxide technology to decrease the interface states density,[3] then diamond film was grown on the thin layer of $SiO_2$. In our experiment, hot-filament chemical vapor depositon (HFCVD),[4] electron-assistance CVD (EACVD)[5] and microwave plasma CVD (MWP-CVD)[6] methods were used to synthesize polycrystalline dimond film on (100) N-type prime silicon wafer with 5Ω·cm-resistivity and 50 mm-diameter (prime wafer would formed the silicon layer of SOD wafer). After 2 μm-diamond film was deposited on prime silicon wafer. $N_2$ was put into action system to anneal the diamond film for increasing its resistivity.[7] The conditions of deposition and annealing were listed in Table 1. The resistivity of diamond films deposited by three methods as the above at the same varying condition was measured (Fig. 1). Figure 1 shows that the resistivity of diamond film was various to depending on the method of deposition. It indicated that MWPCVD method (Fig. 2) is more advantageous to acquire high resistivity of diamond film. Figure 2 shows the schematic diagram of MWPCVD apparatus. The resistivity of diamond film deposited by MWPCVD method and annealed in $N_2$ is $10^{14}$~$10^{16}$ Ω cm, and it higher $10^4$~$10^6$ times than that of deposition by EACVD method. That is because of the decreasing of pollution source in the system of MWPCVD, and diamond film could be synthesized with less impurity. Annealing technology in $N_2$ would decrease H atom in diamond film and increase the resistivity of diamond film.

BESOD technology was used to prepare SOD wafer. The process to fabricate SOD wafer is shown in Fig. 3. $SiO_2$ layer with 300 nm-thickness was contained on diamond film. A test substrate silicon wafer (the test wafer used as the substrate of SOD wafer) was also oxidized to form $SiO_2$ layer with 300 nm thickness. After cleaning, the surface of two wafers has the characteristics of absorbing water. Prime wafer was then bonded to the test wafer by hydrolyzing the oxide surfaces, mating the wafer and inserting them in a high temperature (1150°C for 4 hours) oxidizing atmosphere.

**Table 1.** The Synthesis Condition of Diamond Film with High Resistivity

| | |
|---|---|
| Substrate materials | N-Si (100) |
| Substrate temperature | 800~1000°C |
| gas pressure | 2~10 kPa |
| $H_2$ flow | 100 ml/min |
| $CH_2/H_2$ | 0~4 (V/V, %) |
| thickness of diamond film | 2 μm |
| Annealing temperature | 800~1000°C |
| A nealing time | 2 h |
| $N_2$ flow | 1 l/min |

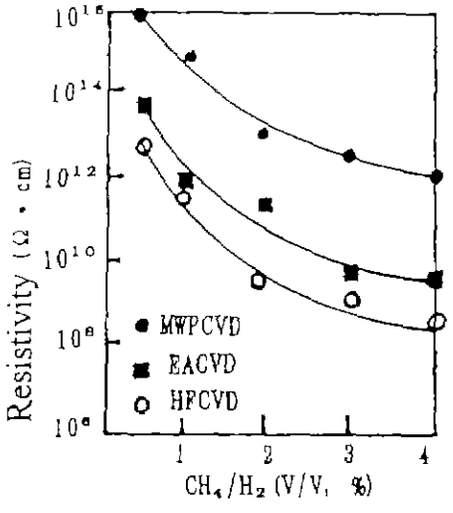


**Fig. 1.** Resistivities of diamond film deposited by various methods.

To prevent wafer defects, the cleaning and bonding processes were performed in a less than class 10 clean room to minimize unwanted particles between the bonded wafer.

After bonding two wafer, prime wafer was then thinned by conventional lapping to a final film thickness of about 30 μm, the removal rate is about 15 μm/min, but this kind of lapping method will introduce 10 μm deep subsurface damage layer. Then "mechano chemical" or "chemomechanical method" was used to polish silicon and remove the damage layer in subsurface by $SiO_2$ milky solution. At the same time, the nanometer-class $SiO_2$ was also used in lapping the surface of Si with the removal rate about 0.2 μm/min. The prime wafer was thinned to a final film thickness of about 5 μm. Non-contact ion beam sputtering polishing was used to reduce the film thickness to 0.3~1 μm, and the final SOD structure wafer was shown in Fig. 3. The noncontaction beam sputtering polishing process was optimized to remove silicon at a rate of about 20 nm/min to allow controlled thinning of the silicon film of SOD structure. We can control the remove rate and the subsurface damage layer by controlling the ion beam current, high quality of silicon thin layer can be acquire just like that of bulk silicon wafer.

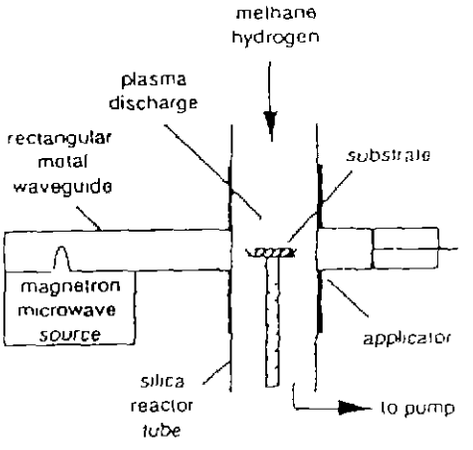


**Fig. 2.** Schematic diagram of MWPCVD apparatus.

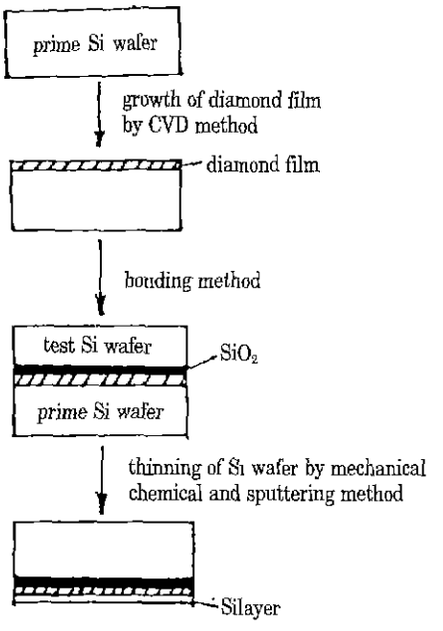


**Fig. 3.** Process sequence for BESOD.

## III. Radiation Response of CMOS/SOD Integrated Circuit

To evaluate the radiation hardness of diamond layer in SOD wafer, 54HCT03 [Quad 2-Input NAND (not and) Gate (open drain)] integrated circuit were made by SOD wafer with traditional CMOS technology, the same circuit was also made by bulk silicon wafer simultaneously.

The 54HCT03 is a logic function circuit fabricated by 3.5 μm silicon-gate CMOS technology which provides the inherent benefits of CMOS-low quiescent power and wide power supply range.

Cobalt-60 radiation were performed at a dose rate of 50

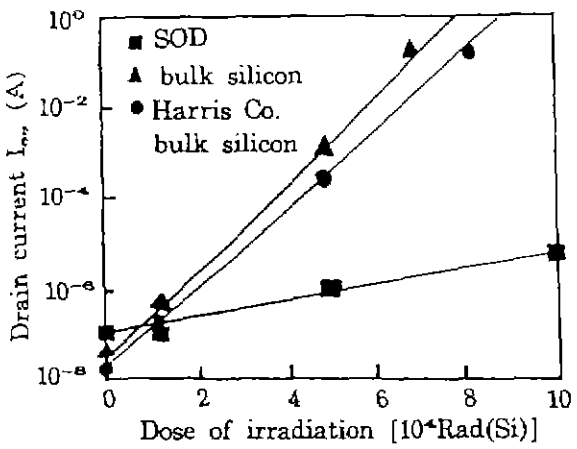


**Fig. 4.** Drain current as a function of all dose of irradiation.

rad (Si)/sec to investigate the radiation hardness characteristics of SOD circuit. At the same time, a commercial 54HCT03 circuit made by bulk silicon wafer under the same condition as SOD circuit's was also been selected for contrasting test. All radiation tests were performed on SOD and bulk Si circuit which were held at fixed bias of 5 V that enhance both gate-oxide voltage shifts and backchannel leakage current. Threshold voltage shift and drain current characteristics were measured in twenty minutes after radiation.

Figure 4 shows the change of drain current with the different of all dose of radiation. It is shown that the change of drain current for bulk silicon circuit is more than 100 times under the radiation dose in $10^4$ rad (Si) range. But for SOD circuit, change of drain current arrival within 100 times under the radiation dose of $10^6$ rad (Si). These indicated that the radiation-hardness ability of SOD circuit in drain current is clearly higher than that of bulk silicon circuit.

## IV. Conclusion

In conclusion, a SOD structure wafer was formed. During the process, MWPCVD method and annealing technology were used to synthesize diamond film with high resistivity and thermal conductivity; silicon wafer bonding technology was utilized to formed the silicon substrate of SOD structure; machine lapping, mechano chemical polishing, non-contact ion beam polishing was introduced to prepare the silicon thin layer of SOD structure. A SOD wafer with 0.3~1 μm-thickness Si layer and 2 μm-thickness diamond film was suitable to fabricated integrated circuits with high radiation-hardness ability in drain current than that of bulk wafer circuits.

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