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A study on crystallization of a-Si:H films

D.Y. Kim, D.G. Lim, H.W. Kim, K.S. Shim, S.H. Lee* and J.S. Yi.
School of Electrical and Computer Engineering, Sungkyunkwan University, Suwon 440-746, Korea
**Samsung Electronics Co. Ltd, Seoul 100-742, Korea*

수소화된 비정질 규소박막의 결정화에 관한 연구

김도영, 임동건, 김홍우, 심경석, 이수홍*, 이준신
성균관대학교 전기전자 및 컴퓨터 공학부, 수원, 440-746
*삼성전자 주식회사, 서울, 100-742

Abstract The crystallization method determines the material quality and consequent device performance. This paper investigates the crystallization of a-Si:H films on various substrate materials and analyzes the crystallization effect with and without using eutectic forming metals. From the examinations of the various substrate materials, a metal Mo was selected for the a-Si:H film growth and subsequent crystallization of it. For a sample without any eutectic metal layer, we observed grain size of 0.8 μm after 1100℃ anneal treatment. To reduce crystallization temperature, we used some of the eutectic forming metals such as Au, Al, and Ag. Poly-Si films with grain size over 10 μm and (111) preferential plains were achieved using a premetal layer of Au at an anneal temperature of 700℃. The various crystallization effects of eutectic metal thickness and type were investigated for photovoltaic (PV) device applications.

요 약 수소화된 비정질규소 박막의 결정화 방법은 물질의 질과 후속으로 제작되는 성능을 결정한다. 본 논문은 다양한 기판위에 성장된 비정질규소 박막의 결정화 특성조사와 고용체 형성 금속 박막의 유·무에 따른 결정화 효과를 분석하였다. 다양한 기판조사로부터 Mo 기판이 비정질규소 박막을 성장하기위해 선택되었다. 고용체 형성 금속을 사용하지않은 경우 1100℃ 열처리후에 결정립의 크기가 0.8 μm에 달하는 다결정을 얻었다. 결정화 온도를 줄이기위해 고용체

형성 금속인 Au, Al, Ag등을 사용하였다. 금속 Au를 사용하여 700℃ 열처리 후에 결정입경 크기가 10 μm 이상이며 (111) 면 우선배향 특성을 갖는 다결정규소 박막이 달성되었다. 광전소자 응용을 위하여 규소박막과 고용체를 형성하는 금속 종류, 금속 두께 등의 결정화 영향을 조사하였다.

1. Introduction

A-Si:H solar cell shows high optical absorption which permits true thin-film ($<$ 1 μm) design and exhibits promising conversion efficiencies well in excess of 12 %. However, a-Si:H cells have exhibited problems on stability of conversion efficiency. Electrical properties and stability of the a-Si:H are dominated by hydrogen movement in the film. Hydrogen movement and the Si film structures are affected by heat treatment. This paper covers some of the efforts to overcome the problems of a-Si:H cell by converting a-Si:H to poly-Si film. Selection of substrate material for a Si film growth requires some considerations. Because a deposition of thin film Si requires high temperature treatment, the substrate material for the thin film Si deposition should meet the following considerations: 1) the thin film Si should well adhere to the substrate, 2) thermal expansion coefficient (TEC) must be close to that of Si to prevent any bending, cracking, or peeling of the Si film, 3) the substrate material must not provide an active impurity in the Si film, 4) the substrate has to be inexpensive, 5) electrical resistivity should be as low as possible for the PV cell applications. Various types of substrates were investigated using metals (Mo, Al, Kovar, stainless steel), oxidized wafer, graphite, ceramic, and glass substrates. Silicon on these substrates was deposited as a thin film a-Si:H. Anneal treatments were performed after Si film growth to give a certain range of crystal arrangement. Methods to achieve grain size enhancement by anneal treatment can be very beneficial to the wider use of poly-Si for active solid state devices. Annealing of the Si film permits an increased atom mobility to be maintained for a much longer time than would be possible during Si film deposition. Reported anneal instruments are furnace, rapid thermal anneal, e-beam, laser, and graphite strip heater scanning anneal [1-5]. During annealing of thin film Si, the presence of certain metals strongly increases the atomic mobility which decreases the time and temperature required for grain growth. Some of the metals investigated for a eutectic phase assisted crystallization are Au, Ag, Al, In, Ga, Zn, and Sn [6-12]. Using a conventional furnace anneal, this paper studies the crystallization effects of eutectic forming metals that contains more than 10 % at Si.

2. Experiment

As a first step, this paper examined various substrate materials for a crystallization of thin film Si. After the examination of substrate materials, then we studied the crystallization effect with and without premetal eutectic forming metals. Figure 1 shows the experimental procedures used in this paper. The a-Si:H films were deposited on substrates by glow discharge decomposition of silane gas. Deposition temperature varied from 225 to 380 ℃ giving a deposition rate of around 0.5 μm/min. These samples were then subjected to different anneal conditions. For an investigation of low temperature crystallization, a thin metal layer of Al, Au, and Ag was placed on top of substrate having a structure of a-Si:H/Metal/Sub. The crystallization of thin film Si was investigated using the a-Si:H layer thickness from 0.5 to 20 μm and premetal layer from 5 to 600 nm. The a-Si:H samples were first cleaned with organic solvent. The sample cleaning process carried out by using four steps; 1) ultrasonically clean in acetone for 3 minutes, 2) ultrasonically clean in methanol for 3 minutes, 3) D.I. water rinse for 5 times, 4) nitrogen gas blow dry. A crystallization was done by Lindberg quartz tube furnace annealing. Nitrogen gas flowing at 2 (lpm) created a nitrogen dominating environment which prevented oxidation during the anneal process. The samples were loaded after the furnace was stabilized at the desired anneal temperature. Anneal temperature ranged from 100℃ to 1200℃

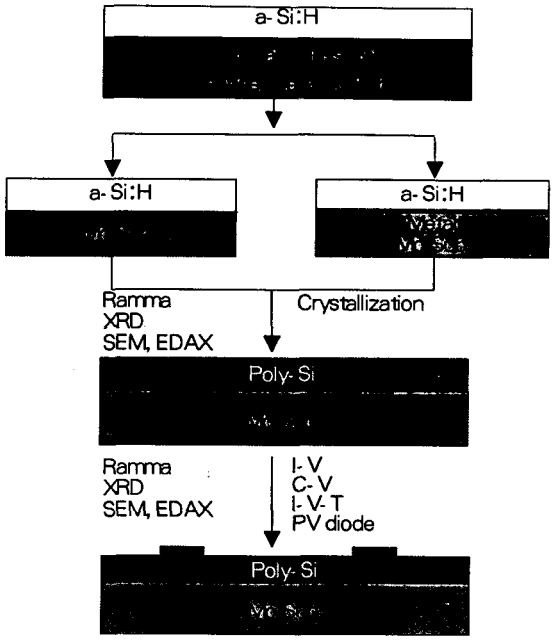

Fig. 1. The employed experimental procedures of the research work.

with 4 h duration. The furnace was cooled at a rate of 2.2℃/min. When the furnace temperature reached 200℃, the crystallized samples were unloaded for the next procedure. The degree of crystallization was studied with XRD SEM, and Raman scattering spectrscopy. Chemical bonding structure was examined with FTIR, AES, and EDAX. Electrical properties were measured using Keithley 617, 230, 595, and computer data acquisition system.

3. Result

We present the experimental results with three main stream lines. The first section covers an investigation of substrate materi-

al. The metal Al substrate shows too low melting point for the crystallization of thin film Si. Although Al is not good substrate choices, a thin layer of Al can serve as a premetal layer for low temperature poly-Si growth [13,14]. A depth profile using auger electron spectroscopy of a thin film Si on stainless steel (S.S.) showed high iron (Fe) diffusion to the Si film above 700℃ anneal [15]. Figure 2 shows the EDAX results on the S.S. substrate. Only the Si peak appears on as-grown intrinsic a-Si:H on the S.S. substrate. Peaks for Fe, Cr, and Ni started to appear after 600℃, 4 h furnace annealing and indicate that these elements diffused into the Si film. Glass or quartz exhibited cracks of Si film after 850 ℃. A graphite substrate requires extra material to make self supporting substrates and porosity is relatively high. Alumina ceramic substrates can stand high temperature, but the high resistivity of the material contradicts condition for the PV applications. The Mo sheet metal is chosen as the substrate material for further crystallization study because it somewhat satisfies the substrate considerations. Molybdenum substrates exhibited good surface morphology after heat treatment while other metal substrates such as S.S. and Kovar showed strong interdiffusion and stress induced defects such as pittings, holes, and large voids. Film quality degraded such that electrical characterization was almost impossible after high temperature anneal. SEM studies for the poly-Si/Mo sample indicate no definite morphology change after heat treatment.

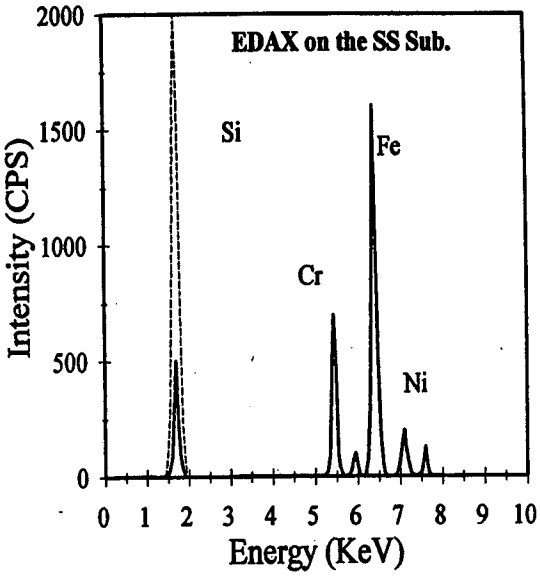

Fig. 2. EDAX results on a-Si:H/S.S. Sub. before and after 600℃ anneal.

With the determination of substrate material as Mo metal plate, we moved our research topic on a crystallization of a-Si:H without any premetal layer. For a sample without any premetal layer (a-Si:H/Mo), Ar laser driven Raman spectroscopy was employed to examine crystallinity of the thin film Si. For an as-grown a-Si:H/Mo, we observed a Raman peak at 480 cm^{-1} and this peak appeared at 520 cm^{-1} after anneal treatment above 600℃. From the Raman spectroscopy study, we learned that the a-Si:H film crystallization was initiated at 600℃. The XRD patterns showed a (111) preferential orientation by increasing anneal temperature. As anneal temperature was increased, the peak intensity was increased and the FWHM was reduced. This result indicates that crystallization is improved

with an increase of anneal temperature above 600℃. Electron microscopy study revealed, however, only fine grains from 20 nm to 800 nm as anneal temperature changed from 600℃ to 1100℃. There was no columnar structure for all the crystallized samples without any premetal layer. For an electrical characterization, resistivity was measured as a function of temperature using the van der Pauw method. Resistivity was reduced from 10^8 Ω-cm for as-grown intrinsic a-Si:H/Mo to 10^4 Ω-cm after 850℃, 4 h anneal treatment. Calculated activation energy in Table 1 shows lower values in n-type than intrinsic sample because of the reduced energy gap from the donor level band-edge effects near the conduction band. By neglecting the grain boundary effect on resistivity, activation energy of the intrinsic poly-Si approximately equals half of the energy gap ($E_g/2$). For an intrinsic sample, therefore, E_a is predicted to be 0.56 eV which is in good agreement with the experimental values of 0.51 eV. The field effect mobility determined from the transconductance method is shown in Fig. 3. Mobility stays in the order of 10^{-3} $cm^2/V.s$ for the

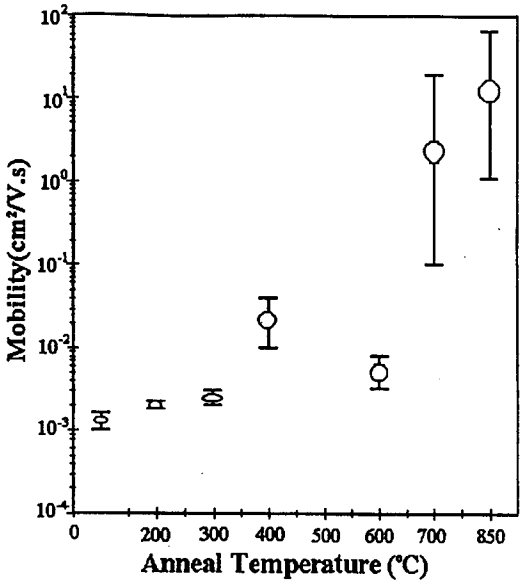

Fig. 3. The field effect mobility on a-Si:H/Mo as a function of anneal temperature.

anneal temperature below 600℃. An anneal temperature higher than 700℃ gave 3 orders improved field effect mobility. After the high temperature anneal above 700℃ and grain boundary passivation, some of the sample exhibited very high field effect mobility to 20~67 $cm^2/V.s$. Although, mobility improvement was observed as increasing anneal temperature, a-Si:H/Mo type requires high temperature treatment to form

Table 1
Activation Energy of Thin Film Si

Sample structure	Si film thickness(μm)	Heat treatment(℃)	Activation energy(E_a[eV])
i/n^+/Mo	5	as-grown	0.900
		850	0.506
		1000	0.515
n/n^+/Mo	5	as-grown	0.200
		850	0.045
		1000	0.044

a poly-Si film and exhibits a fine grain size even for an elevated anneal temperature of 1100℃. To reduce the crystallization temperature, we used some of the eutectic forming metals in between a-Si:H and Mo substrate.

The last portion of this paper investigates the crystallization effect by using eutectic forming metals for a crystallization of thin film Si. The sample structure takes a-Si:H/Metal/Mo with metal layer being Al, Ag, Au, and Al-Si alloy. These metals exhibit a eutectic point at a reduced anneal temperature [16]. For instance a metal Au can form a eutectic layer at the low temperature of 370℃. The eutectic layer can serve as seeding layers for the crystallization of a-Si:H films. The eutectic points are increased to 577℃ for Al and 830℃ for Ag. By using the premetal layer of Au and 700℃, 4 h anneal, we observed poly-Si films with grain size over 10 μm as shown in Fig. 4. The grain size was reduced to 2 μm for Al and Al-Si alloy system. Anneal treatment on a-Si:H/Ag /Mo Sub. at 850℃, 4 h showed good crystallinity with grain size of 5 μm. It is clear that we can achieve enlargement of grains at a reduced anneal temperature by employing eutectic forming metals. Further investigations are focused on Au and Al premetals because of their capability to initiate crystallization at the reduced anneal temperature in comparison to Ag.

Large grain size of poly-Si film is one of the goals to be achieved, however, there are other important considerations such as crystal quality and low impurity concentration. Figure 5 shows the XRD result on poly-Si/Au/Mo samples. XRD results showed that (111) peak increase as the thickness of Au layer

Fig. 4. SEM surface morphology on poly-Si films after 700℃, 4 h anneal for a-Si:H/Au /Mo (Mag. x2,000).

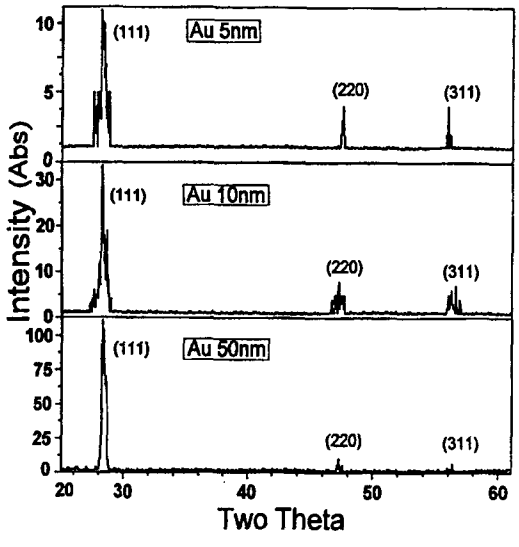

Fig. 5. XRD result that shows the effect of Au layer thickness (Top:5 nm, middle:10 nm, bottom:50 nm).

increased from 5 nm to 50 nm for a fixed anneal temperature of 700℃. If premetal layer is too thin, then there is no way to have continuous Au layer because the Mo substrate roughness is higher than 10 nm. In this case some portions of the Si film are not exposed to Au layer and contributed to have the lowest XRD peak intensity. This result agrees with SEM surface morphology study which revealed the small grains for 5 nm thick Au layer sample. With an intentional control of Au dots of 150 μm × 150 μm squares, we observed that the improved crystallization along the vertical direction. The result shows that a vertical crystallization is faster than the lateral propagation. Crystallinity improvement with Au 50 nm thick layer can be explained by the formation of continuous Au layer. As Au layer thickness increased over 50 nm, however, we observed other side effect of nonuniform grain structures. For the thicker Au metals above 500 nm we observed that the poly-Si film grains were not uniform having two distinctive regions of large and fine grains. Figure 6 shows the typical structure of thick Au premetal layer effect. Two different regions may have created by different amount of gold. During the anneal treatment, Au-rich regions can be formed and different Au concentration in thin film Si may have resulted in different gain size. Since the uniform crystalline structures are preferred for an electronic device application, the Au thickness must not exceeded 50 nm. The premetal layer thickness not only influences the grain size but decides the impurity concentration in thin film Si. To reduce Au impurity in Si film, ultra-thin metal from liquid source was spin coated

Fig. 6. SEM photograph of poly-Si films with two distinctive grain structures (Mag. x2,000).

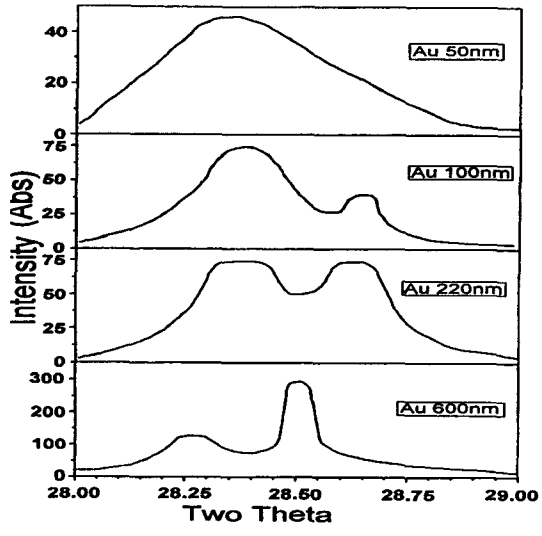

Fig. 7. XRD result on (111) peak position shows the Si lattice constant is reduced as increased Au layer thickness.

and crystallized with average grain size of 0.5 μm [17].

XRD examination for an Al-Si alloy system showed no peak shift because of the lattice shrinkage from high concentration of Al impurities ($>10^{19}$ cm^{-3}). This result suggests that Al assisted crystallization does not change the Si lattice spacing because of the close atomic weight. However, XRD peak for the Si film deposited on Au premetal layer sample was shifted which indicates gold impurities (10^{12} cm^{-3}) are not only act as deep level impurities also changes the silicon lattice spacing. Figure 7 shows the (111) peak position of XRD study for the various thicknesses of Au layer. As the thickness of Au layer increases, a major peak shifted to 28.5° due to lattice shrinkage from Au impurities in Si. As far as surface uniformity is concerned, Al premetal layer samples were much better than Au premetal layer. Also, Al premetal layer showed excellent result for stress induced pitting problems. The XRD result on Al-Si premetal layer type showed about a half peak intensity of Al premetal layer sample. A sample structure of a-Si:H/Al/Mo is suggested to reduce stress induced defect problem and reduce crystallization anneal temperature less than 600℃. Further studies can be directed to a binary systems such as Al-Ga and Al-In because these metals allow a reduced impurity concentrations while maintaining a low temperature crystallization.

4. Conclusions

This paper investigated crystallization of a-Si:H with and without using eutectic forming metals. The Mo substrate satisfied some of the substrate requirements for the PV application. The a-Si:H/M type exhibited crystallization above 600℃, however, grain size was not large enough to be used in the PV application. The premetal layers of Au and Al were studied to reduce crystallization temperature. We obtained large grains over 10 μm size with Au premetal layer. Premetal layer thickness was one of the most important factors for the grain size and impurity concentration of poly-Si. Although, crystallization temperature was lowered by using Au layer, electrical properties are not ensured since Au creates deep level defects in Si film. Future work has to be directed to achieve poly-Si films using Au metal as thin as possible While Au was suffered from impurity concentration, Ag shows difficulties in reducing crystallization temperature due to its higher eutectic point of 830℃. We recommend Al and its binary alloys like Al-Ga and Al-In because these metals can act as shallow acceptors in silicon and impurity concentrations can be reduced.

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