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Poly-Si Cell with Preferential Grain Boundary Etching and ITO Electrode

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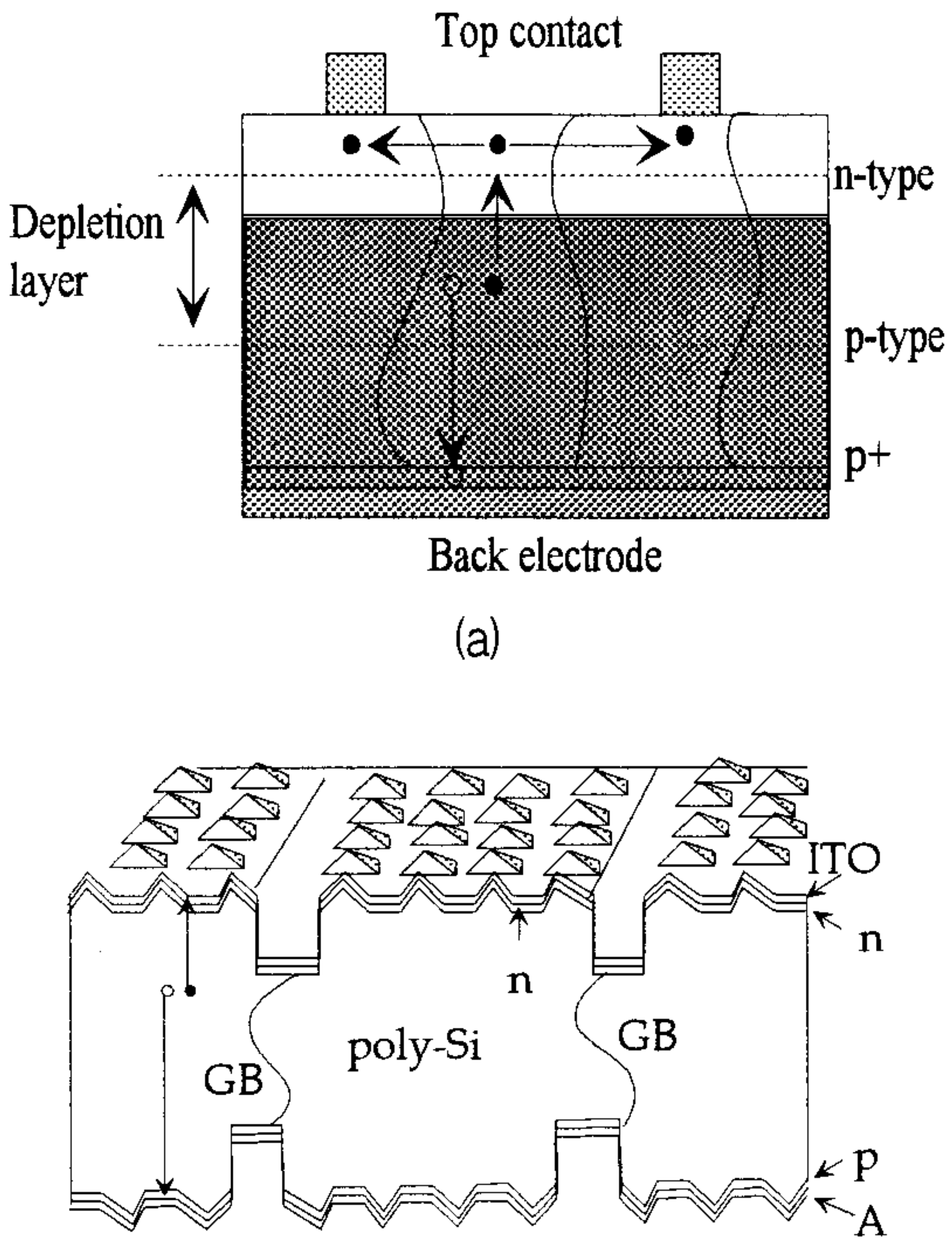
ABSTRACT

This paper deals with a novel structure of poly-Si solar cell. A grain boundary (GB) of poly-Si acts as potential barrier and recombination center for photo-generated carriers. To reduce unwanted side effects at the GB of poly-Si, we employed physical GB removal of poly-Si using chemical solutions. Various chemical etchants such as Sirtl, Yang, Secco, and Schimmel were investigated for the preferential GB etching. Etch depth about 10 ㎛ was achieved by a Schimmel etchant. After a chemical etching of poly-Si, we used $POCl_3$ for emitter junction formation. This paper used an easy method of top electrode formation using a RF sputter grown ITO film. ITO films with thickness of 300 nm showed resistivity of 1.26×10^{-4} Ω-cm and overall transmittance above 80 %. Using a preferential GB etching and ITO top electrode, we developed a new fabrication procedure of poly-Si solar cells. Employing optimized process conditions, we were able to achieve conversion efficiency as high as 16.6 % at an input power of 20 mW/cm^2. This paper investigates the effects of process parameters: etching conditions, ITO deposition factors, and emitter doping densities in a poly-Si cell fabrication procedure.

1. Introduction

The high cost and limited cell size of the single crystalline silicon solar cells have been the major obstacle for their terrestrial applications[1]. For these matters, poly-Si solar cell has been considered as an alternative solution[2),3)]. However, defects and potential barriers at the GB of poly-Si reduced a short circuit current (I_{sc}) and conversion efficiency of solar cells[4]. To reduce these undesired effects, we developed physical removal of GB and adopted an ITO film5)~7) as a top electrode.

Conventional and our new cell structures are given Fig. 1. In carrier collection processes, a GB potential barrier hinders photo-generated carriers in the conventional poly-Si cells. Removing GB region and placing an ITO electrode directly on top of GB, we expect that most of the photo-generated carriers can be collected without experiencing the GB potential barrier. By using an illustrated cell structure in Fig. 1(b), we were able to fabricate poly-Si solar cells with reduced GB effects.



(a)

(b)

Fig. 1. Structural comparison between (a) typical poly-Si cell and (b) preferential GB etching plus transparent ITO electrode.

2. Experimental

We took an experimental procedure in the order of organic cleaning, preferential GB etching, POCl$_3$ doping, Al back-side metallization, ITO top electrode formation, and solar cell characterization. Fig. 2 shows experimental procedures employed in the research work. We used poly-Si substrates with a wafer size of 10 cm×10 cm, thickness 350 μm, resistivity 1~5 Ω-cm, and minority carrier lifetime 5 μs. Grain sizes were ranged from 5 mm to 50 mm giving an average size of 16.9 mm. After chemical etching of poly-Si by various etchants such as Sirtl, Yang, Secco8),

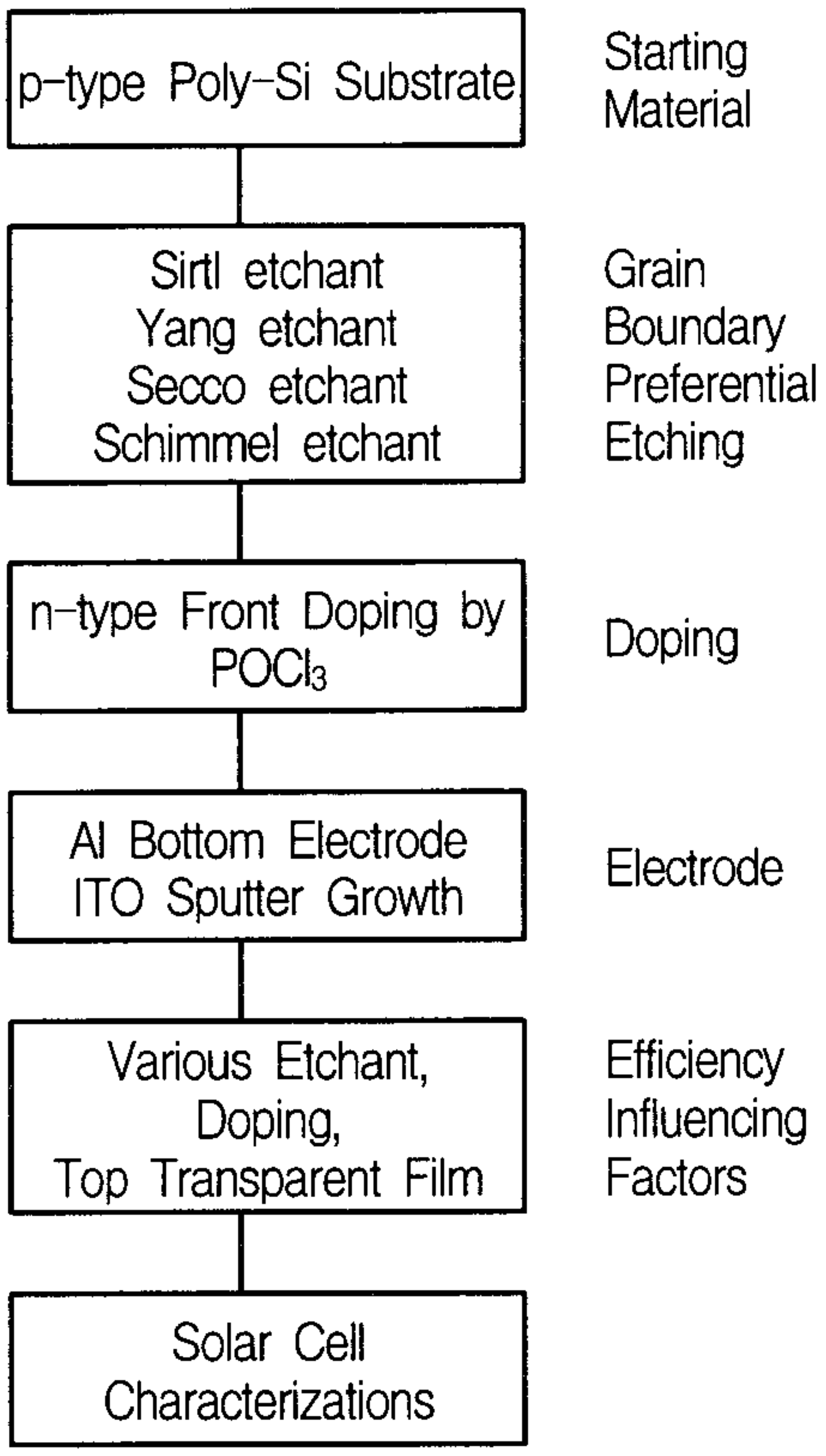


Fig. 2. Experimental procedures employed in this research work.

and Schimmel[9], we used phosphorous doping for a junction formation. N-type emitter junction was achieved by $POCl_3$ diffusion at a temperature of 900 ℃ for 30 min. A diamond saw-cutter (Buehler ISO-9001) was employed to isolate p-n junction. Resistivity was measured by a 4-point probe system of Signatone S-30L. Current-voltage (I-V) characteristics of solar cells were investigated under dark and light illumination. Spectral response was examined using a Jobin Yvon XC-150, MAP23 scanning controller, and Keithley 617.

3. Result and Discussion

Among various etchants such as Sirtl, Yang, Secco, and Schimmel, a Schimmel etchant showed an excellent preferential etching properties along grain boundaries as well as texturing effects on grain surface. Table 1 shows etching properties of the investigated etchant. As far as grain boundary etch depth is concerned, a Secco etchant exhibited better than any other chemical formulas. However, the surface texturing effect was not as good as the Schimmel etchant. Fig. 3 shows a confocal microscope image of poly-Si substrate etched by the Schimmel etchant for 10 minutes. We can clearly see a deep trench of 10 ㎛ along grain boundaries and textured grain surface about 2 ㎛. From various etching investigations, we recommend the Schimmel etchant for solar cell applications.

To make an easy electrode formation, we adopted ITO film as a top electrode. Various RF sputtering parameters such as a substrate

Table 1. The Poly-Si Etching Properties in the Various Etchants.

Etchant	Textured Surface (㎛)	GB etch depth (㎛)	Overall comment
Sirtl	1.3	3.7	poor
Yang	1.5	4.0	fair
Secco	2.0	10.7	good
Schimmel	2.3	9.8	excellent

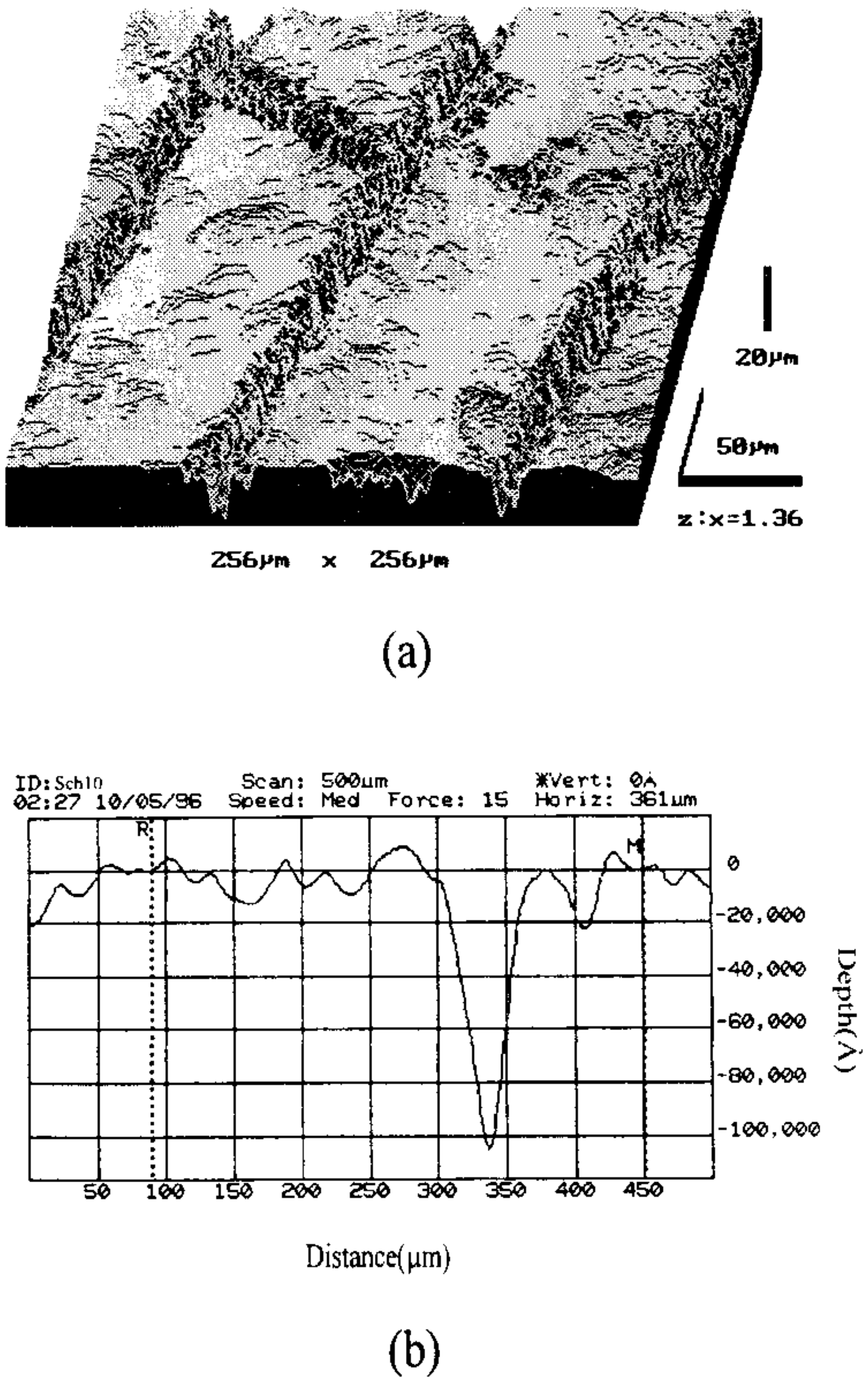


Fig. 3. A surface structure of poly-si substrate etched by the Schimmel etchant for 10 min. (a) confocal microscope image, (b) α-step profile.

temperature, gas pressure, annealing temperature, and other deposition condition were examined to achieve a higher transmittance and conductivity. From XRD examination on ITO films, we observed a preferred (222) orientation. As a substrate temperature increased, XRD result exhibited the more dominated (222) peak. The highest (222) peak intensity was observed at a substrate temperature of 500 ℃. However, keeping a p-n junction poly-Si at 500 ℃ for a long time, we observed a junction shorting problem due to indium migration. With the optimum growth conditions, ITO films showed resistivity of 1.14×10^{-4} Ω-cm and transmittance of 81.2% for the wavelengths between 300 nm and 900 nm.

Table 2 illustrates transmittances at a fixed wavelength of 620 nm and displays resistivities of ITO films. Fig. 4 shows the transmittance characteristics of ITO films grown at various substrate temperatures. A calculated optical band gap[10] of ITO film ranged from 3.65 eV to 3.95 eV. For high conductivity and transmittance, we recommend readers to take a substrate temperature of 400 ℃.

Fig. 5 shows the characteristic parameters

Table 2. Variation of ITO Film Transmittance and Resistivity for Different Substrate Temperatures.

Substrate temp. (℃)	T (%) @620nm	ρ $\times10^{-4}$(Ω-cm)
RT	81.1	32.83
100	75.4	9.16
200	76.8	2.19
300	86.1	2.67
400	83.1	1.14
500	82.3	1.26

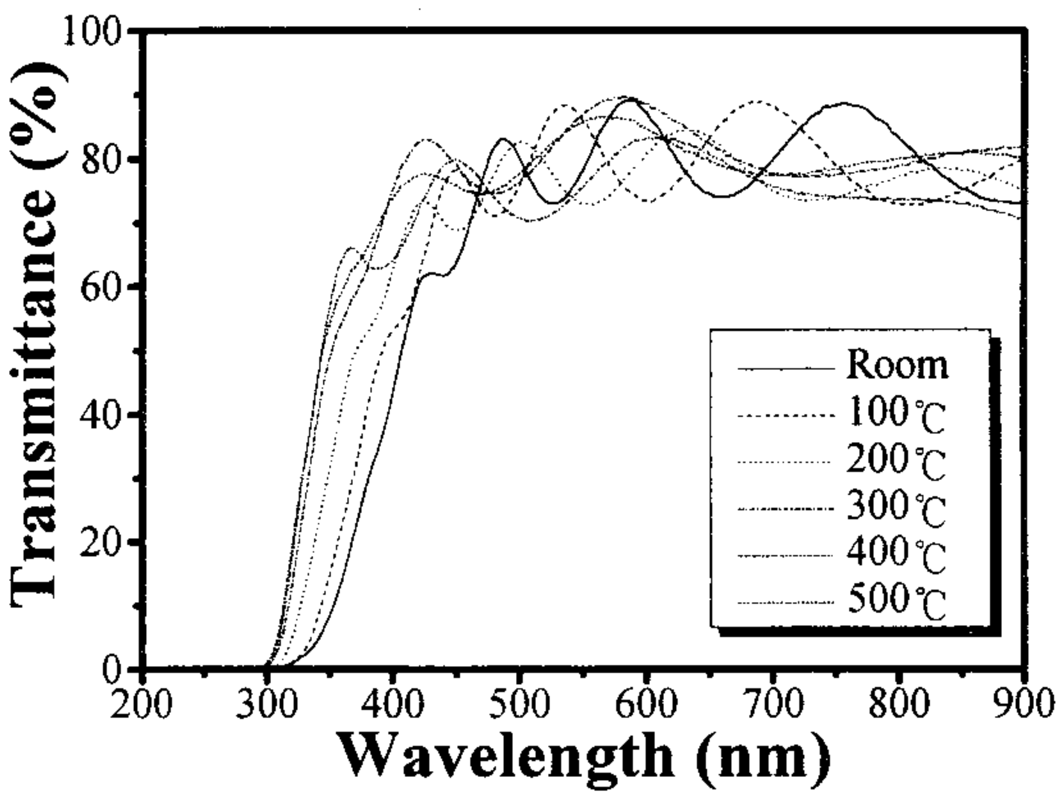


Fig. 4. Optical transmittance spectra of ITO films with various substrate temperatures.

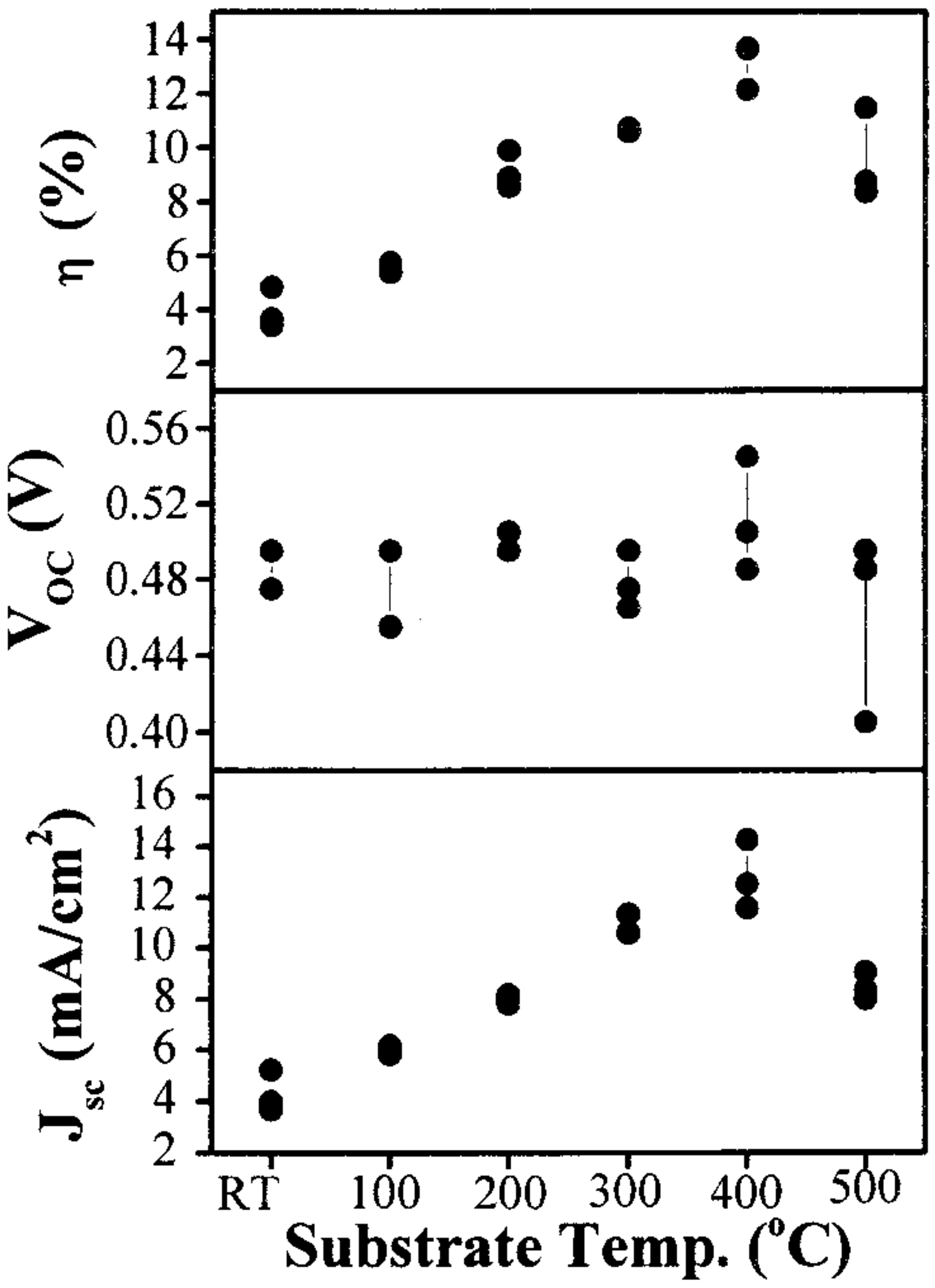


Fig. 5. The solar cell characteristics for various ITO growth temperatures.

of the poly-Si solar cells for various ITO deposition temperatures. J_{sc} exhibited strong dependence on an ITO film growth temperature while V_{oc} demonstrated little changes. Reflectance (R) study as a function of ITO thickness showed fluctuations from R=4.6 % for a 68 nm thick ITO film to R=27 % for a 175 nm film. For other ITO thickness, reflectance was ranged between the maximum of R=27 % and minimum R=3 %. Reflectance variations as well as resistivities and transmittances of the ITO films contribute very large modifications in the cell efficiency. We suggest that the highest efficiency at 400 ℃ are resulted from the reduced resistivity and appropriate AR coating effect of ITO[11]. Reduced efficiency at 500 ℃ can be interpreted by indium migration to n-type emitter layer. Because V_{oc} is limited by internal built-in potential, little fluctuations in V_{oc} was monitored with substrate temperature variation.

Having optimized conditions in ITO film growth, we directed our efforts to find the best conditions of a GB removal process for poly-Si solar cells.

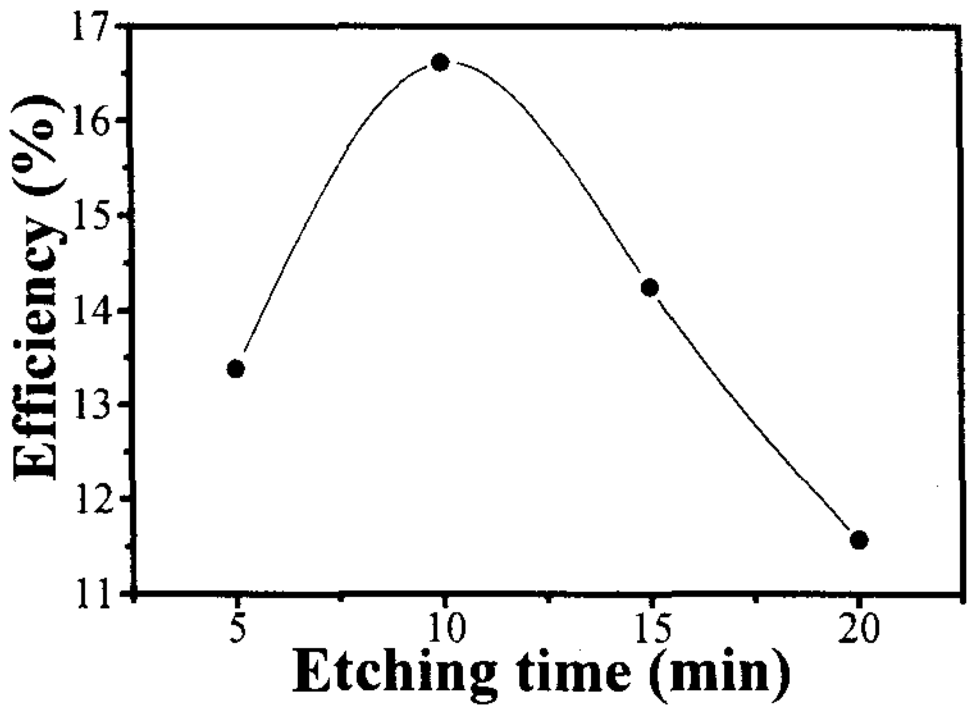


Fig. 6. Solar cell efficiency as a function of etching time in the Schimmel etchant.

Fig. 6 shows that conversion efficiency is strongly related to the GB etching time of a Schimmel etchant. We focused on the Schimmel solution because GB removal property exhibited the best results. Cells fabricated with 10 minutes of etch duration showed the highest cell efficiency of 16.6 %. If poly-Si is subjected to either shorter or longer than 10 minutes of the Schimmel etching, then cell efficiency decreases due to under or over etched nature.

Light I-V characteristic with voltage variation from -0.3 V to 0.5 V is illustrated in Fig. 7 for a cell fabricated with the Schimmel etching for 10 min. At a low input power of 20 mW/cm^2, we achieved an improved J_{sc} of 17.46 mA/cm^2. Efficiency changes are mostly resulted from J_{sc} variations with different etching conditions. Considering input power density, we regard J_{sc} is relatively high. However, V_{oc} and fill

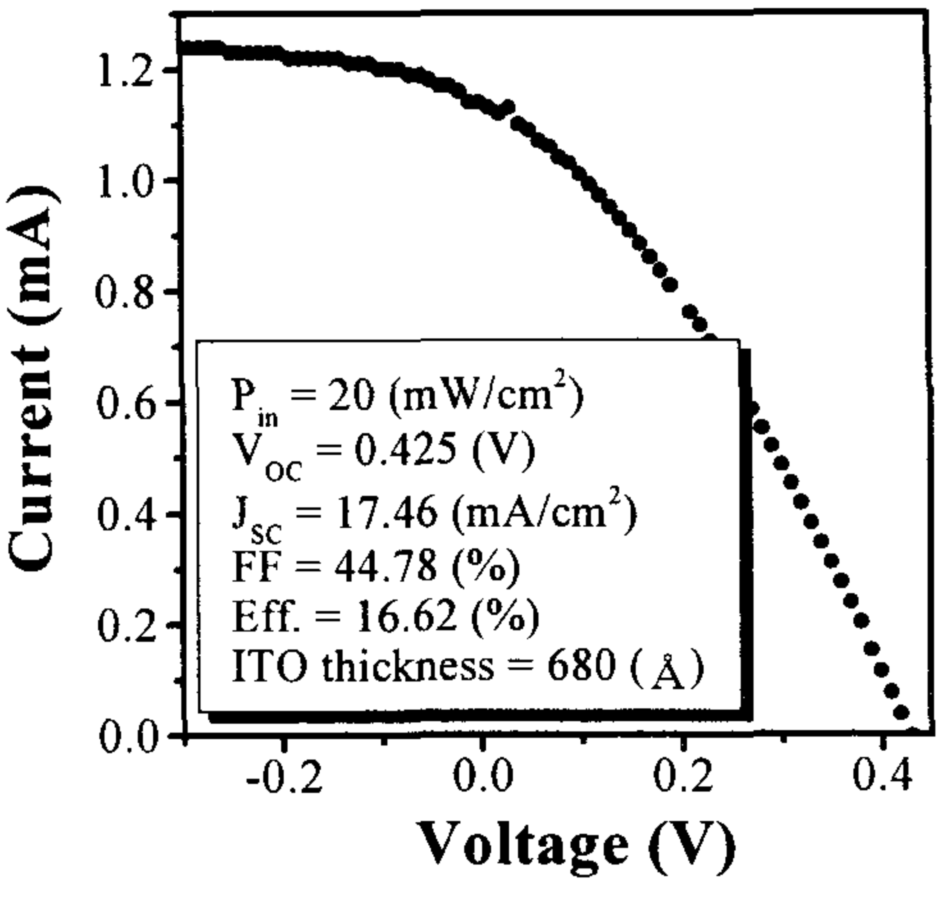


Fig. 7. Light I-V result for a solar cell fabricated after a ten-minute of the Schimmel etch.

factor exhibited rather low values as 0.43 V and 44.78 %, respectively. These results may have influenced by a low doping density of emitter layer. With the modulation of light intensity from 20 mW/cm^2 to 80 mW/cm^2, we observed I-V curves and calculated series resistance from the divided differentials of photocurrent and voltage. Investigated cells suffered from high series resistance over 10 Ω which may be responsible for the low FF and V_{oc}. We think that higher cell efficiency can be achieved by optimizing emitter layer doping density and reducing poly-Si base thickness.

4. Conclusion

To reduce the grain boundary effect, this paper investigated various parameters such as the preferential etch solution, etch time, ITO electrode, heat treatment, and emitter layer effect. A Schimmel etchant demonstrated excellent GB etching characteristics. By employing ITO top electrode, we showed an easy and effective method in photo-generated carrier collection without passing through the GB. ITO film served not only as a top electrode but also as an effective AR coating layer. We recommend ITO film deposition at the substrate temperature of 400 ℃. Using the optimized conditions, we were able to achieve conversion efficiency as high as 16.6 % at an input power of 20 mW/cm^2. Further studies will be directed to reduce the thickness of poly-Si substrate, and to optimize the emitter doping concentration.

Acknowledgement

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