신호 전이 밀도 전파 동작에 기초한 향상된 전력 평가 방법의 연구

김 동 호† · 우 종 정††

요 약

전력 평가를 위한 전이 밀도 전파에 대한 개선된 방법을 제안한다. 제로 지연 모델을 위한 전력 평가는 전력 소모의 하한 경계 값에 대한 적절한 기준이다. 전력 예측을 위한 하한 값으로 제로 지연 모델을 사용한 전이 전파 방법에 대한 연구가 있지만 전이 밀도 전파 과정 중 잉여 요소들을 제거하지 못하였다. 본 연구에서는 전이 전파 밀도 동작을 분석함에 의하여 잉여 요소들을 제거할 수 있는 향상된 신호 전이 밀도 예측 기법을 제안한다. 실험에 의하면 제안된 방법이 기존의 방법에 비하여 상대적으로 양호한 예측 정확도를 나타낸다.

Improved Power Estimation Methodology Based on Signal Transition Density Propagation Behavior

Dongho Kim† · Jongjung Woo††

ABSTRACT

An improved transition density propagation method for power estimation is proposed. The power estimation for the zero delay model is a proper criteria for the lower boundary for power consumption. A transition propagation method, including the zero delay model as a lower boundary for power estimation was studied. However, there were some redundancy factors in the process of transition density propagation. Hence this paper will explore the transition density propagation behavior to eliminate the redundancy factors and present the improved estimation methodology for the signal transition density. The experiments show that the proposed method has comparably better estimation accuracy than the conventional methods.

1. Introduction

While the demand for mobile computing and complexity for devices is dramatically increasing, the importance of low power design has made power estimation technology as an emerging issue. Indeed, power estimation technology can diagnose and keep several reliability problems from degrading the digital circuit performance. In CMOS circuits, one of the basic reasons for power consumption is the signal transition by charging and discharging of a load capacitance at each gate node. The exact transition estimation of digital circuits is very difficult because the input behavior that is a crucial factor for transition is not known at the design stage. Several probabilistic approaches have been presented [1-4]. Among them, the method of transition density propagation [1] has emerged as a useful power estimation method. It is known that this method

* This Paper was supported by a Grant from Sungshin Women's University in 2000.
† 정 회 원 : Univ. of Texas at Austin 대학원 전기 컴퓨터 공학과
†† 종신회원 : 성신여자대학교 교수
논문접수 : 2000년 5월 10일, 심사완료 : 2000년 7월 26일

is very fast and efficient. However even if this method can apply to the zero delay model as a lower boundary for power consumption, it is said that this method has failed to consider the effect that is a general phenomena, i.e. simultaneous signal transition, in the zero delay model. To overcome this problem, the modified transition propagation method was explored [4]. But this work did not overcome this problem and could not give a good estimation for power consumption. Our observation said that the conventional transition density propagation has some redundancy factors in the process of propagating the transition density. Hence we will present an effective transition density propagation method for the zero delay model by eliminating the redundancy factors that are the simultaneous signal effect and the signal correlation.

The paper is organized as follows. In section 2, we will explore the basic concept of the probabilistic approach for power estimation. In section 3, the redundancy effect that occurs in the transition density propagation method will be explained and a new approach for the signal transition density propagation will be presented. In section 4, the simulation process and its results will be discussed. Finally the conclusions and future work will be discussed.

2. Background

CMOS digital logic can be considered in two main parts : N-channel networks and P-channel networks. In these types of circuits, power is dissipated during the signal transition time. Since the status of n-channel and p-channel is complimentary to the input signals, electrical short from V_{DD} to GND which is the main reason of power consumption occurs only when the switching activity exists at the gate output node. When the input voltage switches from high(V_{DD}) to low (GND), the n-channel transistors are turned off and the p-channel transistors start conducting. During this period, the output load capacitance is charged by the current that is flowing from V_{DD} to GND via the p-channel. When the input voltage switches from low to high, the n-channel and p-channel are in alternate states to each other. At this moment, the accumulated charge at the load capacitance is discharged from the load capacitance to GND via the n-channel network. Hence the signal transition can be considered as the barometer for power consumption.

Power estimation techniques, and estimating the signal transition, can be categorized by statistical approaches [5, 6] and probabilistic approaches [1-4]. However regardless of the power estimation approach adopted, how to determine the input pattern and how to handle the signal are very important factors.

It is known that there are probabilistic approaches and statistical approaches in power estimation. However it is commonly accepted that the statistical approach is generally more accurate but more time consuming than probabilistic approaches. The probabilistic approach is generally to use signal probability and is based on the spatio-temporal independence of the input signal and the zero delay model. In this approach, forced probability to primary inputs in circuits is to propagate from primary inputs to primary outputs for computation of each node's probability. Then each node power consumption and total power consumption is computed by multiplying the used operating frequency with the computed signal probability of each circuit node. As an advanced approach, a transition probability estimation methodology was proposed [7]. This method considered arbitrary signal transition behavior and improved the accuracy of the signal transition probability.

Other approaches [1, 4] propagate the input transition density value through the whole circuit, being based on the assumption that all the inputs of each gate have spatio-temporal independent characteristics. This approach requires the input signal transition density value and the signal probability of the input signal to compute the signal transition density by applying the Boolean difference [1].

The power estimation method can be divided into two approaches. The first one is to apply the operating frequency on each node's signal transition probability that has been computed by propagating the probability of

the primary input signal through the whole logic node to the primary output. If a temporal independence is assumed, the transition probability is expressed as follows,

$$P_{0\to1}(y) = P(y=0)P(y=1) = (1-P(y=1))P(y=1) \quad (1)$$

where the P(y) for each gate is shown in table.

〈Table 1〉 The Signal Probability Computation for AND and OR Gates

	P(y = 0)	P(y = 1)
AND	$(1-P_{x1}P_{x2})$	$P_{x1}P_{x2}$
OR	$(1-P_{x1})(1-P_{x2})$	$(1-(1-P_{x1})(1-P_{x2}))$

The actual transition is twice $P_{0\to1}$ because the transition has occurred during change of a state, 0 to 1 and 1 to 0. After obtaining the transition probability, the estimated power consumption for each node can be computed by,

$$P(x) = \frac{1}{2T_c} V_{dd}^2 P_t(x) C_i \quad (2)$$

$$P_{total} = \sum_{x \in all-node} P(x) \quad (3)$$

where T_c is the clock period, C_i is the total capacitance and P_t is $2P_{0\to1}$.

Since power estimation is obtained by multiplying the operating frequency with each node's transition probability, this method can not consider the local transition density variation. In order to overcome this problem, a transition density propagation method was proposed [1] and this method was used as a cost function for low power synthesis [8]. The transition density propagation is expressed by,

$$D_p(y) = \sum_{i=1}^{n} P\left(\frac{\partial y}{\partial x_i}\right) D_p(x_i) \quad (4)$$

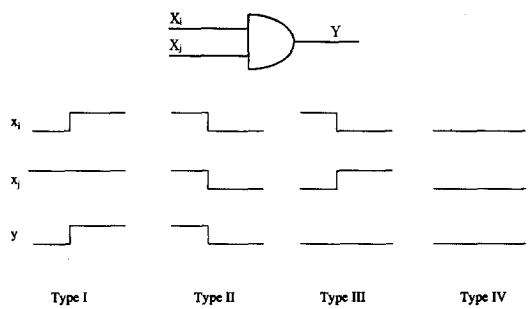
where $D_p(x)$ is the transition density that is explained by the amount of transition in a given time interval. $\partial y/\partial x_i$ is known as the Boolean difference that is expressed by

$$\frac{\partial y}{\partial x_i} = y|_{x_i=1} \oplus y|_{x_i=0} \quad (5)$$

Since the probability of the Boolean difference shows how input change affects the output signal transition, equation (4) can mean that the input signal transition density is propagated to the output node by the probability of the Boolean difference.

3. Advanced Transition Density Propagation

The eventual purpose of this paper is to improve the accuracy of power estimation by considering the simultaneous signal effects and the correlation factor that degrades the accuracy of power estimation in the conventional method.

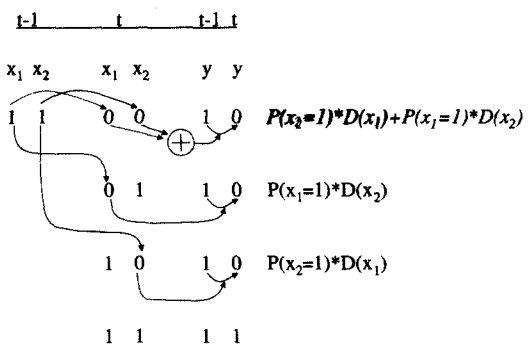


(Figure 1) 4 Types of Transition Density Propagation

As shown in equation (4), the density propagation equation can explain the density propagation behavior characteristics at gate level. From our observations, there is some redundancy in the process of transition density propagation. (Figure 1) shows that the density propagation behavior of input and output signals for an AND gate. In this figure, all of the input signals can be categorized in 4 groups.

- Type I : all of the input transition density can be propagated by TDPE(Transition Density Propagation Equation).
- Type II : Some of the input density should be eliminated from density propagation by TDPE.
- Type III : All of input density should be eliminated from density propagation by TDPE.
- Type IV : There is no propagation by TDPE and there is no actual density propagation.

Among the 4 groups, the propagation behavior of the type I and the type II is in accordance with TDPE exactly. Type III has been shown that there should be the additional consideration for redundancy [4]. From our observation, type II should also be taken into account to improve the accuracy of power estimation. One of the relationships between the input signal and output signal is shown in (Figure 2). (Figure 2) shows that the input signal transition from the previous input logic state '11' to the current input logic state '00' has more density propagation than is actually the case. In this figure, each signal transition density, $D(x_1)$ and $D(x_2)$, is propagated by the amount of the probability : $P(x_2=1)$ and $P(x_1=1)$. Even if both signal transitions can not contribute to the output signal transitions separately; actually the transition density of the signal x_1 and x_2 are propagated by each corresponding other input signal probability that is derived from Boolean difference of equation (3).



(Figure 2) The Transition Behavior

Example 1.

As shown in (Figure 2), if it is assumed that the transition density $D(x_1)$ and $D(x_2)$ is 1 and the probability of both input signals are 0.5, the propagated density is 1(1*0.5+1*0.5). However the output signal transition density is actually approximately 0.75. Hence there exists a 25% power estimation error.

From (Figure 2) and example 1, it is known that this redundancy effect should be eliminated to increase the accuracy of power estimation. In order to overcome the limitation of equation (4), the density propagation equation that considers the redundancy factor will be presented. Before suggesting density propagation equation, several terms will be defined. If output signal y has x_1, x_2, ···, x_n as primary input, several sets are defined as S = {1, 2, 3, ···, n} and its subset S_i = {all subset of S and n(subset) = i}.

Lemma 1. Empty set

If L = {0, 1},

then

$$P_{i\to i}(x_\phi) = 1$$

where i is an element of set L.

Lemma 2. Multiplication

If L = {0, 1},

then

$$\prod P_{i\to i}(x_{\{1,2,\cdots,m\}}) = \prod_{k=1}^{m} P_{i\to i}(x_k)$$

where i is an element of set L.

Lemma 3. Expansion

$$\underset{i\in\{1,2,\cdots,m\}}{\beta}\{D(x_i)\} = \beta\{D(x_1), D(x_2), \cdots, D(x_m)\}$$

where β can be displaced by *max* or *min* depending on the gate type.

And the equation for density propagation is as follows,

$$D_p(y) = \sum_{i=1}^{n} P\left(\frac{\partial y}{\partial x_i}\right) D_p(x_i) - 4\sum_{i=2}^{n}\left[\sum_{\forall j\in S_i}\prod_{j} P_{0\to 1}(x_j)\prod_{k\in(S-j)} P_{i\to i}(x_k)\left[\sum_{m=1}^{n} D_p(x_m) - \sum_{m\in(S-j)} D_p(x_m) - \underset{m\in j}{\beta}\{D(x_m)\}\right]\right] \quad (6)$$

where β is *max* and *min* for OR and AND gate respectively. In this equation, *max* and *min* is introduced to take into consideration the more accurate elimination of the redundancy factors. In the case of an AND gate, *max* should be substituted with β because output signal transition density of AND gate is governed by the least input signal transition density among inputs.

Expansion for 3-input OR gate.

If $y = x_1 + x_2 + x_3$ and each density and probability are $D(x_1)$, $D(x_2)$, $D(x_3)$, $P(x_1)$, $P(x_2)$ and $P(x_3)$ respectively, the Boolean difference is,

$$P\left(\frac{\partial y}{\partial x_1}\right) = P((x_2 + x_3) \oplus 1) = P(\overline{x_2 + x_3}),$$

$$P\left(\frac{\partial y}{\partial x_2}\right) = P((x_1 + x_3) \oplus 1) = P(\overline{x_1 + x_3}),$$

and $P\left(\frac{\partial y}{\partial x_3}\right) = P((x_1 + x_2) \oplus 1) = P(\overline{x_1 + x_2})$. In here, $S = \{1, 2, 3\}$, $S_2 = \{\{1, 2\}, \{2, 3\}, \{1, 3\}\}$ and $S_3 = \{\{1, 2, 3\}\}$. And second term is reduced,

$$\begin{aligned}
&-4\sum_{i=2}^{3}\Big[\sum_{\forall j\in S_i}\prod_{j}P_{0\to1}(x_j)\prod_{k\in(S_i-j_i)}P_{1\to1}(x_k)\\
&\quad\Big[\sum_{m=1}^{3}D_p(x_m)-\sum_{m\in(S-j)}D_p(x_m)-\min_{m\in j}\{D(x_m)\}\Big]\Big]\\
&=-4\sum_{\forall j\in S_2}\prod_{j}P_{0\to1}(x_j)\prod_{k\in(S_1-j)}P_{1\to1}(x_k)\\
&\quad\Big[\sum_{l=1}^{3}D_p(x_l)-\sum_{l\in(S-j)}D_p(x_l)-\min_{l\in j}\{D(x_l)\}\Big]\\
&\quad-4\prod_{j\in S_3}P_{0\to1}(x_j)\prod_{k\in(S-j)}P_{1\to1}(x_k)\\
&\quad\Big[\sum_{l=1}^{3}D_p(x_l)-\sum_{l\in(S-j)}D_p(x_l)-\min_{l\in j}\{D(x_l)\}\Big]\\
&=-4\prod P_{0\to1}(x_{\{1,2\}})\prod P_{1\to1}(x_{\{3\}})\\
&\quad\Big[\sum_{l=1}^{3}D_p(x_l)-D_p(x_{\{3\}})-\min\{D(x_{\{1,2\}})\}\Big]\\
&\quad-4\prod P_{0\to1}(x_{\{1,3\}})\prod P_{1\to1}(x_{\{2\}})\\
&\quad\Big[\sum_{l=1}^{3}D_p(x_l)-D_p(x_{\{2\}})-\min\{D(x_{\{1,3\}})\}\Big]\\
&\quad-4\prod P_{0\to1}(x_{\{2,3\}})\prod P_{1\to1}(x_{\{1\}})\\
&\quad\Big[\sum_{l=1}^{3}D_p(x_l)-D_p(x_{\{1\}})-\min\{D(x_{\{2,3\}})\}\Big]\\
&\quad-4\prod P_{0\to1}(x_{\{1,2,3\}})\prod P_{1\to1}(x_{\phi})\\
&\quad\Big[\sum_{l=1}^{3}D_p(x_l)-\min\{D(x_{\{1,2,3\}})\}\Big]\\
&=-4P_{0\to1}(x_1)P_{0\to1}(x_2)P_{1\to1}(x_3)[D_p(x_1)+D_p(x_2)\\
&\quad-\min\{D_p(x_1),D_p(x_2)\}]\\
&\quad-4P_{0\to1}(x_1)P_{1\to1}(x_2)P_{0\to1}(x_3)[D_p(x_1)+D_p(x_3)\\
&\quad-\min\{D_p(x_1),D_p(x_3)\}]\\
&\quad-4P_{1\to1}(x_1)P_{0\to1}(x_2)P_{0\to1}(x_3)[D_p(x_2)+D_p(x_3)\\
&\quad-\min\{D_p(x_2),D_p(x_2)\}]\\
&\quad-4P_{0\to1}(x_1)P_{0\to1}(x_2)P_{0\to1}(x_3)[D_p(x_1)+D_p(x_2)\\
&\quad+D_p(x_3)-\min\{D_p(x_1),D_p(x_2),D_p(x_3)\}
\end{aligned}$$

Finally all expressions are as follows,

$$\begin{aligned}
D_p(y) &= (1-P(x_2))(1-P(x_3))D(x_1)\\
&\quad+(1-P(x_1))(1-P(x_3))D(x_2)\\
&\quad+(1-P(x_1))(1-P(x_2))D(x_3)\\
&\quad-4P_{0\to1}(x_1)P_{0\to1}(x_2)P_{1\to1}(x_3)[D_p(x_1)\\
&\quad+D_p(x_2)-\min\{D_p(x_1),D_p(x_2)\}\\
&\quad-4P_{0\to1}(x_1)P_{1\to1}(x_2)P_{0\to1}(x_3)[D_p(x_1)\\
&\quad+D_p(x_3)-\min\{D_p(x_1),D_p(x_3)\}\\
&\quad-4P_{1\to1}(x_1)P_{0\to1}(x_2)P_{0\to1}(x_3)[D_p(x_2)\\
&\quad+D_p(x_3)-\min\{D_p(x_2),D_p(x_2)\}\\
&\quad-4P_{0\to1}(x_1)P_{0\to1}(x_2)P_{0\to1}(x_3)[D_p(x_1)\\
&\quad+D_p(x_2)+D_p(x_3)\\
&\quad-\min\{D_p(x_1),D_p(x_2),D_p(x_3)\}
\end{aligned}$$

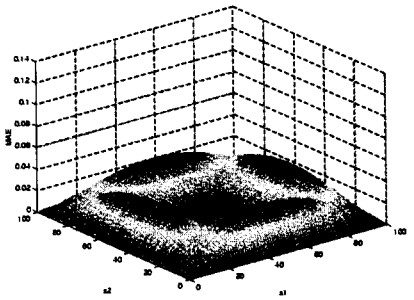
In the case of a 3-input AND gate, all of terms that are shown in the 3-input OR gate example are the same except for changing *min* to *max*, and the first term.

4. Simulation and Result

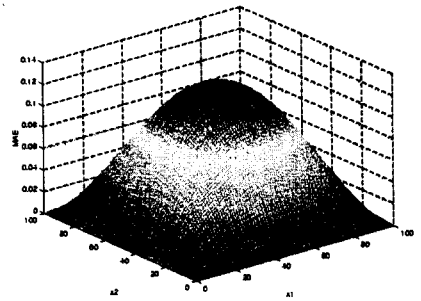
The proposed transition density propagation equation uses signal probability and the transition density to compute the signal transition density in CMOS circuits. Accurate computation of the signal density propagation has a very crucial role in power estimation because this is not only for measuring the exact density propagation but also for being used in low power logic synthesis as a cost function.

However exact power estimation is known as NP-hard [1]. In practice, the probability of the input can not be determined when power estimation is computed. In our observation, the performance of power estimation should be evaluated by how much accuracy of power estimation is obtained for a certain gate type and for various signals' probability. Hence our simulation considered this aspect by varying the input signal probability of a certain gate. We suggest that the good performance of this kind of simulation can guarantee good performance for real logic circuits. In this simulation, the proposed power estimation methodology, Najm's methodology, Chou's methodology and the simulation approach are implemented in C. The simulation approach used a random signal as its input signal whose probability is in the range of 1 and 0 and applied on an AND gate and an OR gate. The signal transition

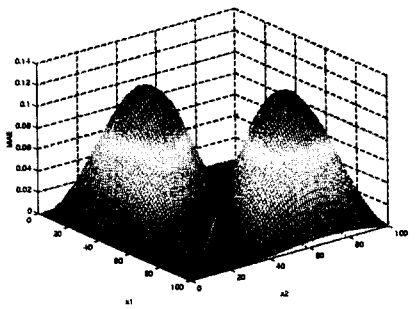
density and its probability of random signal is obtained from the simulation approach and this data is also used as input pattern in probabilistic approaches : the proposed power estimation methodology(ADTPE), Najm's (DTPE) and Chou's(MDTPE). (Figure 3) shows the simulation result of 2-input OR and AND gates. In this figure, x and y axis are the probability of each input and z axis is the signal transition density difference between the simulation approach and each probabilistic approaches. As shown in the figure, the proposed methodology has better accuracy than Najm's and Chou's methods over entire probability, especially around the center part of x-y plain. In these figures, our proposed method shows better accuracy, especially around the propability 0.5, compared to the other two methods.



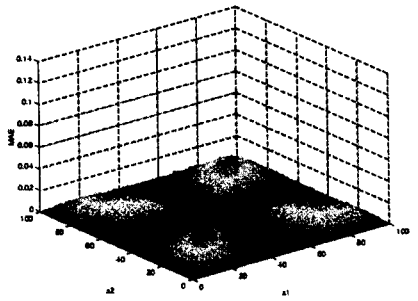
(a) ATDPE for OR Gate



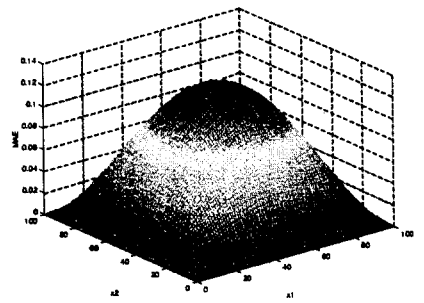
(b) TDPE for OR Gate



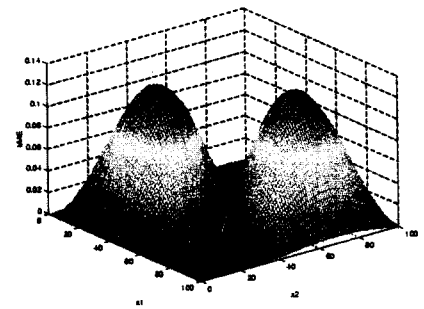
(c) MTDPE for OR Gate



(d) ATDPE for AND Gate



(e) TDPE for AND Gate



(f) MTDPE for NAD Gate

(Figure 3) Result of an Absolute Error for 2 Input Gates

In <Table 2> and <Table 3>, each acronym stands for three methods : the proposed method(ATDPE), Najm's(TDPE) and Chou's(MTDPE). In this experiment, the operating frequency is assumed to be 1MHz and the resulting signal transition density is normalized by this operating frequency. As shown in <Table 2>, the proposed methodology shows the better performance with respect of mean absolute error, being obtained between the simulation approach and other three probabilistic approaches, and its standard deviation.

〈Table 2〉 Comparison for 2 Input Gates

	OR			AND		
	ATDPE	TDPE	MTDPE	ATDPE	TDPE	MTDPE
Mean Error	0.0174	0.0556	0.0418	0.005	0.0556	0.0418
Std. Dev.	0.0087	0.0369	0.0363	0.0048	0.0369	0.0363

〈Table 3〉 Comparison for 3 Input Gates

		OR		AND	
	$P(x_3=1)$	ATDPE	TDPE	ATDPE	TDPE
Mean Error	0.25	0.0311	0.0945	0.0073	0.0654
	0.5	0.0242	0.0980	0.0013	0.0963
	0.75	0.0226	0.0669	0.0099	0.0934
Std. Dev.	0.25	0.0112	0.0482	0.0061	0.0361
	0.5	0.0123	0.0505	0.0012	0.0521
	0.75	0.0092	0.0352	0.0080	0.0497

Instructions used in each method were compared to obtain information about its complexity. <Table 4> shows that Najm's method has the best performance with respect to elapsed time for computation. But even though our proposed method has better performance than Chou's method, it is expected that they have similar elapsed time.

〈Table 4〉 Complexity Comparison for Each Method(2-input)

	ATDPE		TDPE		MTDPE	
	OR	AND	OR	AND	OR	AND
Addition	9	4	6	1	11	8
Multiplication	8	8	4	4	8	8
Division	0	0	0	0	2	2
If-else	1	1	0	0	0	0

5. Conclusion

In this paper, we explored the redundancy factors in the process of the signal transition density propagation. We proposed the advanced signal transition density propagation methodology for the zero delay model to be a good criteria for the lower boundary of power consumption. In addition, we showed that this proposed methodology has the comparably better performance than the other two methods : Najm's and Chou's.

Even if the zero delay model can be applied as a criteria for the lower boundary power consumption, additionally the glitch effect also should be taken into consideration in the power consumption for real digital circuits.

References

[1] F. Najm, "Transition density : a new measure of activity in digital circuits," IEEE transaction on Computer-Aided Design, pp.224-228, November 1993.

[2] A. Ghosh, S. Devadas, K. Keutzer, and J. White, "Estimation of average switching activity in combinational and sequence circuits," ACM/IEEE Design Automation Conf, pp.253-259, 1992.

[3] J. Monteiro, S. Devadas, B. Lin, C-Y. Tsui, M. Pedram, and A. Despain, "Exact and approximate methods of switching activity estimation in sequential circuits," Intl. Workshop on Low Power Design, Napa Valley, 1994.

[4] T. Chou, K. Roy, and S. Prasad, "Estimation of circuit activity considering signal correlations and simultaneous Switching," IEEE/ACM International Conference on Computer-Aided Design, pp.300-303, 1994.

[5] C. M. Huizer, "Power dissipation analysis of CMOS VLSI circuits by means of switching-level simulation," IEEE European Solid State Circuits Conference, pp.61-64, 1990.

[6] R. Burch. F. Najm, P. Yang, T, Trick, "McPOWER : a Monte Carlo approach to power estimation," IEEE/ACM International Conference on Computer-Aided Design, pp.90-97, 1992.

[7] Q. Wu, M. Pedram and X. Wu, "A note on the relationship between signal probability and switching activity," Proc. of Asia and South Pacific Design Automation Conf., pp.117-120, 1997.

[8] R. Panda and F. N. Najm, "Technology-dependent transformations for low-power synthesis," 34th Design Automation Conference, pp.650-655, 1997.

김 동 호

e-mail : donghkim@ece.utexas.edu

1990년 경북대학교 전자공학과 학사

1992년 경북대학교 전자공학과 석사

1992년~1997년 LG전자 주임 연구원

1997년~현재 Univ. of Texas at Austin 전기 컴퓨터 공학과 박사과정

1998년~1999년 AMD Software Test Engineer

관심분야 : Power Estimation, Low Power Synthesis 및 Computer Arithmetic

우 종 정

e-mail : jwoo@cs.sungshin.ac.kr

1982년 경북대학교 전자공학과 학사

1982년~1988년 산업연구원 책임 연구원

1988년~1993년 Univ. of Texas at Austin 전기 컴퓨터 공학과 석사 및 박사

1998년~1999년 Univ. of Texas at Austin 전기 컴퓨터 공학과 Visiting Scholar.

1993년~현재 성신여자대학교 교수

관심분야 : 병렬처리, 컴퓨터구조, 멀티미디어시스템, CAD