The Effect of Dielectric Thickness and Barrier Rib Height on Addressing Time of Coplanar ac PDP

Sung-Hyun Lee, Young-Dae Kim, Joong-Hong Shin, Jung-Soo Cho and Chung-Hoo Park

Abstract - The addressing time should be reduced by modifying cell structure and/or driving method in order to replace the dual scan system by single scan and increase the luminance in large ac plasma display panel(PDP). In this paper, the effects of the dielectric layer thickness and the barrier rib height on the addressing time of ac PDP are investigated. It is found out that the addressing time was decreased with decreasing thickness of dielectric layer on the front glass and thickness of white dielectric layer on the rear glass. The decreasing rate were 160ns/10㎛ and 270ns/10㎛, respectively. Also in case of decreasing the height of barrier rib, addressing time was decreased at the rate of 50ns/10㎛.

Key Words - AC PDP, addressing time, dielectric layer, barrier rib

1. Introduction

One of the most important problems in address-display separated(ADS) scheme[1,2] in ac plasma display panels (PDP) is that they have too long addressing period. One line scanning time is about 3㎲, so that the time for 480 lines in VGA resolution is about 1.4ms. A frame consists of 8 sub-field for 256 gray level. Therefore, the total addressing time is 11.52ms, which is about 70% of one frame. As the addressing time increases, the sustaining period for display image should be decreased. As a result, the luminance of the PDP decreases.

The dual scan method has adopted to solve this problem in a large ac PDP. In this case the scanning period can be half reduced compared with single scan. However, the driving circuit cost increase is inevitable. In case of the high definition TV(HDTV) whose scan line is more than VGA resolution, the addressing speed will be big issue[3]. The addressing time depends strongly on the cell geometry and on the thickness of the dielectric layers on the display and address electrodes[4].

In this study, we investigated the effect of the dielectric thickness and barrier rib height on the addressing time of ac PDP.

2. Experimental

Fig. 1 shows a well-known coplanar ac PDP cell and Table 1 shows the spec. of 4 inch model PDP in this study with VGA resolution. The electrode shapes of the conventional discharge sustain electrode X, scan/discharge sustain electrode Y and address electrode A are shown in Fig. 1 which is well known as 3 electrodes stripe structure [5,6].

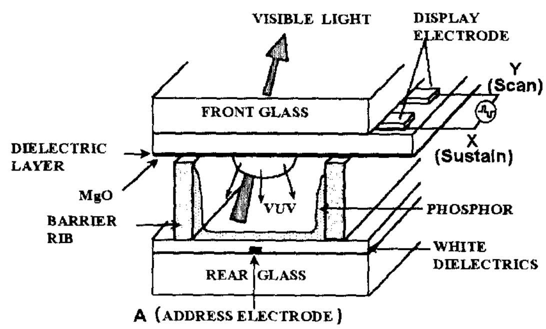

Fig. 1 The schematic diagram of model ac PDP

Table 1 Spec. of 4-in ac PDP

Front panel		Rear panel	
ITO width	310㎛	Address electrode width	100㎛
ITO gap	60㎛	White back thickness	15㎛
Bus width	100㎛	Rib height	150㎛
Dielectric thickness	25㎛	Rib pitch	360㎛
MgO thickness	5000Å	Rib width	70㎛
		Phosphor thickness	15㎛

Fig. 2 shows the driving waveform in order to detect the addressing time in the addressing period. The applied voltage pulses for each electrode is listed in the Table 2. One sequence of this driving scheme is about 2ms, and this sequence is repeated. In order to eliminate the cross-talk phenomena, the address electrodes are addressed in alternate lines.

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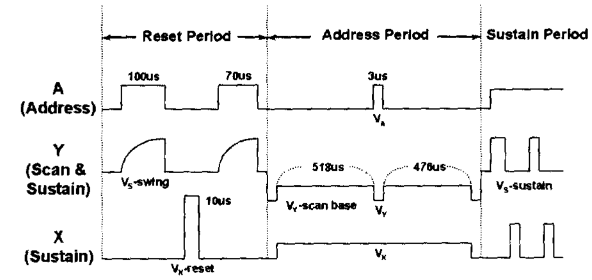
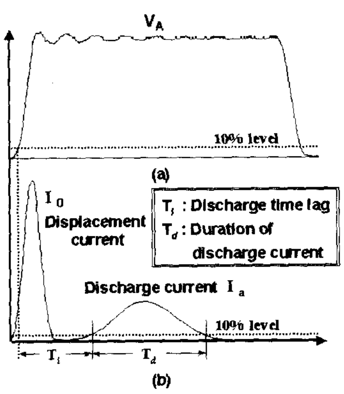


Fig. 2 The schematic diagram of driving waveform in the experimental(ADS method)

Table 2 The conditions of applied voltage

V_Y	-150~160V
V_Y_scan base	-50V
V_A	100~120V
V_X	90V
V_X_reset	380V
V_S_sustain & swing	180V
Rising time of addressing pulse	100ns/100V

Fig. 3 shows the typical waveform of addressing pulse voltage V_A, charging current I0 (displacement current) and addressing discharge current I_a by gas discharge. The discharge time lag T_l and the duration of discharge current T_d are also denoted in the Fig. 3. The T_l is the period of time which elapses between the application of an electric field and the onset of a breakdown, and T_d is the sustained time of the addressing discharge current. Since the addressing discharge process is finished in the time of the $T_l + T_d$, the addressing time is determined by the $T_l + T_d$[7].



(a) Applied voltage waveform

(b) Displacement and Discharge current waveform

Fig. 3 The definition of T_l and T_d.

3. Results and Discussion

Fig. 4 shows the addressing time characteristics as a parameter of the thickness of dielectric layer on the display electrodes. The discharge time lag and addressing time increase with increasing the dielectric thickness, as shown in Fig. 4.

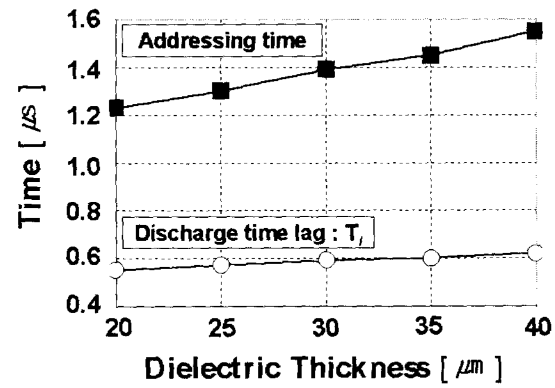


Fig. 4 The addressing time as a parameter of dielectric thickness

These results may be explained as follows. Fig. 5(a) shows a pair of sustain electrode arrangement in a discharge cell. Fig. 5(b) shows the capacitance equivalent circuit of the Fig. 5(a). C_g is the capacitance of space gap and C_d is the capacitance of dielectric layer. Before the discharge starts, the gap voltage appearing across the discharge space decreases with increase in the dielectric thickness (d) in Fig. 5.[8] Therefore, the discharge time lag increases with the thickness (d) of dielectric layer under the same applied voltage condition.

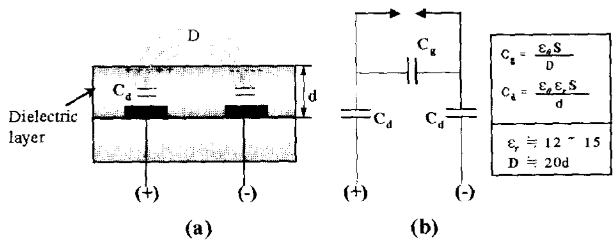


Fig. 5 Sustain electrode arrangement and capacitance equivalent circuit in a discharge cell.

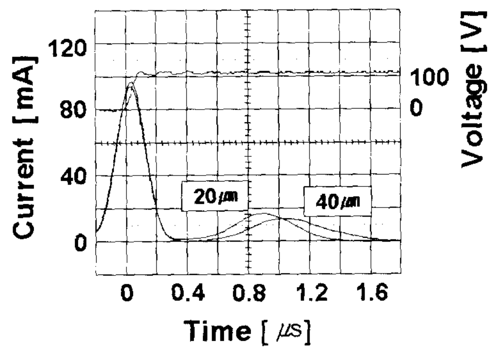


Fig. 6 The current waveforms as a parameter of dielectric thickness

Fig. 6 shows a typical current waveforms when the thickness of dielectric layers on the display electrodes are 20 ㎛ and 40 ㎛. The discharge time lag and addressing time increased with the thickness of white dielectric layer. The increasing rates of the discharge time lag and addressing time are 35ns/10 ㎛ and 160ns/10 ㎛, respectively.

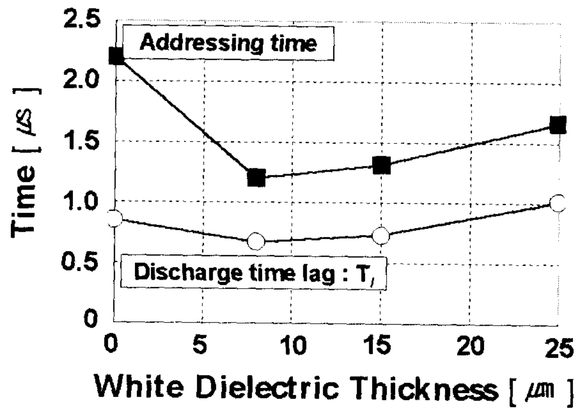


Fig. 7 The addressing time as a parameter of white dielectric thickness

Fig. 7 shows the addressing time as a parameter of the thickness of white dielectric layer on the address electrodes. In case of increase in the white dielectric layer, the gap voltage decreases, whereas the discharge time lag increases. The reason may be the same as the dielectric layer on display electrodes as described in Fig. 4. During the address pulse, a discharge starts between the Y and A electrodes, as shown in Fig. 1. The plasma first forms close to the dielectric surface above the A electrode(anode), and then expands towards the Y electrode(cathode).[9] At this point, the successive discharge forms between the X and Y electrode due to the first discharge. At the end of the address pulse, the positive charges are accumulated on the dielectric surfaces above Y electrode and the negative charges are accumulated on the dielectric surfaces above X and A electrodes, respectively. These charges called wall charges above the X and Y electrodes are going to make possible gas breakdown between X and Y electrodes during the sustain period.[6] However, without the white dielectric layer, most of negative charges flow in A electrode. Consequently, the width of current waveform and addressing time increase. Also, the sustaining discharge between X and Y electrodes may not be occurred due to deficiency of negative wall charge above the X electrode.

Fig. 8 shows a typical current waveforms when the thickness of the white dielectric layer are zero, 15 ㎛ and 25 ㎛. The discharge time lag and addressing time increased with the thickness of white dielectric layer. The increasing rates of the discharge time lag and addressing time are 200ns/10 ㎛ and 270ns/10 ㎛, respectively.

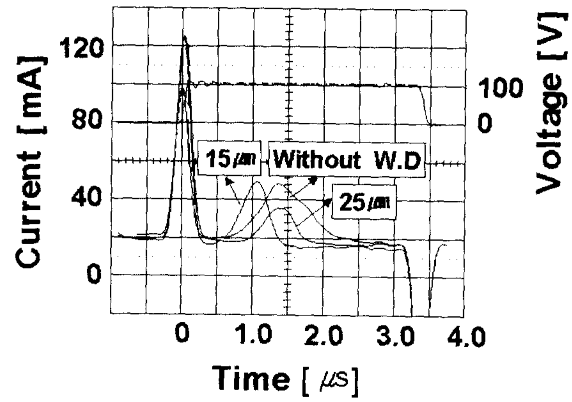


Fig. 8 The current waveforms as a parameter of white dielectric thickness

Fig. 9 shows the addressing time as a parameter of the height of barrier rib. In ac PDP, the barrier ribs are used to prevent electrical and optical interaction (cross-talk) between the cell, and also play an important role in the UV-visible photon conversion since a layer of phosphor is deposited on the rib walls. The discharge time lag increases with the rib height, as shown in Fig. 9. At the address period, when the rib height increase, that is to say, the discharge gap between A and Y electrode increase, the breakdown voltage and discharge time lag increase according to Paschen's law. However, when the rib height was below 80 ㎛, the sustain voltage increased due to reduction of discharge area and diffusion loss of plasma in sustain period.[10]

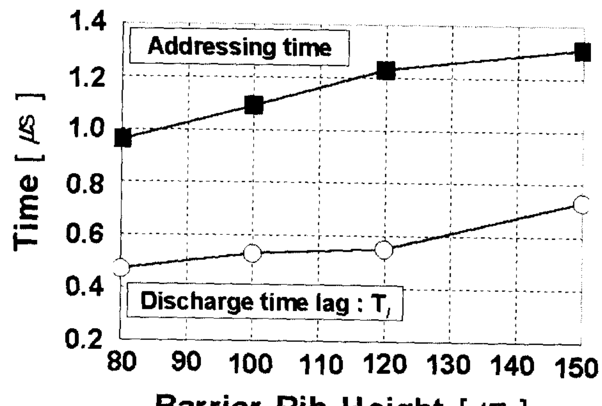


Fig. 9 The addressing time as a parameter of rib height

Fig. 10 shows a typical current waveforms when the height of the barrier rib are 100 ㎛ and 150 ㎛. The discharge time lag and addressing time increased with the height of barrier rib. The increasing rates of the discharge time lag and addressing time are 37ns/10 ㎛ and 50ns/10 ㎛, respectively.

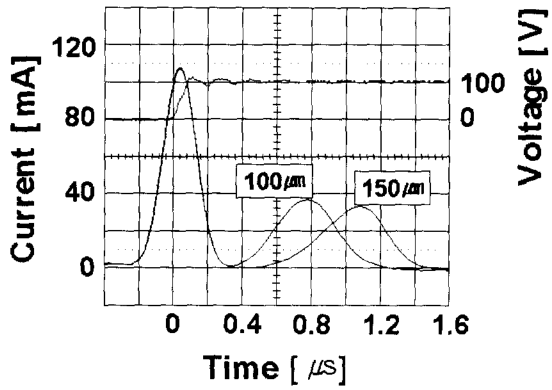


Fig. 10 The current waveforms as a parameter of rib height

4. Conclusion

In this paper, the effect of dielectric thickness and barrier rib height on the discharge time lag and addressing time are investigated.

The discharge time lag and addressing time were increase with the thickness of dielectric layer, and the increasing rate were 35ns/10 ㎛ and 160ns/10 ㎛, respectively.

The discharge time lag and addressing time were increased with the thickness of white dielectric layer on address electrode. The increasing rate were 200ns/10 ㎛ and 270ns/10 ㎛, respectively.

When the phosphor thickness 15 ㎛, the most reasonable rib height was 100 ㎛ from addressing and sustaining discharge point of view, and the discharge time lag and addressing time were increased with the height of barrier rib at the rate of 37ns/10 ㎛ and 50ns/10 ㎛ with decreasing height of barrier rib, respectively.

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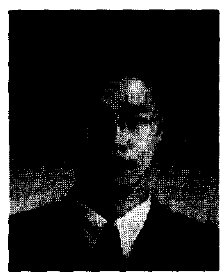

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