A Review of SiC Static Induction Transistor (SIT) Development for High-Frequency Power Amplifiers

Y.M. Sung, J.B. Casady and J.B. Dufrene

Abstract - An overview of Silicon Carbide (SiC) Static Induction Transistor (SIT) development is presented. Basic conduction mechanisms are introduced and discussed, including ohmic, exponential, and space charge limited conduction (SCLC) mechanisms. Additionally, the impact of velocity saturation and temperature effects on SCLC are reviewed. The small-signal model, breakdown voltage, power density, and different gate structures are also discussed, before a final review of published SiC SIT results. Published S-band (3-4 GHz) results include 9.5 dB of gain and output power of 120 W, and L-band (1.3 GHz) results include 400 W output power, 7.7 dB of gain, and power density of 16.7 W/cm.
Keywords - SiC, SIT, Static Induction Transistor, high-frequency, power-amplifier.

1. Introduction

The SiC Static Induction Transistor (SIT) is based on the original SIT concepts developed in 1950 [1] by Nishizawa, which have received continued development for the past 5 decades [2-7]. Recently, more research and development has occurred using SiC SIT's for high power, high-frequency amplifiers. Here, we review much of that reported progress. As compared to a Si Bipolar Junction Transistor (BJT), the SIT has advantages in being a majority carrier device, simpler to fabrication, voltage-controlled, and often higher breakdown voltage and input impedance. While most SIT development has occurred in Si, renewed interest in the use of SiC SIT's over the past 10 years has occurred because of SiC's ten-fold advantage (3 MV/cm) in critical field strength and nearly two-fold advantage in saturated electron velocity (1.6-2.0 x 10^{7} cm/s) [8-11]. Additionally, SiC has an extremely high thermal conductivity (θ_k = 3 W/cm·K) which far surpasses that of Si and GaAs, and helps SiC to be ideal for high-power operation. SiC device have dramatically reduced PN junction leakage currents resulting from its wide (E_g = 3.2 eV for the 4H-SiC polytype) bandgap. By use of SiC, it is thus possible to increase the voltage (and thus power) rating of high-frequency amplifiers, and also increase the power density by a factor of 4 to 10 in UHF to S-band transistors. Parasitic capacitances are reduced, by shrinking the device area while maintaining the power level and higher input/output impedance of the devices often requires little or no impedance matching. Limitations, which have slowed commercial insertion of SiC devices to date, include wafer size (75 mm maximum diameter available in 2001), wafer cost, device/epitaxy processing, and wafer defects. Detailed reviews of SiC can be found elsewhere (for example, [12, 13]).

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2. SIT Device Physics

Both recessed gate and planar SIT's have been fabricated in Si and SiC. However, because of difficulty in deep ion implantation (p-type dopant Al implanted at an energy of 380 keV has a peak range of only 0.42 • m into SiC) and the lack of diffusion at temperatures below 1800°C, the recessed gate structure has been favored in SiC. Typical recessed gate SIT structures are shown in Fig. 1, with primary differences found in the gates. The gate may be a Recessed Gate - Bottom contact (RG-B), as shown in Fig. 1a), or a RG with Sidewall and Bottom contact (RG-SB), as shown in Fig. 1b) which provides a longer gate channel length (L_g). Increasing L_g improves gate control, and transconductance (g_m), while reducing the output resistance (r_{DS}). The gate material may be formed from either a Schottky metal or a PN junction, and can be thought of as analogous to a vertical dual-gate MESFET or JFET structure, respectively. The gate depletes the channel from each side a distance (x_d) into the channel. The total channel thickness (2a or source finger width), trench width (t), and drift region length (L_{gd}) are illustrated in Fig. 1. The cartoon in Fig. 1b) is depicted in actual form by the Focused Ion Beam (FIB) image of a SiC SIT fabricated by Northrop Grumman shown in Fig. 1c) [12]. In Fig. 1c), the solid metal air bridge is shown which connects the source fin-

gers with low parasitic gate-to-source capacitance (C_{gs}), while the back side drain contact is not shown. Planar gates can also be fashioned in SiC [14], but the recessed gate with a Schottky barrier offers the lowest parasitics and most efficient gating [6]. A PN junction gate can be used with higher gate resistance (R_G), but offers less gate-to-source leakage and potentially higher power density. The

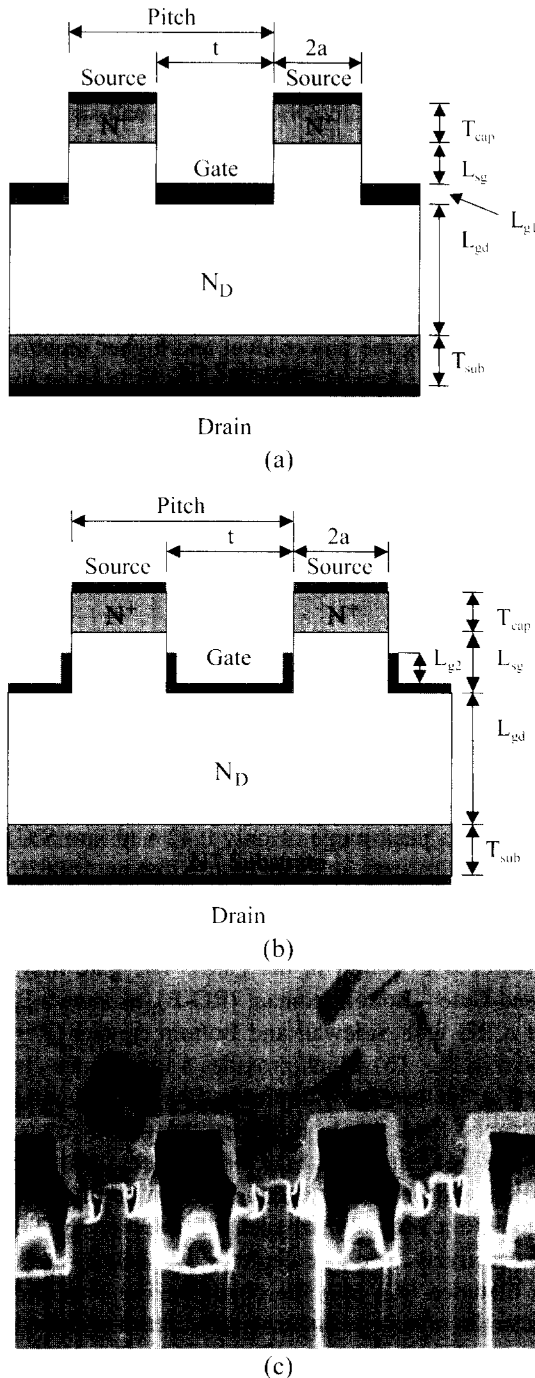


Fig. 1 Cross-sectional cartoons of a) SiC recessed gate SIT with bottom contact, b) SiC recessed gate SIT with bottom and sidewall gate contact, and c) FIB of a SiC SIT developed at Northrop Grumman.

PN gate leakage at high temperatures in SiC devices is substantially reduced (proportional to the intrinsic carrier concentration of n_i or n_i^2) compared to Si or GaAs devices.

2.1 D.C. Operation

With $V_G = V_S = 0$ V, the conventional SIT has its channel completely depleted ($x_d > a$). If $x_d < a$ (often done to increase maximum total current and power), then the SIT is referred to as mixed-mode [5]. Other terms for the SIT include gridstor, VFET, or Permeable Base Transistor (PBT) [6]. PBT's often have extremely short gates ($L_g < a < x_d$). The VFET nomenclature is generally reserved for devices with saturated drain-source output curves, unlike the triode characteristics of the SIT. The SIT name itself refers to the fact that the output characteristics are modified by static induction (see detailed explanation in exponentional conduction region as described below) and not just the input (gate) voltage as is the case for conventional FET's in the saturation mode. There are three basic conduction mechanisms possible when the SIT is on, known as the ohmic, exponential, and Space Charge Limited Current (SCLC) regions, which are identified in Fig. 2 for a simulated RG-SB SIT in SiC with a channel and drift region doped at 5×10^{15} cm^{-3}. (One may increase the channel doping to increase the total maximum current.) The transistor conduction mechanisms are two-dimensional, and a short basic description of the various regimes is given below, while more detailed explanations can be found elsewhere [3-7]. Current flow is modified by gate, drain, and source potentials, through a saddle point minima between the gate electrodes, as shown by the three-dimensional conduction band energy distribution in Fig. 3, where the minima is located at the mid-point of the channel.

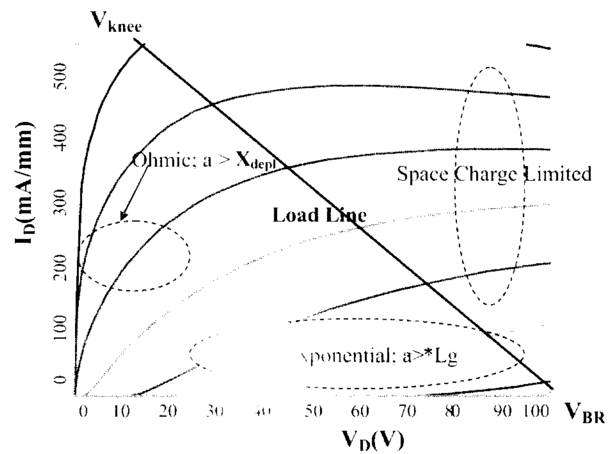


Fig. 2 Simulated output characteristics of a SiC RG-SB SIT with channel and drift-region doping at $N_D = 5 \times 10^{15}$ cm^{-3}. The drift region length is 4.0μm, L_G is 0.6μm, the trench depth is 1.0μm, and the trench width is 1.2μm with a Schottky metal gate.

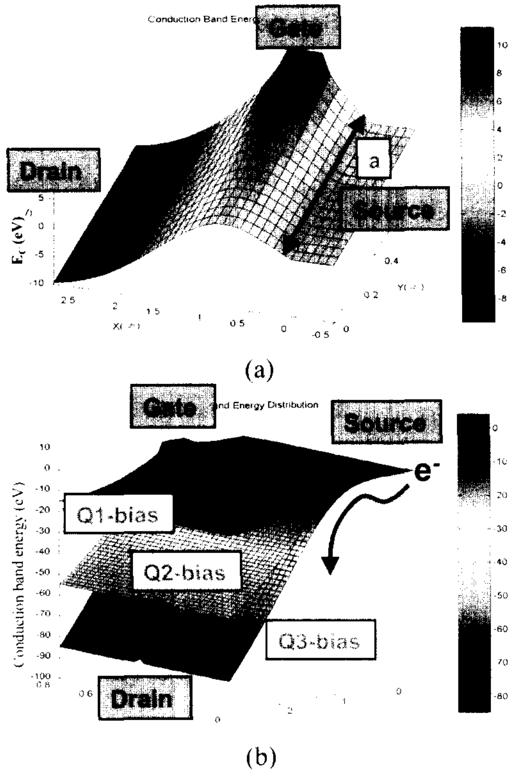


Fig. 3 Conduction band energy diagram distribution from MEDICI for the channel region of a SiC SIT (with output characteristics shown in Fig. 2). In a), the diagram illustrates the case for a = 0.6 μm, V_D = 10 V, V_G = - 10 V, and V_S = 0 V. In b), the diagram illustrates three cases for a = 0.6 μm, V_D = 15 V, V_G = 0 V, and V_S = 0 V (Q1); V_D = 55 V, V_G = -3 V, and V_S = 0 V (Q2); V_D = 85 V, V_G = - 1 V, and V_S = 0 V (Q3).

2.1.1 Ohmic region

In the ohmic (linear) region, the channel is not completely pinched off by the depletion regions under fairly low gate and drain bias (see Fig. 2, Fig. 3a, and Fig. 3b). The current from drain-to-source (I_{DS}) is controlled by ohmic resistances found between the depletion regions under (beside) the gate, undepleted portions of the drift region, and the partially depleted portion of the channel immediately above the gate. The limiting portion is of course the region between gate depletion regions, which is often very narrow. Each channel is depleted from the gate on both sides by x_d which is given by Eqn. (1), where ε_S = 10.0 for SiC, ε_O = 8.854 x 10^{-14} F/cm^2, and N_D is the channel doping. V_{bi} and V_G represent the built-in potential and gate voltage, respectively.

$$x_d = \sqrt{\frac{2\varepsilon_S\varepsilon_O(V_{bi} - V_G)}{qN_D}} \qquad (1)$$

Where,

$$V_{bi} = \phi_B - \frac{1}{q}[\frac{E_g}{2} - kT\ln(\frac{N_D}{n_i})]$$

The quantity ϕ_B is the Schottky barrier height (typically 1.1 eV for Ni on SiC) at the metal-SiC junction. The current density in this region can be given by $J_D = qv_{nD}N_D$, and the area is simply $A=2a_{eff}Z$ per finger. The quantities a_{eff} and Z are the undepleted channel width and channel depth, respectively. In this low-field region, the current is not limited by v_{sat}, but rather proportional to the effective open area, channel doping, and low-field electron velocity (v_{nD}). For this reason, the 4H polytype of SiC is the commercially-available preferred polytype because it has the highest electron mobility.

2.1.2 Exponential region

In the exponential region, even though the channel is depleted with a low gate bias, a high drain bias influences conduction over the potential barrier in the channel from drain to source. The potential barrier in the channel (as shown in Fig. 3a and 3b for half of a 1.2 m channel thickness) between the two gate electrodes has barrier lowering in the mid-point region exponentially dependent upon the high drain bias. Since the exponential relationship exists, the current in this region can be described below in Eq (2) as exponentially dependent upon the amount of barrier lowering in the channel (ΔΦ), which is a function of the drain and gate bias [3, 6].

$$I = I_o e^{\frac{q\Delta\Phi}{kT}} \qquad (2)$$

2.1.3 Space Charge Limited Conduction region

$$J_D = 2\varepsilon_S\varepsilon_O v_{SAT}\frac{V}{L^2} \qquad (3)$$

In the Space-Charge Limited Conduction (SCLC) region the drain current can be given by Eq. (3) under velocity saturation conditions. V is the voltage drop from the contact (drain terminal) to the saddle point minima and L is the distance from the drain to the saddle point minima (L_{sg} + L_g + L_{gd}). V_{sat} is the saturated electron drift velocity. Eq. 3 can be expressed in terms of total current [6] as shown in Eq. (4). Note that total current for similar voltage and frequency rated Si and SiC devices will be quite different as L_{gd} would be an order of magnitude thinner and v_{sat} would be 1.5 to 2X higher in the case of SiC. However, in using these equations, there is an intrinsic assumption made regarding the SIT operation, which is explicitly that the electric field remains high enough (> 1x10^5 V/cm in SiC) throughout the device, so that the electron velocity remains in saturation. While this is a simplifying assumption, when not in velocity saturation, I_D and f_T will be lower. it can easily be violated, and can have significant impact on device operation (see discussion regarding temperature limits

below for example).

$$I_D = 2\varepsilon_S \varepsilon_O v_{sat} \frac{V_D}{(L_{sg} + L_g + L_{gd})^2} A_{eff} \quad (4)$$

2.1.4 Voltage gain, output resistance, transconductance, and Power Density

The voltage gain can be measured from output characteristics, and is historically denoted by the symbol μ, and given by ($\mu = -\Delta V_D / \Delta V_G$). The value of μ is proportional to values for L_g, L_{gd}, and 1/a. Other small-signal parameters such as output resistance (r_{DS}) and transconductance (g_m) can also be found from the output characteristics. In velocity saturated SCLC, the output resistance, voltage gain and transconductance can be found in Eq. 5.

$$\begin{aligned} r_{DS} &= (L_{sg} + L_g + L_{gd})^2 / 2\varepsilon_S \varepsilon_O v_{sat} A \\ g_m &= 4\varepsilon_S v_{sat} A (L_{gd} + L_{sg}/2)(L_{sg} + L_g) / ab(L_{gd} + L_g + L_{gd})^2 \\ and, r_{DS} \cdot g_m &= \mu = \frac{2(L_{gd} + L_{sg}/2)(L_{sg} + L_g)}{\varepsilon_O ab} \end{aligned} \quad (5)$$

The effect of the device feature sizes on the small-signal and cut-off frequency parameters (discussed below) is shown in Table 1. One can clearly observe the trade-off between DC voltage gain and f_T.

Table 1 Summary of parameter sizing affects on device performance.

Parameter to be increased	Voltage Gain μ	Transconductance g_m	Output Resistance r_{DS}	Cut-off Frequency f_T
L_{GD}	↑	↓	↑	↓
L_G	↑	↑	↓	↓
2a	↓	↓	↓	↑

The load line is given in Fig. 2 between V_{BR} ($I_{DS} = 0$) to I_{max} ($V_{DS} = V_{knee}$), where V_{BR} is the static breakdown voltage between drain and source. I_{max} is the maximum total current in the ohmic region at $V_G = 0$ before conduction begins to be affected by SCLC and series resistance denoted at $V_{DS} = V_{knee}$. The very high V_{BR} of SiC SIT's (up to 450 V for S-band parts has been demonstrated) allows the theoretical power density (P_D) described in Eq. 6 to be much higher than in Si. The MEDICI™ simulated breakdown in the SiC SIT shown in Fig. 4, where one can observe the high field regions in the device. Fig. 4 illustrates the simulated electric field distribution in a 4H-SiC SIT (neglecting field crowding effects at the device edge) with 4 μm drift region doped at 5×10^{15} cm^{-3} under a maximum field of 2.25 MV/cm (75% of theoretical parallel-plane breakdown) showing a gate-to-drain blocking voltage of 600 V. The maximum electric field in the device interior occurs directly under the corner of the gate in the drift region.

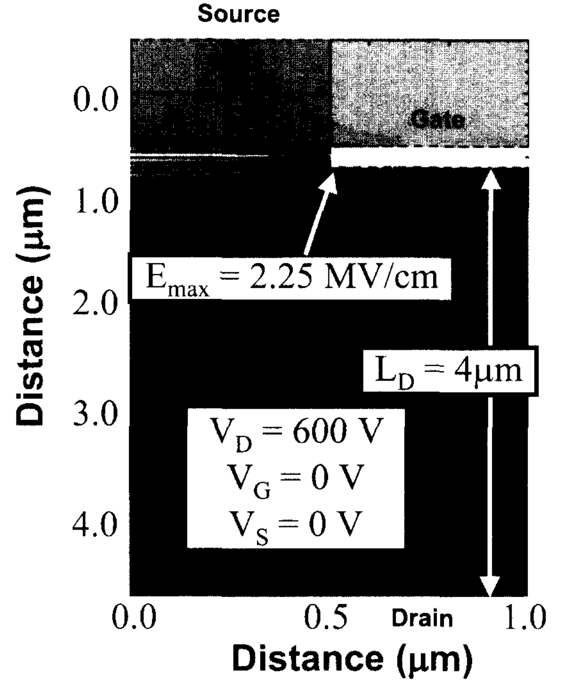


Fig. 4 Electric field contour lines from MEDICI simulation for a SiC SIT (with output characteristics shown in Figure 2). The SIT has $V_D = 600$ V, $V_G = 0$ V, and $V_S = 0$ V. A maximum field of 2.25 MV/cm is found in the interior of the device, under the corner of the gate in the drift region. This represents about 75% of the critical field, which is normally reached first at the edge of the device.

Since P_D is proportional to V_{BR}^2, and SiC's V_{BR} is nominally 10X that of Si for similar-rated parts, this translates to a 100X higher theoretical power density advantage for SiC SIT's over Si. Achieving those advantages will also require exceptional packaging technology to be implemented for SiC parts.

$$P_D = \frac{1}{8} I_{max}(V_{BR} - V_{knee}) = \frac{(V_{BR} - V_{knee})^2}{8R_L} \quad (6)$$

Using SiC provides for another advantage in broadband amplifiers, which require minimum output impedance from the transistor. Since scaling the area up in a device decreases both input and output impedance, the area of the device can be constrained by this requirement. SiC's ability to operate at higher voltages can increase the total output power while still maintaining a required output impedance.

2.2 A.C. Operation (small-signal)

The small-signal model of the SIT can be seen in Fig. 5. Of particular importance in the common-source mode is the input capacitance (C_{in}), which is given in Eq. 7, while ignoring significant effects of parasitic source and gate

resistances for simplicity. The gate-to-drain capacitance (C_{gd}) is multiplied by a large number, which is commonly known as the Miller Effect in FET's. This mode thus gives the device and circuit designer trade-offs to pursue between small-signal gain (proportional to g_m) and the bandwidth. The transit frequency (f_T) is the frequency where the short-circuit current gain is one, and is given also in Eq. 7. C_{gd} can be lowered by reducing gate area, although this can increase the gate resistance.

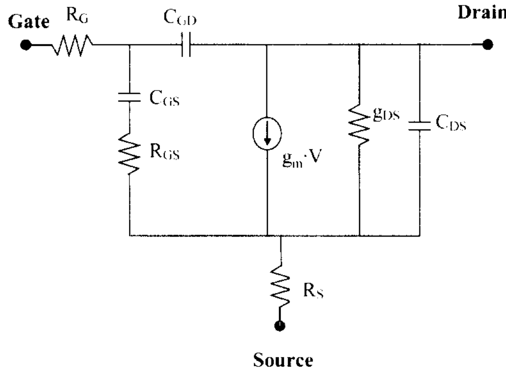


Fig. 5 Small-signal model of the SIT.

$$C_{in} = C_{gs} + C_{gd}\{1 + g_m(\frac{R_L}{1+R_L g_{ds}})\}$$

$$fT = \frac{g_m}{2\pi C in}$$

$$\approx \frac{1}{\pi} \cdot \frac{(L_{gd} + L_{sg}/2)^2 (L_{sg} + L_g)}{b \cdot L_{sg} \cdot \varepsilon_s \cdot K \cdot (L_{gd} + L_{sg}/2) + a \cdot A \cdot Z \cdot \varepsilon_s)} \quad (7)$$

From the simplified expression for f_T, one can observe a few basic design trade-offs. We have given an approximate expression in Eq. 7 by assuming $C_{gd} << C_{gs}$, and assuming $R_G = R_S = 0\ \Omega$. Increasing the drift region length (L_{gd}) and channel length (L_g) will decrease f_T, while increasing . Increasing L_{gd} also boosts the V_{BR}, and maximum power gain. Again, this is summarized in part by Table 1. Most of our discussion has focused on common-source operation, but to boost gain at higher frequencies, the common-gate mode is often employed to boost the gain by eliminating the Miller effect. However, bandwidth is often compromised in this mode, which is important since 10-15% bandwidth is required for most applications.

While beyond the scope of this review to treat fully, a brief statement concerning maximum temperature capability should be given since the ability of SiC to operate under high-temperature and/or high-power conditions is considered a key advantage. Under very high power density, the T_{jmax} can climb significantly even under modest ambient conditions. Although SiC's high thermal conductivity is a great benefit in dissipating the heat, the natural rise in temperature can degrade the performance in several ways. First, assuming the electric field is very high; f_T is controlled by the saturated drift velocity, among other parameters per Eq. 7. Rising temperature will lower v_{sat}, and thus f_T. Second, rising temperature decreases the electron mobility even faster that v_{sat}, which can cause an upward shift in the electric field required to reach velocity saturation [10]. Thus, if not designed properly, the device can slip from velocity saturated to mobility controlled SCLC, which will further decrease f_T. Finally, the increased leakage current through a Schottky gate, die attach reliability, shifts in output resistance, and other operating characteristics will also be critical at elevated junction temperatures.

3. Performance of SiC SIT Structures

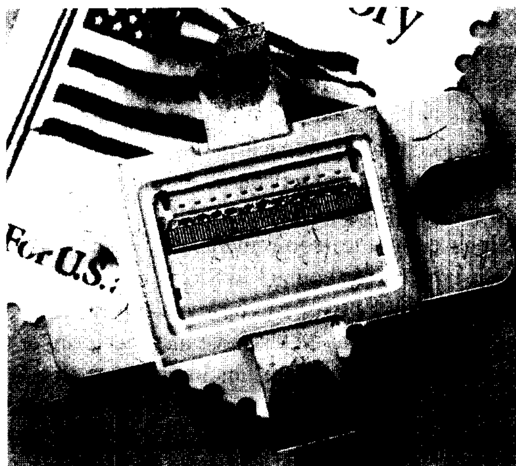
Table 2 displays results of SiC SIT performance over the past few years. Gains of up to 15 dB have been achieved at 3 GHz and 10 dB at 4 GHz. Output power as high as 165 kW/in^2 (practical Si limit is 78 W/in^2) at 600 MHz has been achieved, as well as, good linearity in class AB operation from 50 to 450 W (P_{out}) on a 34.5 cm periphery SiC SIT [15]. Along with the results shown in Table 2, Northrop Grumman has reported 4H-SiC 450 W SIT's at 600 MHz, 1kW and 2.5 kW high-definition T.V. transmitter modules at 850 MHz [14] and good linearity of SiC SIT structures in common source, class AB operation [15]. Purdue has reported unity-gain cut-off frequencies of 7 GHz [21] and 9.1 GHz [6].

4. Results and Discussion

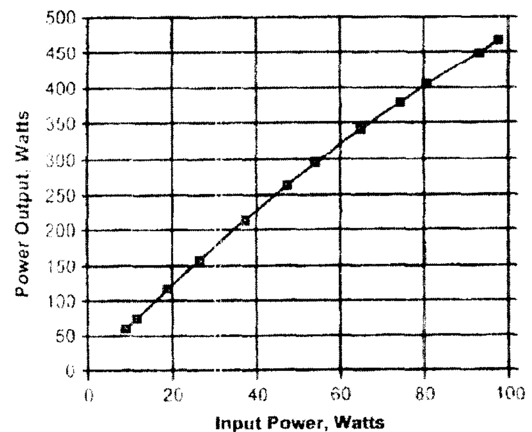
Clearly the SiC SIT's have demonstrated sufficient performance for commercial applications, including radar and digital television transmitter applications. They offer advantages in comparison to other wide bandgap high-frequency devices including a vertical structure for high power density, and no requirements for semi-insulating wafers or susceptibility to back-gating effects as is the case for MESFET's. In comparison to bipolar transistors, the SIT is a majority carrier device requiring only one dopant type, which eases the requirements for epitaxy. Additionally, the p-type ohmic contact in SiC is challenging, meaning that lowering the extrinsic base resistance will be challenging for the bipolar. SIT's have also been under development for quite sometime, including the first HDTV broadcast in 1996 [15], and a picture of the packaged parts and power linearity in common-source, class AB operation is shown in Fig. 6a) and 6b), respectively from that demonstration. A scanning electron microscope image, of a similarly completed 1.5 cm periphery SIT, with gate and source tabs shown is pictured in Fig. 7 [16].

Table 2 Reported gain of SiC SITs over the Past 5 years.

Gate Structure	Gain	Ref.	Comments
RG-SB	8.7 dB at 600 MHz	[16]	packaged devices (1.5 cm parts with total periphery of 16.5 cm) – max. current, 1A/cm - max. blocking voltage, 200V - 47% PAE, 225W output power, and power density of 13.5 W/cm at 600 MHz - cut-off frequency 4 GHz – common-source mode
RG-SB	9.5 dB at 3 GHz	[15]	packaged devices (three unmatched 1 cm devices connected in parallel) – operated at 80V on the drain - 42% PAE, 36 W output power, and 9.5 dB gain at 3 GHz – common-gate mode packaged devices (23 cells connected in parallel with total periphery of 34.5 cm – shown in Fig. 5) – operated at 90V on the drain – power density was 165 kW/in^2 and good linearity observed in class AB operation from output power of 50 to 450 W at 600 MHz – common-source mode
RG-SB	15 dB at 3 GHz	[17]	single devices – drain bias of 40V – 80V resulted in 11.5 dB - 15 dB gain at 3 GHz
RG-SB	9.5 dB at 3-4 GHz	[17]	packaged devices (airbridged parts with total periphery of 3 cm) - 40% PAE, 38 W of output power, power density of 300 KW/cm^2 and 9.5 dB gain at S-band frequencies (3-4 GHz)– power levels up to 120 W have been observed from these S-band SIT packages
P-SB (PN gate)	9dB at 2 GHz	[14]	single device - max. channel current, 700 mA/cm – max. blocking voltage, 250 V
P-SB (PN gate)	7 dB at 1.3 GHz	[14]	packaged devices – Class AB operation - 80-90V on the drain - voltage swing of 200V - 52% drain efficiency, 35W of output power, and power density of 15.5 W/cm
RG-SB	7.7 dB at 1.3 GHz	[18]	Packaged devices (16 parts with 1.5 cm source periphery) - 55% PAE, power density of 16.7 W/cm and power of 400W
RG-SB	7 dB at 4 GHz	[18]	packaged devices (four 1.29 cm airbridged parts) - 30% drain efficiency and 47W of output power at 4 GHz 40% drain efficiency, 78W output power and power density of 15.5W/cm at 2.9 GHz
RG-SB	10 dB at 4 GHz	[19]	packaged devices (total periphery of 1 cm – approximately 200 fingers) – measurements taken on wafer at full channel current – drain bias of 40V - 40% drain efficiency and 16W output power at 1.3 GHz – common-gate mode
RG-B	14 dB at 950 MHz	[20]	packaged devices (total periphery of 5 mm) – 27% PAE, 3W output power at 950 MHz – common-source mode



(a)



(b)

Fig. 6 a) SiC SITs in a 0.4 inch power transistor package. b) Power transfer characteristics showing good linearity in common source, class AB operation. Taken from [13] A.W. Morse, P.M. Esker, R.C. Clarke, C.D. Brandt, R.R. Siergiej, and A.K. Agarwal, "Application of High Power Silicon Carbide Transistors at Radar Frequencies," *IEEE MTT-S Digest*, pp. 677-680, 1996.

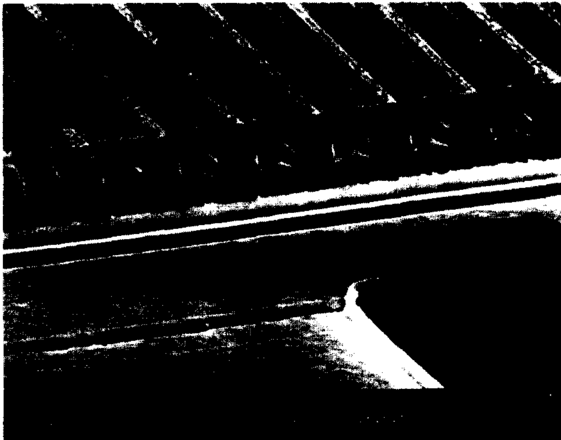


Fig. 7 Microphotograph (top-view) of completed 1.5 cm periphery SiC Static Induction Transistors (SITs). Gate and source bonding tabs can be seen. Taken from [16].

The most challenging aspects of fabricating the SIT revolve around the gate and source regions. Using a recessed gate structure involves the challenge of placing the gate Schottky metal on the sidewalls without shorting to the source in the case of the RG-SB 3structure, or selectively keeping the metal off the sidewall in the RG-B structure [20] which achieved 14 dB gain at 950 MHz in common-source mode. Achieving a self-aligned structure is a key to solving this problem.

5. Conclusions

A cursory review of 4H-SiC SIT's has been given. These transistors have demonstrated excellent output power, linearity, and adequate gain at frequencies from UHF to S-band. Many, but not all, of the S-band results were achieved in common-gate mode to enhance the gain via reduction of the Miller effect, while compromising the bandwidth.

Most results were from recessed gate Schottky contact structures, although 7 dB gain at 1.3 GHz in class AB operation was demonstrated using an implanted, planar PN gate [14]. Remaining issues to be studied further include temperature effects in the device under high power conditions, and how the saturated velocity SCLC mode can be extended. Also, achieving a self-aligned process [20] is key to achieving a manufacturable product.

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