

# A Study of AC-DC PWM Full-Bridge Integrated Converter Topologies

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## ABSTRACT

Two AC-DC PWM full-bridge converters that can shape the input current to improve input power factor while performing dc-dc conversion are investigated in this paper. Both converters are simple in that they are similar to the standard PWM full-bridge converter with a diode rectifier/LC low-pass filter input, and both can operate with a simple method of PWM control. In the paper, the operation of the converters is explained and their steady-state characteristics are discussed. The feasibility of the converters and their ability to meet EN61000-3-2 Class D standards for electrical equipment are shown with results obtained from experimental prototypes. The performance of both converters in terms of dc bus voltage level, input power factor and efficiency is compared and discussed.

**Key Words :** AC-DC PWM full bridge converter, power factor correction

## 1. Introduction

Power converter manufacturers are being pressured by regulatory agencies to implement some form of power factor correction (PFC) in their products. The increasing use of electrical equipment such as computers, telecommunications systems, consumer electronics, etc. by society threatens to increase the amount of harmonic pollution in the ac utility grid, and regulatory agency standards on current harmonic content such as EN61000-3-2 are being enforced to try to reduce the problem. For conventional two-stage ac-dc converters with output isolation where an ac-dc rectifying stage and an isolated dc-dc conversion stage are used, this has meant replacing the traditional passive diode rectifier/LC filter input combination with a boost converter in the rectifying stage.

The boost converter can shape the input line3-2, but an additional switching converter must be current so that it is more sinusoidal and with a harmonic content compliant with agency standards such as EN61000- implemented. and the cost complexity of the overall two-stage converter are therefore increased.

Converters that integrate the PFC and dc-dc conversion functions in a single switching converter have been proposed to try to minimize these disadvantages <sup>[1]-[14]</sup>. Most of this research, however, has focused on low power, "integrated" forward converters, and there has been much less investigation done on higher power full-bridge type converters ( $\geq 500$  W). Of the full-bridge integrated converters that have been previously proposed <sup>[8]-[14]</sup>, most have at least one of the following major drawbacks: (i) They produce an output voltage with a large low frequency (120 Hz) ripple, which limits them to applications where a tightly regulated output voltage is not required. (ii) They do not have an energy storage capacitor across the dc bus, which causes high voltage overshoots and ringing to

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appear across the dc bus unless damped by a lossy snubber. (iii) They do have an energy storage capacitor across the bus, but the voltage across this capacitor is excessive (i.e.  $> 500\text{-}600\text{ V}$ ). (iv) They are complex and require the addition of auxiliary transformers and extra components.

PWM full-bridge converters that can operate with integrated PFC and satisfy the EN61000-3-2 Class D standards for electrical equipment, but without the above disadvantages have been proposed by the authors and studied in detail in [15] and [16]. Both converters are simple in that they are similar to the standard PWM full-bridge converter with a diode rectifier/LC low-pass filter input, and both can operate with a simple method of PWM control. In the paper, the operation of the converters is explained and their steady-state characteristics are discussed. The feasibility of the converters and their ability to meet EN61000-3-2 Class D standards for electrical equipment are shown with results obtained from experimental prototypes. The performance of both converters in terms of dc bus voltage level, input power factor and efficiency is compared and discussed.

## 2. Converter Operation

The two converters, which will henceforth be referred to as Converter A and Converter B in this paper, are shown in Fig. 1 and Fig. 2 respectively. Converter A, is representative of typical integrated forward and full-bridge converters where the number of energy-transfer modes in a single switching cycle is matched by the number of times energy from the input inductor is transferred to the energy storage capacitor. Converter B is a simplified version of Converter A and has the property of having a lower number of times in a switching cycle that energy is transferred from the input inductor to the energy storage capacitor. This is a property that is possible only in full-bridge type integrated converters and not in forward-type integrated converters, and can result in a lower dc bus voltage  $V_{Cb}$  than that found in other integrated converters. The main difference between these converters and the conventional PWM full-bridge converter with a diode rectifier/LC filter input is that the input inductor,  $L_{in}$ , is connected to both bottom converter switches in the case of Converter A and it is connected to a single bottom switch in the case for Converter B. This allows the bottom

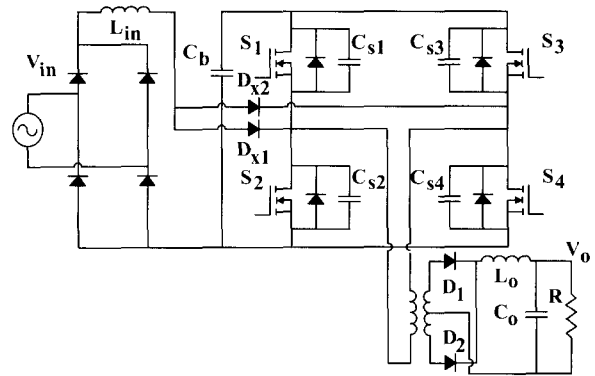


Fig. 1. Integrated PWM full-bridge Converter A

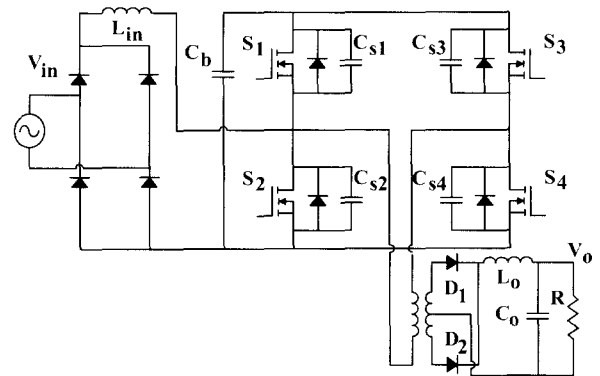


Fig. 2. Integrated PWM full-bridge Converter B

switch(es) to shape the input current while the converter is performing dc-dc conversion in a way that is similar to that of a standard full-bridge converter. In order for this to happen, however, a different PWM technique than the standard phase-shift control technique typically used in a full-bridge converter must be used. In the standard phase-shift PWM technique, the gating signals have the same duration and the control is performed by shifting the gating signals of the switches in one converter leg with respect to those of the other leg. For Converters A and B, the gating signals of the switches in a converter leg are asymmetrical with the bottom switch having a pulse width of  $DT_{sw}/2$  (where  $D$  is the converter duty cycle and  $T_{sw}$  is the switching period) in order to perform the input current shaping.

The converter is in an energy-transfer mode and energy is transferred from the dc bus capacitor on the primary side to the output whenever a pair of diagonally opposed switches are on. It is in a freewheeling mode whenever both bottom switches are off. In the case of Converter A,

energy stored in  $L_{in}$  is transferred to  $C_b$  whenever the converter is in a freewheeling mode. In the case of Converter B, the transfer of energy from  $L_{in}$  to  $C_b$  may occur only after every other freewheeling mode, depending on whether the instantaneous input current is larger or smaller than the transformer primary current.

Converters A and B can operate in any one of several possible combinations of operating modes. The output section of the converter can operate in either the discontinuous conduction mode (DCM) or the continuous conduction mode (CCM). The input section can operate in DCM, CCM, or a semi-continuous conduction mode SCM, which is a combination of DCM and CCM. Regardless of the combination of input and output section modes, both converters pass through several distinct intervals of operation during a single steady-state switching cycle. The operating intervals for Converter A are as follows with the case when the instantaneous input current is greater than the instantaneous transformer primary current being presented first, then the case when the input current is the smaller current.

### 2.1 Input current ( $I_{in}$ ) is greater than the transformer primary current ( $I_p$ )

The primary-side equivalent circuits and the operating waveforms of the converter for this case are given in Figs. 3 and 4 respectively.

#### (a) Interval 1 [ $t_0 - t_1$ ], (Fig 3(a)):

Switches  $S_1$  and  $S_4$  are on at  $t = t_0$ , and the voltage across the transformer primary is equal to the voltage across  $C_b$ ,  $V_{bus}$ . The input current rises as power is being transferred to the load. Its value at  $t_1$  is:

$$I_{in,k}(t) = I_{in,k}(t_0) + \frac{V_{in,rec,k} D_k T_{sw}}{2L_{in}} \quad (1)$$

where,  $I_{in,k}(t_0)$  is the original input current before the start of Interval 1 (this is zero if the input current is discontinuous),  $V_{in,rec,k}$  is the diode bridge rectifier voltage during Interval 1,  $D_k$  is the duty-cycle, and  $T_{sw}$  is the switching period of the full-bridge converter. The current flowing through  $S_1$  is  $I_{p,k}$ , the transformer primary current (the sum of the reflected secondary current and the magnetizing current, assumed here to be negligible) and

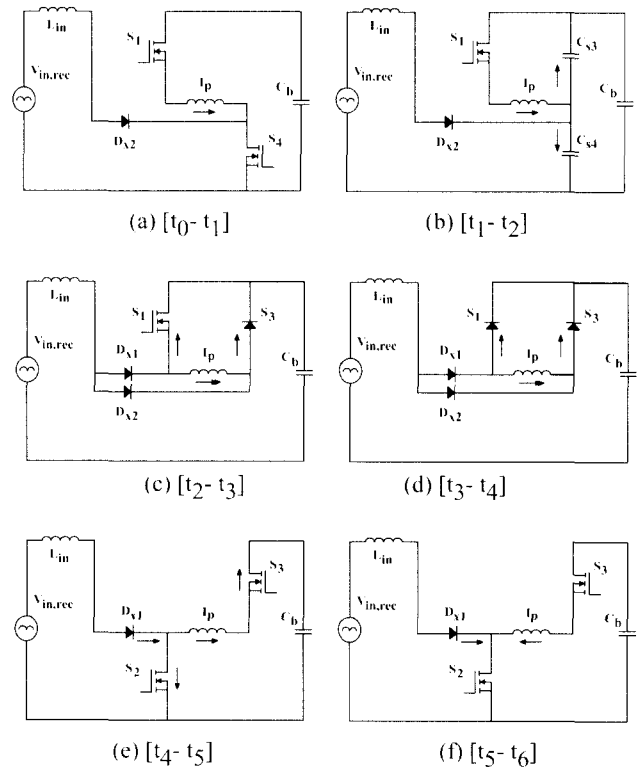


Fig. 3. Operating intervals for a half-switching cycle for Converter A when the instantaneous input current is greater than the instantaneous transformer primary current.

the current flowing through  $S_4$  is

$$I_{S4,k} = I_{in,k} + I_{p,k} \quad (2)$$

#### (b) Interval 2 [ $t_1 - t_2$ ], (Fig. 3(b)):

Switch  $S_4$  is turned off at  $t = t_1$  and capacitors  $C_{s3}$  and  $C_{s4}$  discharge to zero and charge to  $V_{bus}$  respectively. Energy from the input inductor  $L_{in}$ , the output inductor  $L_o$  and the transformer leakage inductance  $L_{lk}$  is available for this task.

#### (c) Interval 3 [ $t_2 - t_3$ ], (Fig. 3(c)):

The converter is in a freewheeling mode as the voltage across the transformer primary is zero. The current flowing through  $D_{x1}$  is  $I_{p,k}$ . The remaining current,  $I_{in,k} - I_{p,k}$ , is divided between  $S_1$  and  $D_{x2}$ , with the voltage drop across  $S_1$  clamped by  $D_{x2}$ . The current flowing into energy-storage capacitor  $C_b$  is

$$I_{Cb} = I_{S1,k} + I_{Ds3,k} = I_{in,k} \quad (3)$$

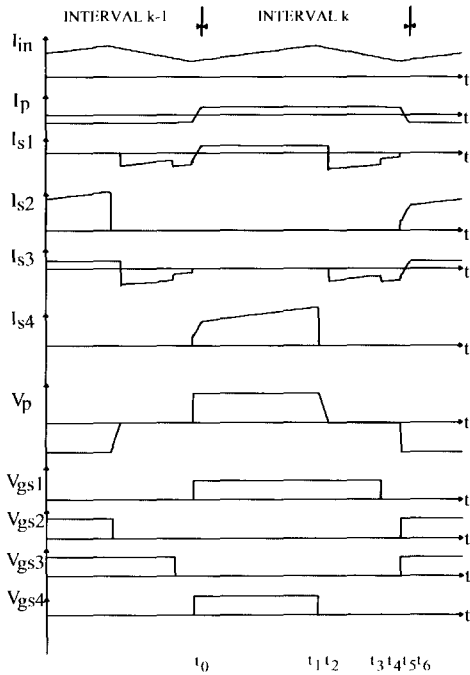


Fig. 4. Typical waveforms for Converter A when the instantaneous input current is greater than the instantaneous transformer primary current.

The input current falls because the voltage across the input inductor is equal to the difference between the input voltage and  $V_{bus}$  (which is larger than the input voltage). The input current at the end of Interval 3,  $t_3$ , is:

$$I_{in,k}(t_3) = I_{in,k}(t_2) - \frac{(V_{bus} - V_{in,rec,k})d_k T_s}{2L_{in}} \quad (4)$$

where,  $I_{in,k}(t_2)$  is the input current value at the beginning of Interval 3 and  $d_k T_s$  is the duration of the interval.  $I_{in,k} = 0$  and  $D_k + d_k < 1$  when the input current is discontinuous,

**(d) Interval 4 [ $t_3 - t_4$ ], (Fig. 3(d)):**

Switch  $S_1$  is turned off at  $t = t_3$ . The converter is still in a freewheeling mode, but the distribution of the current between the anti-parallel diode of  $S_1$  and  $D_{x2}$  is different.

**(e) Interval 5 [ $t_4 - t_5$ ], (Fig. 3(e)):**

Switch  $S_2$  is turned on at  $t = t_4$ , and the current that was flowing through  $S_1$  and  $D_{x2}$  now flows through this switch. The current flowing through  $S_2$  during this interval is

$$I_{S2,k} = I_{in,k} - (I_{p,k} - \frac{V_{bus}(t-t_4)}{L_{lk}}) \quad (5)$$

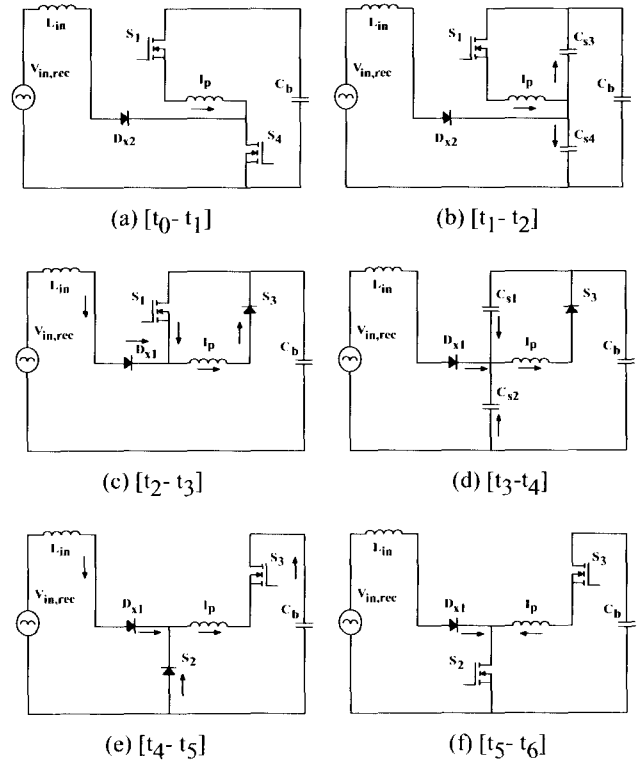


Fig. 5. Operating intervals for a half-switching cycle for Converter A when the instantaneous input current is less than the instantaneous transformer primary current.

and the current flowing through the anti-parallel diode of  $S_3$  decreases, reaching zero at  $t = t_5$ .

**(f) Interval 6 [ $t_5 - t_6$ ], (Fig. 3(f)):**

At  $t = t_5$ , the transformer primary current begins to flow in the opposite direction and continues to rise until  $t = t_6$ . After  $t = t_6$ , the converter is in the same state as it was after  $t = t_0$ , except that switches  $S_2$  and  $S_3$  are on instead of  $S_1$  and  $S_4$ .

## 2.2 Input current ( $I_{in}$ ) is less than the transformer primary current ( $I_p$ )

The primary-side equivalent circuits and the operating waveforms of the converter for this case are given in Fig. 5 and Fig. 6 respectively. The operating intervals during a half switching cycle when the instantaneous input current,  $I_{in,k}$ , is less than the transformer primary current,  $I_{p,k}$ , are very similar to those when  $I_{in,k} > I_{p,k}$  with one exception. The flow of current in the full-bridge switches when the converter is in a freewheeling mode is different. During Intervals 3-5 (Figs. 5(c)-(e)), the difference between

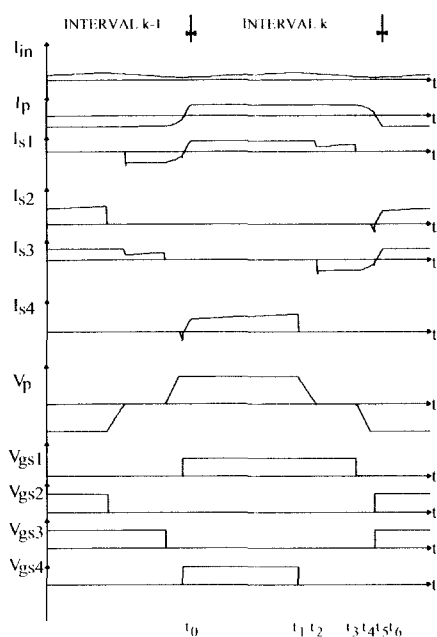


Fig. 6. Typical waveforms for Converter A when the instantaneous input current is greater than the instantaneous transformer primary current

the transformer primary current and the input current flows through  $S_1$  then discharges and charges  $C_{s1}$  and  $C_{s2}$  respectively after  $S_1$  is turned off. This current eventually flows through the anti-parallel diode of  $S_2$ . Regardless of how current flows in the full-bridge during a freewheeling mode, the flow of input current through the converter remains the same when  $I_{in,k} >$  or  $< I_{p,k}$ .

### 2.3 Operating intervals for Converter B

The operating intervals of Converter B are a combination of those of Converter A for one leg, and those for a conventional PWM full-bridge converter for the other because Converter B has input inductor  $L_{in}$  attached to only one of its legs. These intervals will therefore be not be discussed in detail except to explain the circuit operation during the particular intervals shown in Fig. 7. In Fig. 7(a), the converter is shown to be operating with switches  $S_2$  and  $S_3$  on. In this case, the converter is in an energy-transfer mode as the dc bus voltage is placed across the transformer primary and energy from capacitor  $C_b$  is transfer to the output. While this is occurring, the full rectified input voltage is placed across  $L_{in}$ , and the input current will rise. In Fig. 7(b) the converter is shown to operate with switches  $S_1$  and  $S_4$  on.

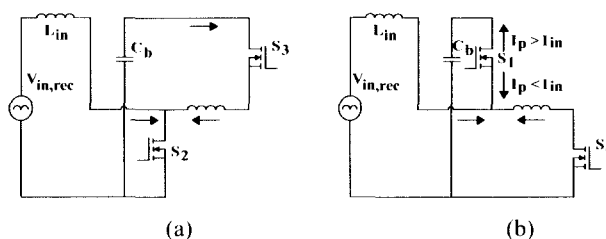


Fig. 7. Energy transfer mode operating intervals for Converter B

This is also an energy-transfer mode, but the net amount of energy transfer is dependent on whether the instantaneous input current  $I_{in,k}$  is greater or less than the instantaneous transformer primary current  $I_{p,k}$ . If  $I_{in,k}$  is greater than  $I_{p,k}$ , then the difference between the two current will flow into capacitor  $C_b$ . If  $I_{in,k}$  is less than  $I_{p,k}$  then the difference between the two current will flow out of  $C_b$ . If the  $I_{in,k}$  is zero, which may be the case if the input current is discontinuous, then the converter operates in the same manner as a standard PWM full-bridge converter.

## 3. Steady-State Characteristics

An analysis of the characteristics of Converters A and B was performed in [15] and [16]. The key parameter that was derived in both cases was the dc bus/storage-capacitor voltage  $V_{Cb}$  because it is only when this is determined that the values for the other parameters can be determined. Special efforts have to be made to determine  $V_{Cb}$  because is not solely regulated by an independent ac-dc boost PFC stage like a conventional two-stage converter, and therefore cannot be kept constant. This voltage was derived by noting that an energy equilibrium must exist for storage-capacitor  $C_b$  when the converter is in steady-state operation. The energy pumped into the capacitor from the input section must be equal to the energy that  $C_b$  provides to the output, so that the net dc current flowing in and out of  $C_b$  must be zero during a half-line cycle.

From the analysis of the converters, the following general characteristics were noted.

- 1) When output current  $I_o$  and input current  $I_{in}$  are both discontinuous,  $V_{Cb}$  remains constant regardless of what the load is. It is dependent on the ratio of  $L_{in}/L_o$ , and on the transformer turns ratio  $N$ .
- 2) When  $I_o$  and  $I_{in}$  are both continuous,  $V_{Cb}$  again remains almost constant regardless of what the load is.

It is dependent mainly on the transformer turns ratio  $N$ , and slightly on the ratio of  $L_{in}/L_o$ . This is particularly true if  $I_{in}$  and  $I_o$  are deep in continuous current mode CCM.

- 3) The voltage across capacitor  $C_b$ ,  $V_{Cb}$  will increase when the load decreases if  $I_{in}$  is discontinuous and output current  $I_o$  is continuous.
- 4)  $V_{Cb}$  decreases as  $L_{in}$  is increased and the other component values are kept constant, especially when  $I_{in}$  is fully discontinuous.
- 5)  $V_{Cb}$  decreases as  $L_o$  is decreased and the other component values are kept constant, especially when  $I_{in}$  is fully discontinuous.
- 6)  $V_{Cb}$  decreases as transformer turns ratio  $N = N_1/N_2$  is decreased and the other component values are kept constant.

Several of these properties can be seen in the graph shown in Fig. 8, which is a graph of dc bus voltage  $V_{Cb}$  vs. output power for various combinations of transformer turns ratio  $N$ , input inductor  $L_{in}$ , and output inductor  $L_o$  for Converter B. For example, it can be seen that when  $L_o = 20 \mu\text{H}$  and  $L_{in} = 160 \mu\text{H}$  and  $N$  is changed from 2.5 to 3.5, the dc bus voltage will in fact be increased. Also as an example, it can also be seen that the curve for  $N = 2.5$ ,  $L_o = 20 \mu\text{H}$  and  $L_{in} = 50 \mu\text{H}$  is more constant under light load conditions than the other curves due to the fact that  $L_{in}$  is smaller and both input and output current are in discontinuous current mode (DCM).

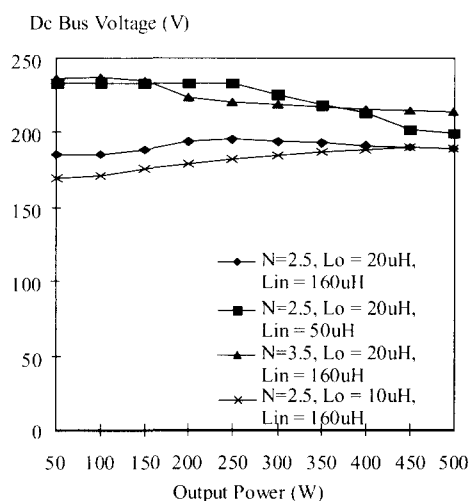


Fig. 8. Dc bus voltage vs output power for  $V_{in} = 100 \text{ Vrms}$  and  $V_o = 48 \text{ V}$  for Converter B

## 4. Experimental Results

In order to compare the performance of Converters A and B, an experimental prototype was built to operate under the following conditions

Input voltage  $V_{in} = 85 - 265 \text{ Vrms}$

Output voltage  $V_o = 48 \text{ V}$

Maximum output power  $P_o = 500 \text{ W}$

Maximum dc bus voltage  $V_{Cb} < 450 \text{ V}$

Switching frequency  $F_{sw} = 50 \text{ kHz}$

Three different sets of results were obtained: The first set was for the case of Converter A designed to operate across the full input voltage range with  $L_{in} = 203 \mu\text{H}$  and  $L_o = 4.5 \mu\text{H}$  (Case 1).

The second set was for the case of Converter B designed to operate across the full input voltage range with  $L_{in} = 140 \mu\text{H}$  and  $L_o = 32 \mu\text{H}$  (Case 2).

The third case was for the case of Converter A designed to operate with the same set of values as those used for Case 2 except with the input voltage range restricted to  $V_{in} = 85 - 132 \text{ Vrms}$  (Case 3). A common value of transformer turns ratio of  $N = 2.5$  was used for all three cases in order to facilitate the investigation.

Figs. 9(a) and (b) show the input current waveforms for Converter B in Case 2 when it is operating with  $P_o = 500 \text{ W}$  and with  $V_{in} = 230 \text{ Vrms}$  and  $100 \text{ Vrms}$  respectively. The input current waveforms for the other two cases are very similar.

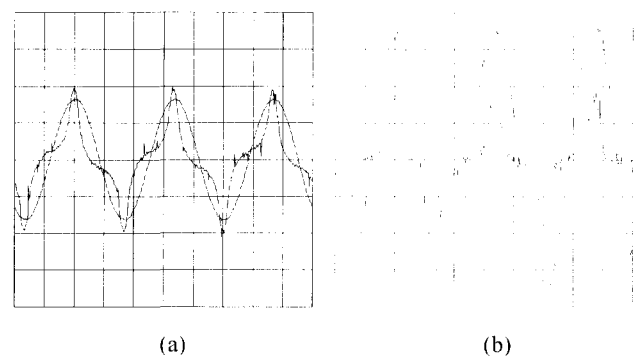


Fig. 9. Input voltage and current waveforms for Converter B operating at  $P_o = 500 \text{ W}$ ; (a)  $V_{in} = 230 \text{ Vrms}$ , scale: V: 200 V/div., I: 4 A/div., t: 5ms/div., (b)  $V_{in} = 100 \text{ Vrms}$ , scale: V: 40 V/div., I: 10 A/div., t: 5ms/div.

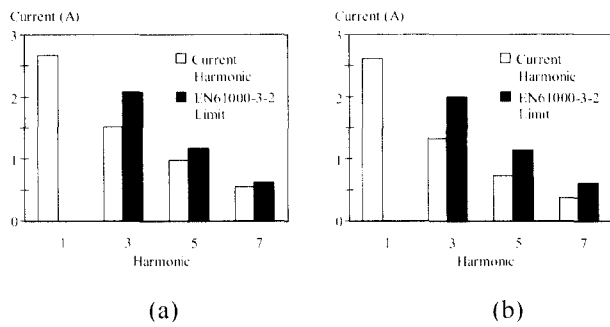


Fig. 10. Input current harmonic content at  $V_{in} = 230$  Vrms and  $P_o = 500$  W; (a) Case 1 (b) Case 2

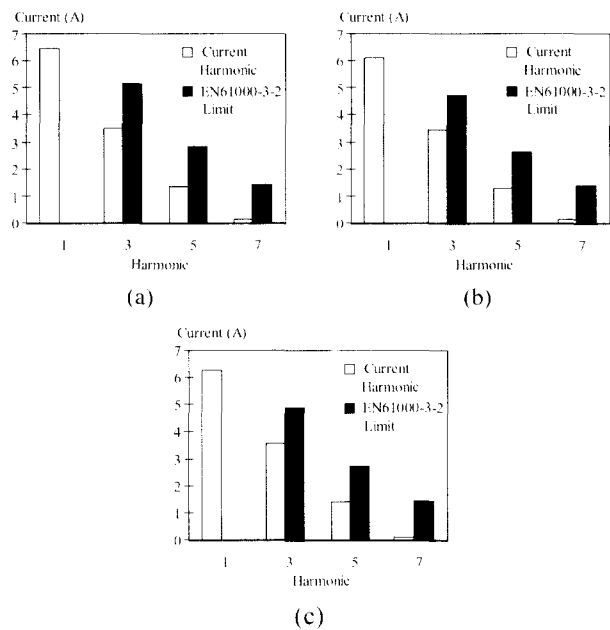


Fig. 11. Input current harmonic content at  $V_{in} = 230$  Vrms and  $P_o = 500$  W; (a) Case 1 (b) Case 2 (c) Case 3

Figs. 10 and 11 show the worst-case input current harmonic content for  $V_{in} = 230$  Vrms and 100 Vrms for all three cases. This will occur under full-load conditions at  $P_o = 500$  W for all three cases. Fig 10 shows the harmonic content for Cases 1 and 2 when  $V_{in} = 230$  Vrms and Fig. 11 shows the harmonic content for Cases 1, 2, and 3 when  $V_{in} = 100$  Vrms. Although the EN61000-3-2 standard for Class D electrical equipment is valid up to an input power of 600 W (after which Class A standards apply), and the input power in some of the cases exceeded the 600 W level, the Class D standard was used since the maximum input power is close to the 600 W level and it is more stringent than the Class A. Since the Class D limits

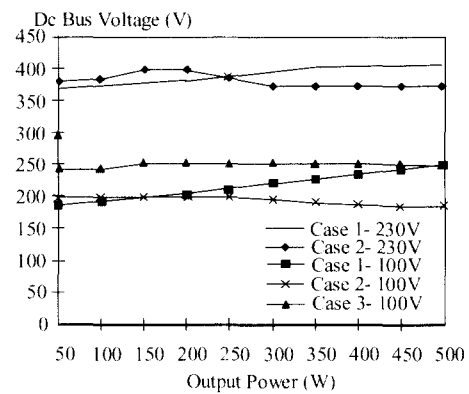


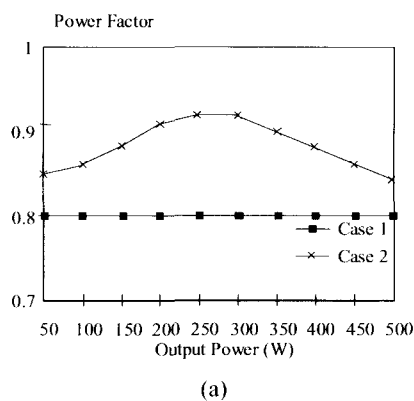
Fig. 12. Experimental dc bus voltage vs. output power

are satisfied for the worst-case current in all three cases under investigation, then so too will the limits be met under lighter load conditions.

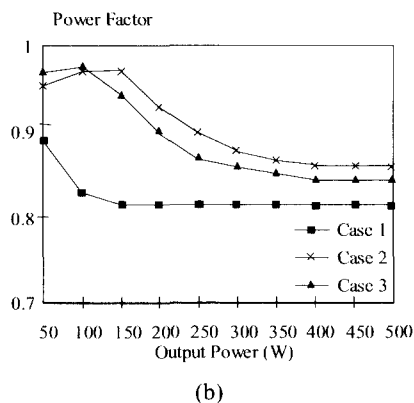
Figs. 12, 13, and 14 show graphs of dc bus voltage  $V_{Cb}$ , input power factor, and converter efficiency vs. load for various values of  $V_{in}$ , ranging from 100 Vrms to 230 Vrms (which was the maximum input voltage available to investigate Cases 1 and 2). It can be seen that the dc bus voltage can be kept at a maximum of about 400 V with a 230 V input (and can be kept at below 450 V for a 265 V input), that the input power factor can range from approximately 0.8 to 0.95, and that a maximum converter efficiency of approximately 85% can be achieved.

The characteristics of Converter A and B operating in the three cases described above and somewhat different than those found in a standard two-stage converter system with a boost converter front end supplying power to a full-bridge dc-dc converter. These differences come from the fact that the dc bus voltage in an integrated converter is not constant since there is no independent means of controlling this voltage as there is in a two-stage converter. The dc bus voltage will vary depending on operating condition.

When looking at Figs. 12 –14 and comparing all three cases, it can be seen that Converter B (Case 2) generally has the better performance. Most of the improvement in performance is a result of the fact that Converter B can operate with a lower dc bus voltage than Converter A because energy from the input inductor is pumped less often into the energy storage capacitor for the same operating point. In order to maintain the dc bus voltage of Converter A at a level less than 450 V for a high line



(a)

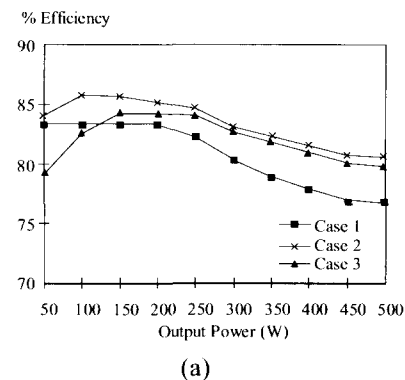


(b)

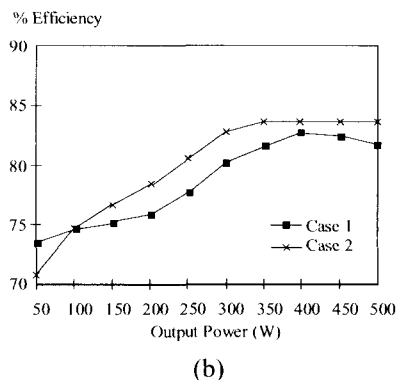
Fig. 13. Experimental input power factor vs. output power; (a) input voltage  $V_{in} = 230$  Vrms, (b) input voltage  $V_{in} = 100$  Vrms

input, the output inductor has had to have been made fairly small to produce a highly discontinuous output current. The output current is much more continuous for Converter B.

Converter B has a higher efficiency than Converter A operating both in Case 1 and in Case 3 mainly because it can be more easily designed to have a lower dc bus voltage than Converter A. Since Converters A and B were implemented experimentally without soft-switching, a lower dc bus voltage would result in less voltage being placed across the converter switches and therefore fewer switching losses. This phenomenon also explains the fact that both Converters A and B exhibit a higher light load efficiency at low line input voltage when the dc bus voltage is lower than at high line input voltage. Converter B can also operate with a higher input power factor than Converter A when it is operating in Case 1 or in Case 3. In the case of Case 1, Converter A is operating with a larger input inductor that Converter B is in Case 2 ( $L_{in} = 203 \mu\text{H}$  vs  $L_{in} = 140 \mu\text{H}$ ).



(a)



(b)

Fig. 14. Experimental efficiency vs. output power; (a) input voltage  $V_{in} = 230$  Vrms, (b) input voltage  $V_{in} = 100$  Vrms

Since Converter B is operating with a smaller input inductor, its input current is much more likely to follow a sinusoidal envelope than is Converter A; therefore it will operate with a higher input power factor. When Converter A is operating as it is in Case 3 with the same input inductor as Converter B in Case 2, then Converter B will operate with a higher input power factor for the following reason. Since Converter B can be made to operate with a lower dc bus voltage for a particular operating point, it will operate with a higher duty cycle than Converter A will for the same duty cycle  $D$ . If output voltage  $V_o = V_{Cb}D/N$  then  $D$  will be higher for Converter B than it will be for Converter A for the same  $V_o$ . Since the shape of the input current for an integrated converter is determined by the converter duty-cycle, operating with a larger duty-cycle means that the input current will start to rise sooner in the line cycle, making its overall shape more spread out and therefore more sinusoidal and/or making its fundamental component more in phase with the input voltage. The latter situation can be seen in Figs. 10, 11 and



13 for the graphs of the various cases when  $P_O = 500$  W where there is little variation in input harmonic content among the various cases but there is variation in power factor.

## 5. Conclusion

Two PWM full-bridge converters that simultaneously perform input power factor correction and dc-dc conversion were examined in this paper. Both converters have a simple topology as they are very similar to the standard PWM full-bridge with a diode rectifier/LC filter front-end except for some slight modifications. The first converter, Converter A, is representative of typical integrated forward and full-bridge converters where the number of energy-transfer modes in a single switching cycle is matched by the number of times energy from the input inductor is transferred to the energy storage capacitor. The second converter, Converter B, is a simplified version of Converter A and has the property of having a lower number of times in a switching cycle that energy is transferred from the input inductor to the energy storage capacitor.

In the paper, the operation of both converters was explained and their general steady-state characteristics were discussed. Both converters were implemented with an experimental prototype. It was shown that both converters are feasible, and that both can be designed to meet EN61000-3-2 Class D standards for electrical equipment while maintaining a dc voltage of less than 450 V, an input power factor ranging from 0.8 to 0.95, and a maximum efficiency of approximately 85%. Converter B was found to have a superior overall performance than Converter A, mainly because of its ability to operate with lower dc bus voltages for the same operating points.

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