A 1.5 V High-Gain High-Frequency CMOS Complementary Operational Amplifier

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In this paper, a 1.5 V high-gain high-frequency CMOS complementary operational amplifier is presented. The input stage of op-amp is designed for supporting the constant transconductance on the input stage by consisting of the parallel-connected rail-to-rail complementary differential pairs. And consisting of the class-AB rail-to-rail output stage using the concept of elementary shunt stage and the grounded-gate cascode compensation technique for improving the low PSRR which was a disadvantage in the general CMOS complementary input stage, the load dependence of open loop gain and the stability of op-amp on the output load are improved, and the high-gain high-frequency operation can be achieved. The designed op-amp operates perfectly on the complementary mode with the 180° phase conversion for a 1.5 V supply voltage, and shows the DC open loop gain of 84 dB, the phase margin of 65°, and the unity gain frequency of 20 ㎒. In addition, the amplifier shows the 0.1 % settling time of 0.179 ㎲ for the positive step and 0.154 ㎲ for the negative step on the 100 ㎷ small-signal step, respectively, and shows the total power dissipation of 8.93 ㎽.

Keywords : CMOS, complementary, operational amplifier, Class-AB

1. INTRODUCTION

Recently, due to the wide use of portable electronic equipments, the requirement for low-power, low-voltage analog IC's has increased in all areas of application. This requirement has become increasingly important for the increased density of integration and the decreased supply voltages in digital and/or mixed-mode integrated circuits [1-3].

In most mixed-mode circuits, the analog circuitry takes only a small portion of a chip area. However, these circuits require considerable design cost because a designer needs to consider varied objectives and constraints in a design process [4].

In particular, as the density of integration is increased, many literatures for reducing the power dissipation on the chip have been presented. As the result, recently presented integrated circuits are designed with supply voltages of 1.5 V or even less. With such low voltages, traditional CMOS circuit solutions can be adopted only if a low threshold process is available. To overcome these design limitations, new circuit solutions with a reduced power supply has been designed [5-10].

One of the most important basic building blocks in analog and mixed-mode VLSI circuits is the operational amplifier of which numerous implementations have been reported [4-14]. And the design specifications of a desirable CMOS VLSI amplifier include the high DC gain, the high unity gain frequency, the fast settling time over a variety of low load capacitor values, the suitability for fabrication in a short-channel digital CMOS process, the capability of rail-to-rail input and output stage to achieve the highest possible dynamic range, the nominal power dissipation, and the small area [12]. However, the realization of a CMOS operational amplifier that combines the high DC gain with the high unity gain frequency has been a difficult problem. The high gain requirement leads to multistage designs with long-channel devices biased at low current levels, whereas the high unity gain frequency requirement calls for a single-stage design with short-channel devices biased at high bias current levels. One method of

overcoming this trade-off includes the use of parallel-connected complementary rail-to-rail differential pairs in the rail-to-rail input stage. It consists in keeping at least one of the input pairs adequately biased for any value of the input common-mode voltage. Thus, the constant transconductance of the input stage is achieved. This makes the unity gain frequency maintain over the full common-mode input range.

In general, most of the previous operational amplifier used common-source type output stages. The main disadvantage of this type of output stage is that its gain is heavily dependent on the output load, and low resistance loads can easily cause gain reductions of the order of 40 dB. An elementary shunt stage can be an alternative for the common-source type output stage which has the advantages of much less dependence on the output load and the secondary pole location at a relatively high frequency [7].

In this paper, a new high-gain high-frequency operational amplifier that works with a 1.5 V supply voltage is presented. It adopts a parallel-connected complementary differential pairs in the input stage and includes a class-AB output stage which is designed using the concept of the elementary shunt stage. The operational amplifier is implemented in a standard 0.8 ㎛ CMOS process, and simulation results are presented.

2. INPUT STAGE WITH COMPLEMENTARY DIFFERENTIAL PAIRS

The input stage with the parallel-connected rail-to-rail complementary differential pairs is shown in Fig. 1. The PMOS differential input pair is made up of the PMOS source-coupled pair M1-M2, the folded current mirror M9-M10, and the bias current source M5. The NMOS differential input pair is made up of the NMOS source-coupled pair M3-M4, the folded current mirror M7-M8, and the bias current source M6. These two differential input pairs are designed with the symmetrical topology which ensures high common-mode rejection ratio.

The proposed rail-to-rail complementary differential pairs operated in parallel allow common-mode input signals to vary from negative to positive supply rails. When the common-mode input signal is near one of the rails, only one of the pairs turns on; the other is cut off. So, the input swing is improved and the trans-conductance of input stage maintains constant. From this proposed complementary input stage, the output current Io for this amplifier is given by;

$$Io = (I_3\text{-}I_4) + (I_2\text{-}I_1) \quad (1)$$

where the subscript represents the drain current Id through the respective transistors.

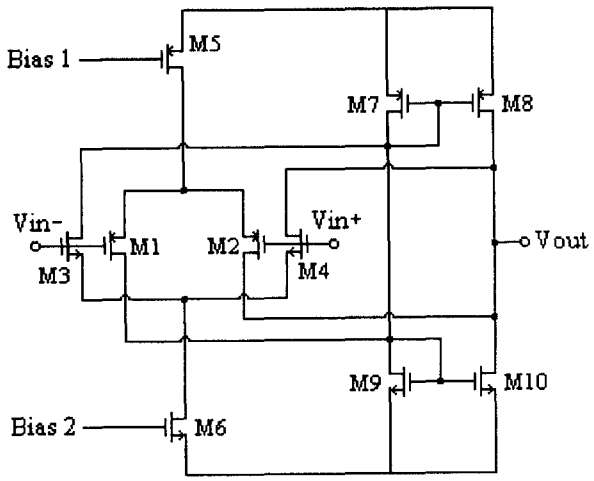

Fig. 1. Input stage with parallel-connected complementary differential pairs.

3. CLASS-AB OUTPUT STAGE AND FREQUENCY COMPENSATION

The main disadvantage of common-source type output stages is that its gain is heavily dependent on the output load. As an alternative for this type output stage, an elementary shunt stage was proposed [7]. Fig. 2 shows the concept of output stage configuration with an elementary shunt stage, in which the shunt stage is driven by a transconductor block with small-signal transconductance Gm. Then, the output stage gain is obtained to the next eq.(2).

$$\frac{Vout}{Vin} = -GmR_C\frac{1 - 1/g_mR_C}{1 + 1/g_mZ_L} \quad (2)$$

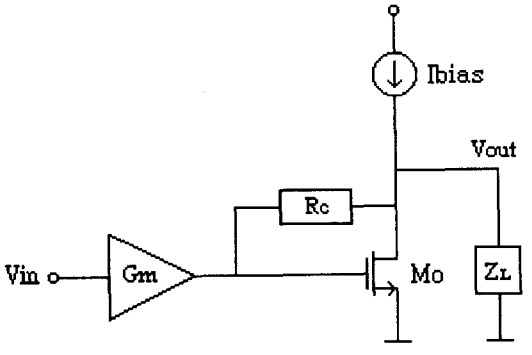

Fig. 2. Output stage configuration with elementary shunt stage.

where g_m is the transconductance of transistor Mo and Rc is the shunt resistance. Typically, both the shunt resistance Rc and the load impedance Z_L are much larger than $1/g_m$. In this case, eq.(2) can be approximated to;

$$\frac{Vout}{Vin} \approx -GmR_C \quad (3)$$

This eq.(3) shows that the output stage gain can be obtained by the product of the transconductance Gm of the transconductor block and the shunt resistance Rc.

Using the concept of output stage configuration with an elementary shunt stage of Fig. 2, the rail-to-rail class-AB output stage for the operational amplifier operated with a 1.5 V supply voltage is proposed in Fig. 3. In this Fig. 3, the transconductor has been realized with transistors M13, M14, and M17, and its transconductance Gm is determined by the g_m of M13 and the current ratio of the current mirror M14 and M17. The PMOS output transistor M19 is directly driven by the output of input stage and the class-AB operation now becomes possible.

And the transistors M15-M17 consist of the current conversion circuit to provide the bias current of the output stage. This circuit can be implemented using the grounded-gate cascode compensation technique with the compensation capacitor Cc [13]. This compensation technique is useful for the frequency compensation and known to improve the power supply rejection ratio. Because the parallel-connected complementary input stage shown in Fig. 1 may be somewhat weak configuration for the power supply rejection ratio, the PSRR of the proposed operational amplifier can be improved with the grounded-gate cascode compensation technique in this stage.

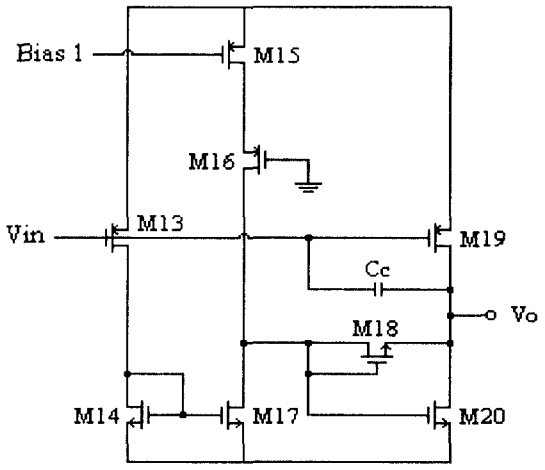

Fig. 3. Proposed Class-AB rail-to rail Output stage.

The shunt resistance Rc can be implemented with the diode-connected transistor M18, which realizes the high resistance on a single transistor size.

4. IMPLEMENTATION OF OVERALL OPERATIONAL AMPLIFIER

The overall schematic of the designed operational amplifier is shown in Fig. 4, and the small-signal equivalent circuit is shown in Fig. 5, respectively. The bias circuit for driving this amplifier consists of transistors M11-M12 and a current source Ibias.

From the small-signal equivalent circuit of Fig. 5, the open-loop gain of the overall amplifier is obtained to;

$$A = \frac{g_{m1}R_1GmR_C}{1+s[C_1R_1+(C_C+C_L)/g_{m20}+C_C R_1GmR_C]+s^2[C_1R_1(C_C+C_L)/g_{m20}]} \quad (4)$$

where it is assumed that R_{20} is much larger than $1/g_{m20}$. Then, the two poles of amplifier are driven to eqs.(5) and (6), approximately. These two poles are real and locate at frequencies far from each other.

$$Sp_1 = -\frac{1}{C_1R_1 + (C_C+C_L)/g_{m20} + C_CR_1GmR_C} \quad (5)$$

$$Sp_2 = -\frac{C_1R_1g_{m20} + (C_C+C_L) + C_CR_1GmR_Cg_{m20}}{C_1R_1(C_C+C_L)} \quad (6)$$

If $1/C_1R_1$ is small and $C_C \approx C_1 << C_L$, the secondary pole of eq.(6) may be approximated to

$$Sp_2 \approx -(GmR_C+1)\frac{g_{m20}}{C_L} \quad (7)$$

It should be noted that the secondary pole of eq.(7) locates at much higher frequency by a factor of (GmR_C+1) than that, $-g_m/C_L$, of the classical two-stage CMOS operational amplifiers. So, an improvement of the load handling capability by a factor of (GmR_C+1) is in principle possible.

The DC gain of the designed input stage is of the order of 50 dB and the output stage has a gain about 30 dB, which decreases by only 16 dB when the load resistance connected to its output is reduced from 1 MΩ to 1 kΩ.

5. SIMULATION AND RESULTS

The overall amplifier of Fig. 4 was designed and

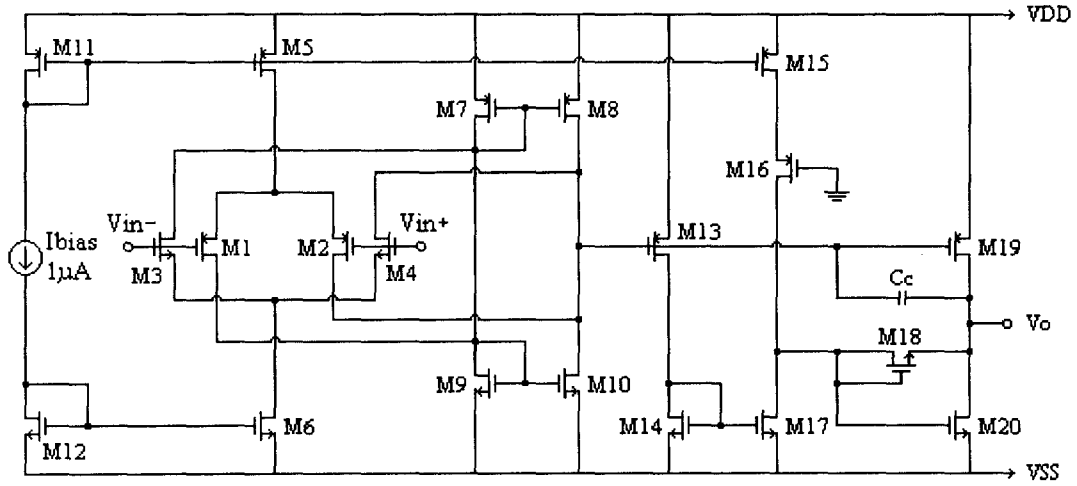

Fig. 4. Overall schematic of the designed Op-Amp.

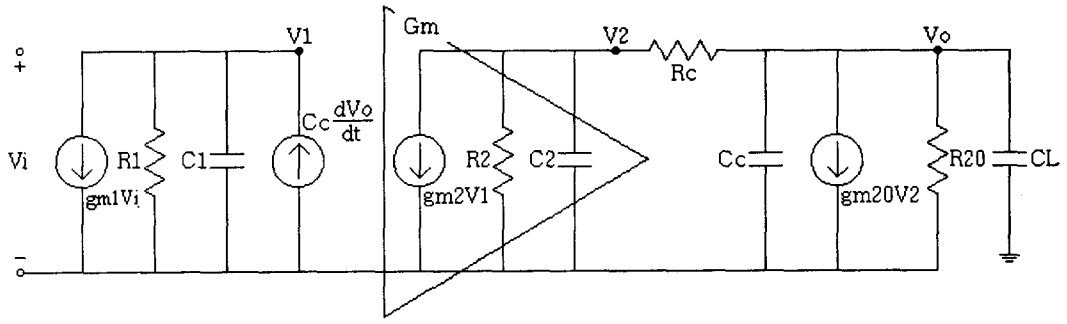

Fig. 5. Small-signal equivalent circuit.

implemented in a standard 0.8 ㎛ CMOS process and simulated with the SPICE. After hand calculations using design equations, the component values of devices were determined with the fine tuning, and summarized in Table 1. And the performance of designed amplifier is shown in Table 2. All results were obtained with a 1.5 V supply voltage and an Ibias of 1 ㎂.

Fig. 6 shows the output current vs the output voltage characteristics of the proposed operational amplifier and illustrates the push-pull takeover behavior of the class-AB output stage. And it shows that the output stage of designed amplifier can be operated at supply voltages as low as 1.5V. But we can see the small output voltage shift for zero output current, which results from the mismatch of transistors.

Fig. 7 shows the frequency responses of the operational amplifier for a load of 1 ㏁ resistance in parallel with 10 ㎊ capacitance when a) Vin+ = ac +1 V, b) Vin+ = ac −1 V, c) Vin− = ac +1 V, d) Vin− = ac −1 V, respectively. This Fig. 7 shows that the designed operational amplifier operates perfectly on the complementary mode with the 180° phase conversion for a 1.5 V supply voltage. And the operational amplifier exhibits the DC open loop gain of 84 dB, the phase margin of 65°, and the unity gain frequency of 20 ㎒. This is the superior performance than those of previously published works [12,14], etc.

Fig. 8 shows the 100 ㎷ small-signal step response of the amplifier for a pure capacitive load of 10 ㎊. This Fig. 8 exhibits the 0.1 % settling time of 0.179 ㎲ for the positive step and 0.154 ㎲ for the negative step, respectively, and shows the full swing of output for the input voltage.

Table 1. Component Values (W/L, μm).

Component	Value	Component	Value
M1	60/2	M12	10/4
M2	60/2	M13	60/2
M3	60/2	M14	80/1
M4	60/2	M15	38/1
M5	64/1	M16	16/1
M6	64/1	M17	8/1
M7	10/4	M18	10/1
M8	10/4	M19	240/1
M9	10/4	M29	24/1
M10	10/4	Cc	4.5 pF
M11	10/4	Ibias	1 μA

Table 2. Performance of Designed Op-Amp.

Supply voltage	1.5 V
DC open loop gain	84 dB for 1 MΩ || 10 pF 68 dB for 1 kΩ || 10 pF
Unity gain frequency	20.3 MHz for 1 MΩ || 10 pF 17.5 MHz for 1 kΩ || 10 pF
Phase Margin	65° for 1 MΩ || 10 pF 70° for 1 kΩ || 10 pF
Slew rate (for 1 V step,1 kΩ || 10 pF)	1.3 V/μs for positive 2.4 V/μs for negative
0.1 % settling time (for 100 mV step, 10 pF)	0.179 μs for positive 0.154 μs for negative
CMRR	62 dB at 1 kHz 58.5 dB at 1 MHz
PSRR(Vdd)	69 dB at 1 kHz
PSRR(Vss)	66 dB at 1 kHz
Offset voltage	50.8 μV
Total power dissipation	8.93 mW

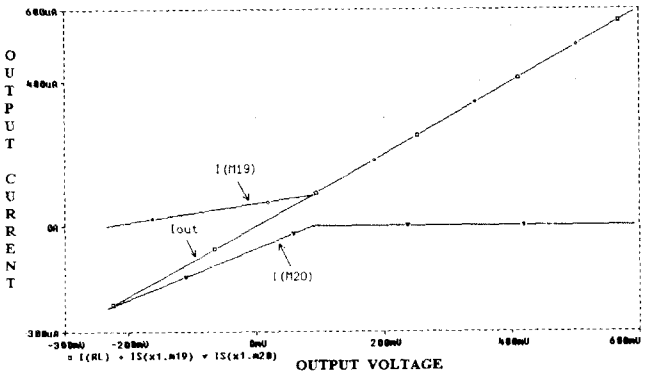

Fig. 6. Output current vs output voltage.
(R_L = 1 kΩ load)

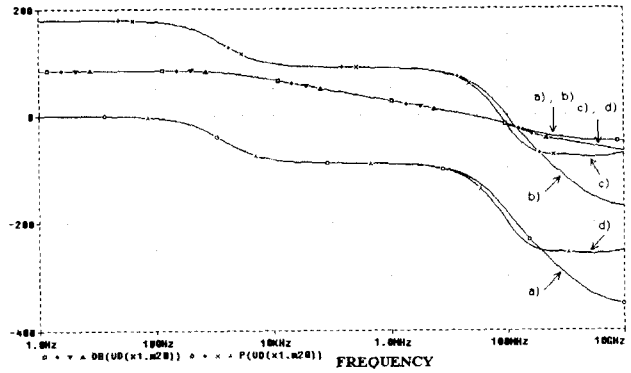

Fig. 7. Frequency response. (1 MΩ || 10 pF load)
a) for Vin+ = ac +1 V b) for Vin+ = ac -1 V
c) for Vin– = ac +1 V d) for Vin– = ac -1 V

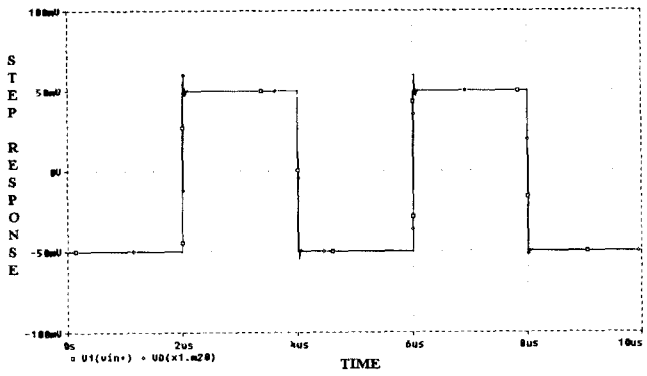

Fig. 8. Small-signal step response.
(100 mV step, 10 pF load)

6. CONCLUSIONS

A 1.5 V high-gain high-frequency CMOS complementary operational amplifier has been presented with the class-AB rail-to-rail output stage. The concept of elementary shunt stage was used in the output stage to overcome the heavy dependence on the output load, and the grounded-gate cascode compensation technique was applied for improving the low PSRR which was a disadvantage in the general CMOS complementary input stage. Using the concept of elementary shunt stage and the grounded-gate cascode compensation technique, the load dependence of open loop gain and the stability of the operational amplifier were improved, and the high-gain high-frequency operation could be achieved. The implemented operational amplifier exhibits the good performance with a 1.5 V supply voltage.

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