A SDR/DDR 4Gb DRAM with 0.11μm DRAM Technology

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Abstract— A 1.8V 650 mm^2 4Gb DRAM having 0.10 μm^2 cell size has been successfully developed using 0.11 μm DRAM technology. Considering manufactur-ability, we have focused on developing patterning technology using KrF lithography that makes 0.11 μm DRAM technology possible. Furthermore, we developed novel DRAM technologies, which will have strong influence on the future DRAM integration. These are novel oxide gap-filling, W-bit line with stud contact for borderless metal contact, line-type storage node self-aligned contact (SAC), mechanically stable metal-insulator-silicon (MIS) capacitor and CVD Al process for metal inter-connections. In addition, 80 nm array transistor and sub-80 nm memory cell contact are also developed for high functional yield as well as chip performance. Many issues which large sized chip often faces are solved by novel design approaches such as skew minimizing technique, gain control pre-sensing scheme and bit line calibration scheme.

Index Terms— DRAM, Process integration, KrF lithography, MIS Capacitor, self-aligned contact.

I. INTRODUCTION

A DRAM technology with 0.11 μm feature size (pitch=0.22 μm) was successfully developed for the first time for 4Gb DRAM. Various resolution enhancement techniques such as phase-shift mask, strong off-axis illumination and optical proximity correction together with high numerical aperture exposure system can extend KrF lithography to the technology node of 0.11

μm. Furthermore, full planarization process by using CMP processes widens latitude of lithography compared to non-planarization process. In order to fabricate 4Gb DRAM, a noble inter layer dielectric gap filling technology using spin-on-glass, self-aligned contact process relied on line-type pattern, novel W-bit line with stud, and triple CVD Al interconnection technology are newly developed based on our previous DRAM technology generations [1], [2], [3]. The capacitor technology for 4Gb DRAM is developed with a low temperature novel MIS structure, which is modified from the MIS capacitor technology of previous generations.

As the generation of the DRAM technology advances beyond 0.15 μm technology node, the performance of the array transistor (memory cell) seriously limits the speed performance and data retention time of the DRAM devices due to its reduced On-current (I_{ON}) and at the same time increased Off-current (I_{OFF}). In order to suppress the increase of I_{OFF} for planar array transistor, three-dimensional vertical array transistor with elongated vertical channel length has been proposed even with 0.15 μm technology node [4]. Although the vertical transistor can solve the I_{OFF} issue, it must solve the I_{ON} issue. Furthermore, vertical array transistor has to prove its production worthy capability through mass-production. It is still under investigation how far planar array transistor can be scaled down. It is generally conceived that the planar array transistor can be used down to 0.10 μm technology node and it can be expected to be down to 0.07 μm technology node with some modifications [5]. In order to use planar array transistor for 4Gb DRAM with 0.11 μm technology generation, 80nm array transistor technology with sub-80 nm array contact is required. The summary of key features of 0.11 μm DRAM technology for 4Gb DRAM is listed in Table 1 and compared with those of our previous 0.13 μm [1]

Table 1.   Key process features of 4Gb DRAM using 0.11 μm technology.

	0.15 μm	0.13 μm	0.11 μm
Lithography	KrF+RET	KrF+RET	KrF+Strong RET
Isolation	STI(HDP)	STI(HDP)	STI(HDP)
Gox	6nm	5nm (Nox)	4nm (Nox)
WL	TiSix	TiSix	TiSix
ILD1	HDP	HDP	SOG
Cell contact	Reverse T-type SAC	Bar-type SAC	Bar-type SAC
BL	W	W	W with Stud
Cell contact	Small cont	BC SAC	Line-Type SAC
S-poly	BOX+HSG	PAOCS+HSG	MSCC(=Concave+Cylinder)
Cap.dielec.	$Ta_2 O_5$	Al_2O_3	Al_2O_3
Metals	triple (1W+2Al)	triple (1W+2Al)	triple (3 CVD Al)
Heat budget	800 ℃	<700 ℃	<700 ℃

and 0.15 μm [2] generations. In this paper, those technologies for 4Gb DRAM with 0.11 μm technology node will be presented.

II. KEY TECHNOLOGIES FOR 0.11 μM DRAM GENERATION

A. 0.11 μm KrF Lithography

It is necessary to maximize the resolution of illumination system in the KrF exposure system to obtain 0.11 μm lithography. The maximum resolution can be achieved by using hard off-axis illumination technique with which the repetitive patterns in cell array can have maximum lithographic performance. However, the isolated patterns in periphery suffer from small latitude of photolithography such as small depth of focus margin. It is due to more severe optical loading effect of off-axis illumination than that of conventional illumination, even though the size of isolated pattern is much bigger than that of repetitive pattern in cell array. In order to solve the severe optical loading effect of isolated main patterns in periphery, supplementary patterns, whose primary role is to increase the first order and second order diffraction intensity of the isolated main pattern, one placed near isolated main patterns as shown in Fig. 1(a). The first order and second order diffraction intensity are important to form the optical image on the silicon. Most of the illumination system only takes the first order

diffraction due to its limited lens size. Therefore, the increased first order diffraction intensity due to supplementary patterns can improve the pattern fidelity of isolated patterns. The size of supplementary scattering bar patterns should be determined from the requirement such that it should not be imaged on the silicon as shown in Fig. 1(b). Using this technique, it was possible to obtain more than 0.3 μm depth-of-focus margin for both cell and peripheral areas simultaneously for all critical layers by this technique[6]. It is well known that the resolution can be enhanced with half-tone phase shift mask compared to binary mask [7], [8]. In addition, the fully planarized surface of all critical layers can greatly relieve the requirement of depth-of-focus margin so that the 0.3 μm depth-of-focus margin is acceptable even for such large chip of 4Gb DRAM.

B.   80 nm Array Transistor Technology

As the minimum feature size of DRAM decreases, it is very difficult to make the array transistor because of its two contradictory requirements of extremely small I_{OFF} and high I_{ON} for satisfying both data retention time and speed performance performance. The target value of I_{OFF} (extrapolated) should be smaller than order of fA (1×10^{-15}A). At the same time, the target value of I_{ON} must be greater than few μA (1×10^{-6} A). Such small I_{OFF} has been achieved by keeping the threshold voltage of array transistor above certain minimum level that is
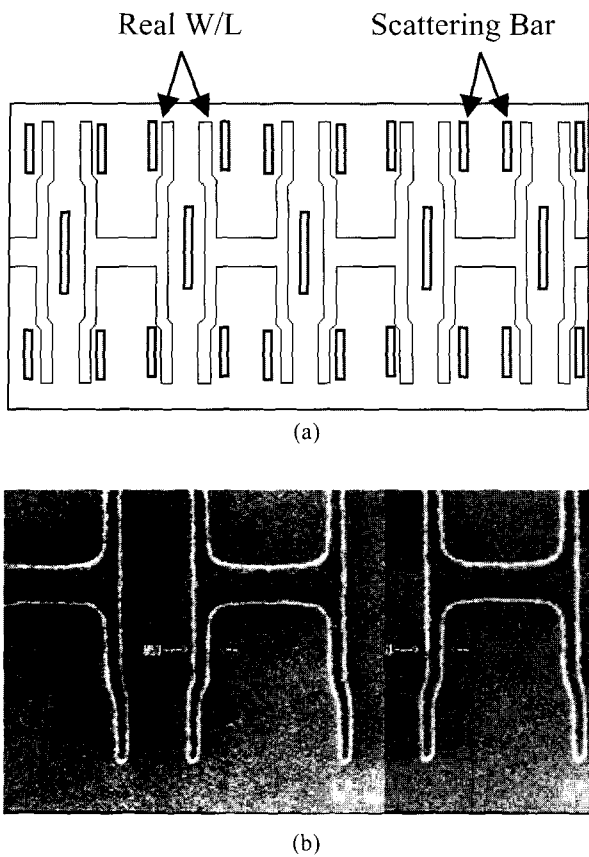
Real W/L   Scattering Bar

(a)

(b)

Fig. 1. Optical proximity correction technique using supplementary scattering bar pattern for isolated and semi-repetitive patterns which lose their depth-of-focus margin in case of hard off-axis illumination. (a) shows the shape of the supplementary scattering bar pattern which is placed near to main patterns. (b) shows the result of the printing of patterns shown in (a). Good pattern fidelity is achieved with scattering bar which does not form any images on the silicon.

approximately 1.0 V with substrate bias. The non-scalability of threshold voltage of array transistor inevitably decreases I_{ON} current as the device dimension shrinks [9]. The dimension of array transistor of 4Gb DRAM is equivalent to 80 nm array transistor where the channel width and the channel length are 75 nm shown in Fig. 2(a) and 80 nm shown in Fig. 2(b), respectively. This is the smallest array transistor ever fabricated. However, it is very concerned that such small array transistor could be properly operated with satisfying both requirements. Fig. 3 shows that the extrapolated I_{OFF} and I_{ON} of 80 nm planar array transistor are less than 1 fA and greater than 5 μA, respectively. The gate-induced drain leakage (GIDL) current is suppressed by optimizing re-oxidation process which is following
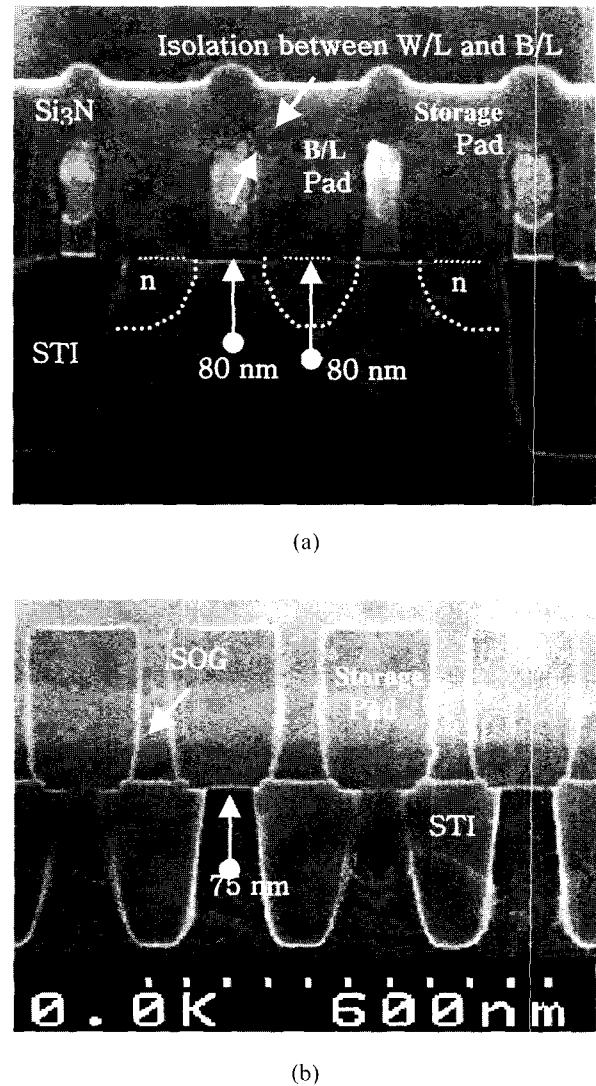

(a)

(b)

Fig. 2. The 80 nm array transistor for 4Gb DRAM using 0.11 μm DRAM technology. (a) shows a cross-sectional SEM image of array transistor along the bit line direction. The dimensions of array transistor for gate length, spacer thickness and contact hole size of landing pad are 80 nm, 30 nm, and 80 nm, respectively. (b) shows a cross-sectional SEM image of array transistor along the word line direction. The dimension of channel width of array transistor is 75 nm.

silicon nitride (Si_3N_4) spacer and it will not be an issue even beyond 80 nm array transistor. From these results, conventional planar 80 nm array transistor can meet both the requirements. Although threshold voltage variations of 100 mV/10 nm and 120 mV/10 nm, for the channel length and the channel width, respectively are little concerned, it can be further reduced below sub-100 mV/10 nm by using local channel and field implantation (LOCFI) [10].
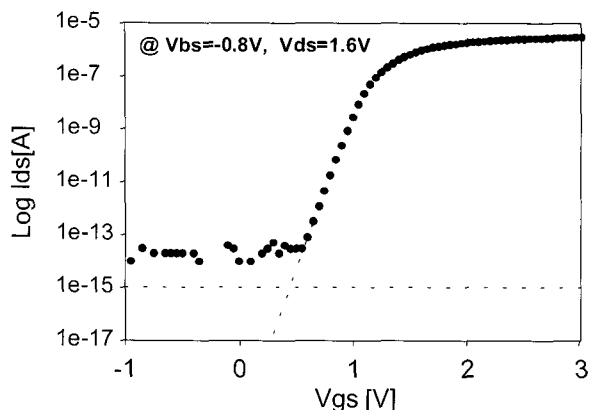
Fig. 3. I-V curve of 80 nm array transistor shown in Fig.2. I-V curve is measured with –0.8 V substrate bias and 1.6 V drain bias at room temperature. The extrapolated I_{OFF} at Vgs=0 is far smaller than 1 fA. No increase in I_{OFF} in negative gate bias indicates that 80 nm array transistor do not suffer from the GIDL current. The I_{ON} current is greater than 5 μA at 2 V gate bias.
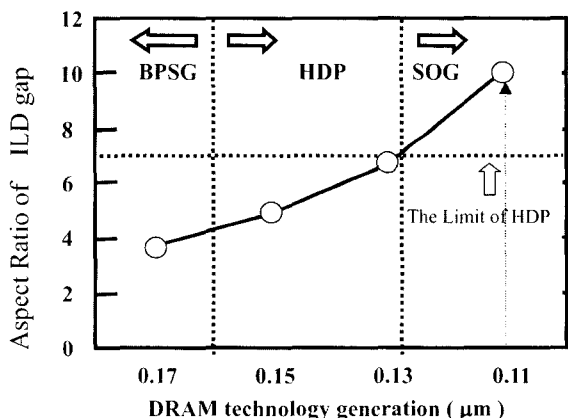

Fig. 4. The trend of aspect ratio of inter-layer dielectric gap with DRAM technology generation. It is shown that the aspect ratio of gap increases with DRAM technology generation and it reaches around 10 at 0.11 μm technology node where commonly used BPSG and HDP oxide can not be useful. Down to 0.15 μm technology node, BPSG with high temperature flowing can be used. HDP oxide having better gap filling can be used for 0.15~0.13 μm technology. For 0.11 μm technology node, novel gap-filling technology using spin-on-glass will be necessary.

C.   Novel Inter-Layer-Dielectric Gap Filling Technology

As scaling down the design rule, one of most serious problems is to fill an inter-layer dielectric into the gap whose aspect ratio tends to increase because it is more difficult to scale down vertical dimension scaling than laterally dimensional scaling [11], [12]. As a result, the aspect ratio of the gap reaches to more than 10 in 0.11 μm 4Gb DRAM as shown in Fig. 4. For such high aspect ratio, the gap-filling materials such as BPSG and HDP-oxide can be no longer useful because of their insufficient gap-filling capability. Therefore, it is necessary to develop novel gap-filling technology. A spin-on-glass is selected as gap-filling material because of its superior gap-filling capability. In fact, spin-on-glass does not have any limitation of aspect ratio due to its nature of spin-coating process where high fluidity always maintains. The spin-on-glass gap-filling technology consists of the spin-coating, baking, and subsequent annealing · at high temperature around 700 °C. The purpose of the baking is to break the chemical bond of deposited film, and thereby to form silica. By properly optimizing the baking process, the subsequent annealing process can transform silica film into the chemically and mechanically stable oxide. Fig. 5 shows the good inter-layer dielectric gap-filling by spin-on-glass technology developed in this paper.
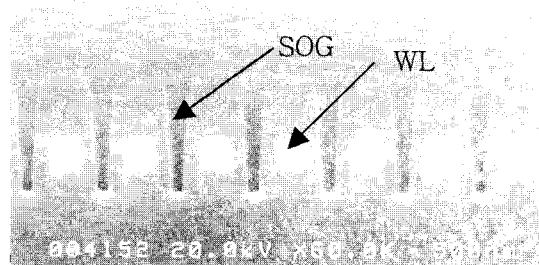

Fig. 5. A cross-sectional SEM image to show the excellent interlayer dielectric gap filling for 4Gb DRAM with novel gap filling technology where aspect ratio of 10 is perfectly gap-filled without any voids and seams.

D.   Sub-80 nm Memory Cell Contact Technology

In order to have high functionality of 4Gb DRAM, sub-80 nm memory cell landing pad should be prepared, which requires sub-80 nm memory cell contact technology as seen in Fig. 2. It is a great challenge to maintain low contact resistance without contact failure in such small contact. It is often observed that thin native oxides or etch-by products easily remain on improperly prepared interface and generates contact failure or induces high contact resistance, thereby resulting in
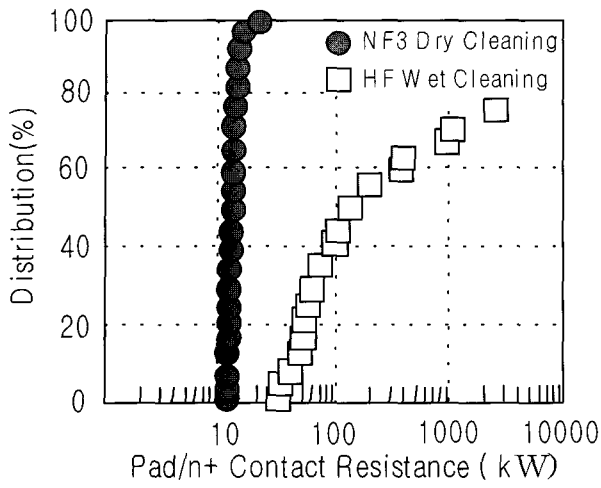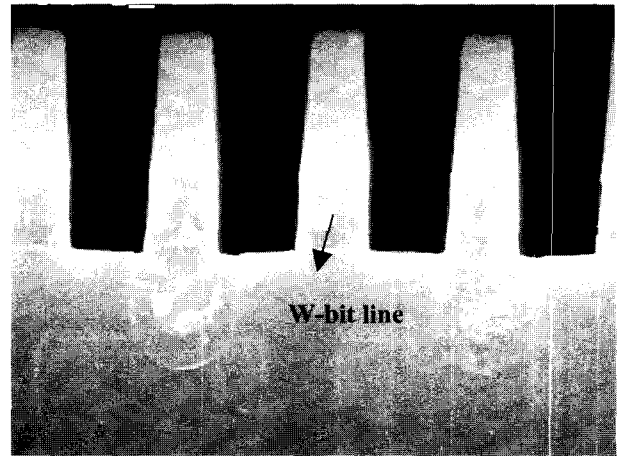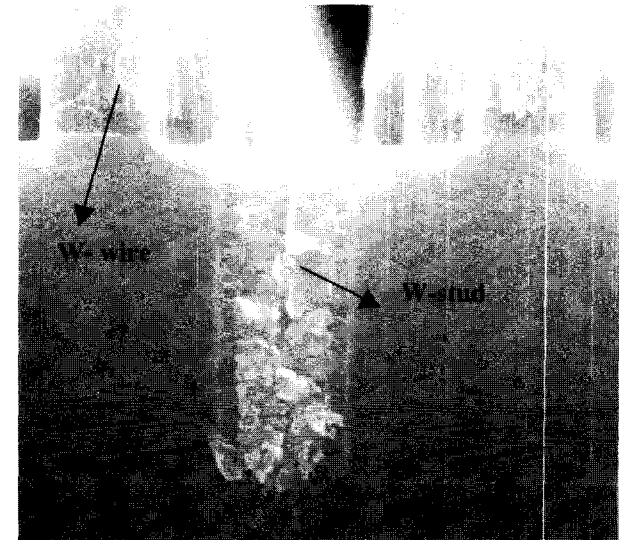
(a)
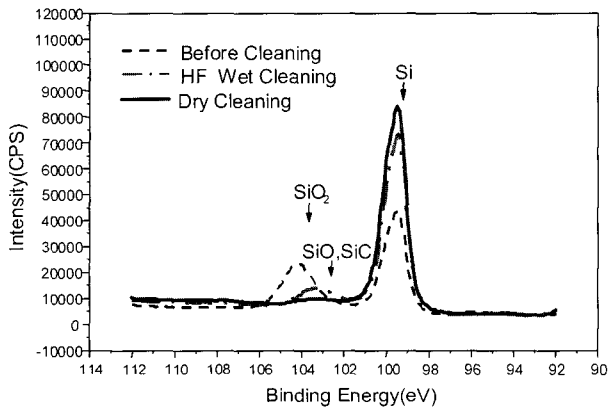
(b)

Fig. 6. Novel surface cleaning technology for sub-80 nm array contact process. (a) shows the contact resistance of 80 nm array contact with conventional wet cleaning and novel NF₃ cleaning. (b) shows the XPS results of silicon surface before and after contact hole cleaning with conventional wet cleaning and novel dry cleaning. The peak corresponding to oxide peak which originates from the native oxide and the peak corresponding to SiC which comes from the polymer of etch by-product are clearly observed before contact hole cleaning. The superior removal ability of these unwanted layers from silicon surface is clearly seen in case of the novel dry cleaning.

(a)

(b)

Fig. 7. Novel W-bit line technology with which both conventional wiring line for interconnection and contact stud used as landing pad for metal contact are simultaneously formed. (a) shows the cross-sectional image of the bit line in cell array. (b) shows the contact stud on which metal contact will be landed.

random single bit failure. Therefore, in order to eliminate the surface oxide at interface, hydrogen termination or oxide breaking process is needed before n+-pad polysilicon deposition. Unfortunately, none of those is possibly implemented in 4Gb DRAM because of its limited effectiveness in the case of hydrogen termination or unallowably high thermal budget due to high temperature in the case of oxide breaking process. Therefore,

we develop a novel dry cleaning process with nitrogen-fluoride (NF₃) remote plasma. The contact resistance with or without novel dry cleaning is shown in Fig. 6(a). As clearly indicated in Fig. 6(a), the contact resistance with novel dry cleaning is much smaller than that without dry cleaning because of removing native oxide and polymer. The XPS data shown in Fig. 6(b) clearly shows that the dry cleaning process is most effective in removing native oxide and polymer.

E. Novel W-Bit Line Technology For Borderless Metal Contact

Another important issue in 4Gb DRAM technology is the metal contact that might have unmanageably high aspect ratio of more than 15 in case of conventional direct metal contact scheme where no landing pad is used. Therefore, in this work, the metal contact with W-landing pad, which is formed at bit line level, is newly developed. In this way, the aspect ratio of metal contact can be decreased to 10 or small, which can be manageably accepted in contact hole etching and subsequent contact hole-filling process with metal. The metal contact is formed on the landing pad with a method of borderless contact process.

The process sequence for novel borderless contact is reported elsewhere [13]. The brief sequences are as follows: First, W-plug is formed in by W deposition and CMP processes, then W film is again deposited over W-plug to form both W bit line in cell array and W-wiring in periphery. Forming W-wring pattern results in W bit line interconnections and W-studs simultaneously in periphery as shown in Fig. 7. Then, Si_3N_4 layer is deposited and patterned, where Si_3N_4 layer works as etch-stopping for metal contact etch. Finally metal contact process is proceeded. It is well known that the resistance of W-bit line contact is quite sensitive to the subsequent thermal budget so that the higher thermal budget leads to the higher resistance [1]. Especially, bit line to P+ contact resistance is rapidly degraded above 700 °C In our 4Gb DRAM, Al_2O_3 capacitor dielectric is used, which requires only 450 °C of thermal deposition process. It is noticed that the thermal budget after bit line process is always remained below 650 °C.

F. Novel Storage Landing Pad Technology

In 0.11 μm technology node, a conventional hole-type storage node SAC scheme can no longer survive, which means that a different scheme should be devised. In this work, we used a line-type SAC pattern for storage node pad. The main difficulty in the hole-type SAC pattern is an insufficient overlay margin in 0.11 μm design rule, which leads to the etch-stopping and not-open problems because small opening area to be etched is prone to induce etching stopping even for small mis-alignment as shown in Fig. 8. On the other hand, there were no such

difficulties in the line-type SAC pattern because line-type SAC pattern can provide more opening area to etch than hole-type pattern.
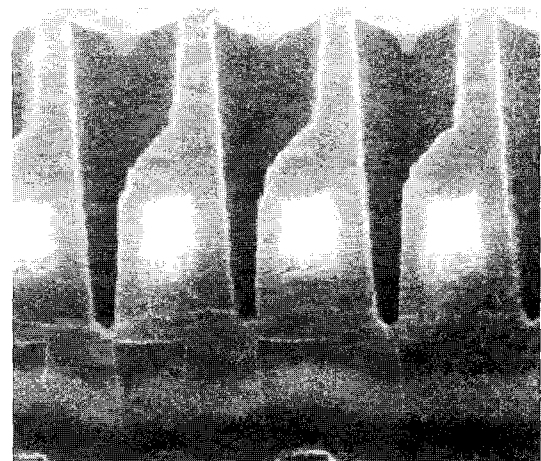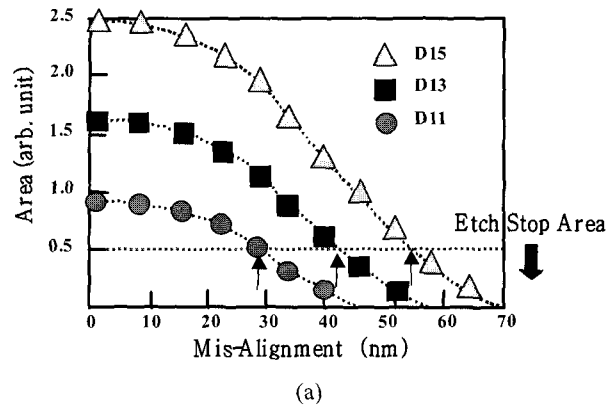

(a)

(b)

Fig. 8. Limitations of the conventional self-aligned contact process based on contact hole type patterns. (a) shows the requirement of mis-alignment toleran with technology generation. The tolerance of mis-alignment of 0.11 μm technology node can not be met within the limit of lithography tool. (b) shows an example of etch stopping due to mis-alignment.

It is noteworthy that both word line and bit line are encapsulated with Si_3N_4 whose role is to protect word line and bit line during SAC etching and to serve as polishing stopping layer for CMP pad separation. Therefore, it is very important to maintain sufficient thickness of Si_3N_4 film. The electrical evaluations show that the line-type SAC pattern generates higher breakdown voltage and less leakage current than that of hole-type SAC pattern, which means that the Si_3N_4 loss is less consumed in the line-type SAC pattern than in the

hole-type SAC pattern. This result can be explained by homogeneous etch condition of line-type SAC process in which opening area to be etched does not depend on alignment tolerance induced from lithographic process.
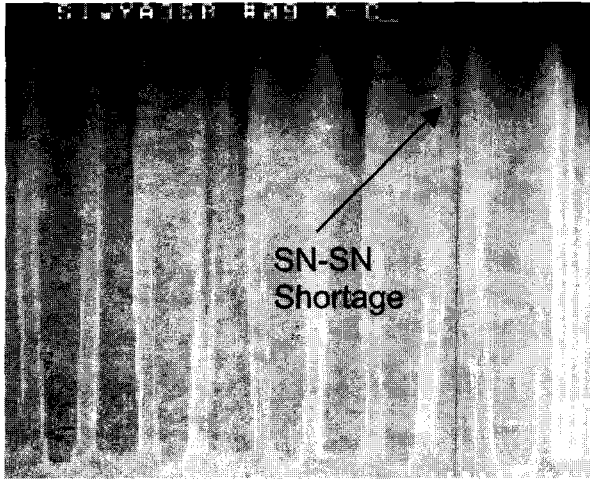

Fig. 9. An example for storage node-storage node shortage of one-cylindrical capacitor structure. The mechanical strength of capacitor to resist SN-SN shortage rapidly decreases with device feature size.

G. Mechanically Robust Capacitor Technology

As the device dimension shrinks, twin bit failure due to the shortage of storage node (SN)-SN as illustrated in Fig. 9, becomes serious yield limiting factor. The SN-SN shortage is closely related to the mechanical stability of capacitor structure [14]. The mechanical strength of capacitor to resist against SN-SN shortage rapidly decreases as device feature size decreases. And it also decreases as the stack height of capacitor increases. In order to improve the mechanical stability of capacitor, novel capacitor structure is developed by merging cylinder structure with concave structure. It is known that concave structure does not have any mechanical stability issue although it has the small available capacitor area for given dimension. On the contrary, cylinder structure has the largest available capacitor area for given dimension. By merging these two extremes, we can successfully develop the mechanically stable capacitor without losing capacitance as shown in Fig. 10. As a result, the commonly observed twin-bit failure due to collapse of storage node is completely eliminated while maintaining cell capacitance greater than 25 fF/cell and the leakage current smaller than 1 fF/cell.

These values of capacitance are obtained with 3.0 nm oxide equivalent thickness of Al_2O_3 dielectric for 1.2 μm thick cylinder and 0.6 μm thick concave structure.
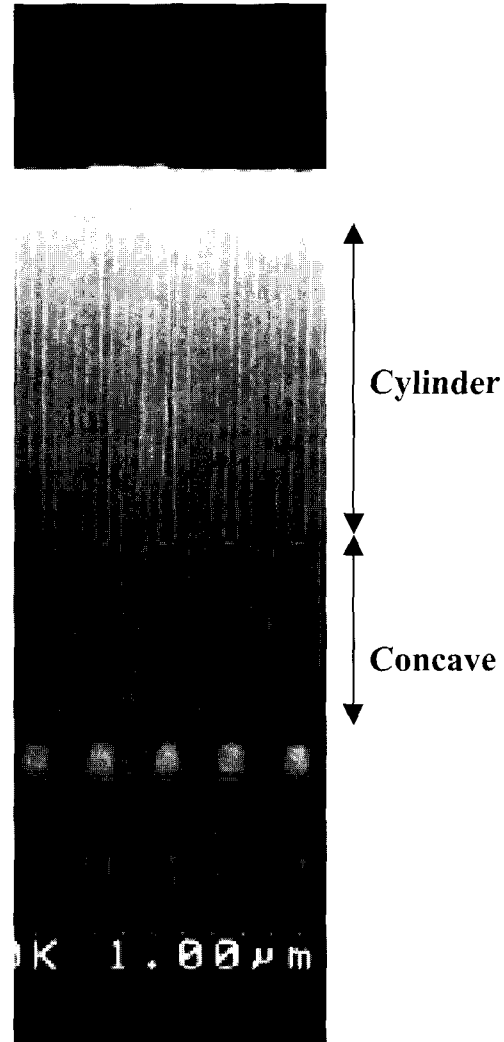

Fig. 10. A cross-sectional SEM image of mechanically stable MIS capacitor structure where concave structure is additionally inserted between cylindrical structure and storage node contact pad.

H. Triple-Level CVD-Al Technology

For the back-end-of-line (BEOL) processes, the triple metal interconnections and the full planarization scheme one developed as shown in Fig. 11. HDP oxide is deposited for inter-metallic dielectric and CMP process is followed for planarization of inter-metallic dielectric. The fully planarized BEOL process not only widens latitude of lithography but also gives wide process

margin for metal etching.

For inter metal connections, via-contact is filled with the CVD (chemical vapor deposition) Al process, which completely eliminates the voids in via-contact for conventional sputtering process. Furthermore, the CVD Al has several advantages such as a good filling property, low resistance, and simplicity in a process over conventional sputtering Al process.
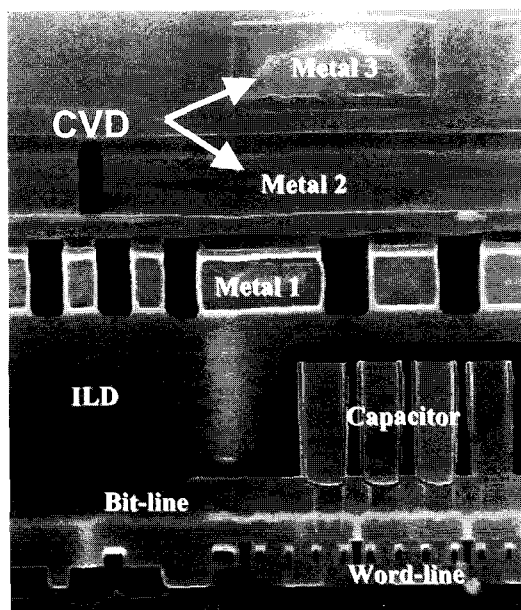

Fig. 11. A cross-sectional SEM of the fully processed 4Gb DRAM using 0.11 μm DRAM technology. The fully planarized structure is clearly shown in this figure.

Fully planarized triple CVD Al process can make metal pitches relaxed, compared to double-metal process, resulting in the reduction of block failure. Furthermore, it improves performance with interconnect delay minimization and power line fortification, thereby permitting low voltage operation.

III. 4Gb DRAM WITH 0.11μM DRAM TECHNOLOGY

A 1.8V, 4Gb DDR SDRAM of 645 mm^2 die size and 0.10 μm^2 cell size as shown in Fig. 12 using aforementioned 0.11 μm DRAM technology generation is designed and fabricated for low voltage and high speed operation in its full density for the first time. To insure good device yield and performance, constraints due to the large chip size must be overcome. It becomes

imperative to make process controls for reducing defects and suppress parameter variations as well as design schemes for controlling the signal skews. The straight gate instead of meandering gate in the core region can curtail the critical dimension variations, inhibiting device mismatches. In order to minimize the signal skew, repeater circuits are used in row and column decoder signals paths and core-control signal paths. Despite of the chip size overhead of 1.22 %, they are effective in re-shaping over-loaded signals and rejecting coupled noise accumulation. Within 512 Mb mat, active and pre-charge control skews under 1.5 ns are obtained with the array voltage of 1.5 V [15]. Furthermore, the amplifier sensitivity and sensing margin are improved with gain-controlled pre-sensing and the reference bit-line calibration schemes. The gain-controlled pre-sensing scheme increases the sensing margin and speed by employing trans-conductance-matched pre-amplification for enhancing the sensitivity and stability of CMOS latch amplifier. Proposed scheme consists of steps of (i) pre-biasing of the sense amplifier, (ii) pre-sensing with gain control of the trans-conductance element, and (iii) full restoring using CMOS latch. Fig. 13(a) shows the simplified schematic of the proposed technique. A pair of n-MOSFET (MN1) and p-MOSFET (MP1) acts like a composite transistor with equivalent Vgs and trans-conductance. Similarly MN2 and MP2 act like another composite transistor with matching characteristics. Two composite transistors form a linear conductance element to amplify the relatively small current signal from a DRAM storage cell capacitor. Fig. 13(b) is the simulation results showing the pre-amplification with an enhancement of the sensing enable time.

The reference bit line calibration scheme can actively mimic the cell data retention characteristics and yield an optimal voltage level for the reference bit-line from the charge shared voltage from replica bit line pairs. Cell data is dependent on many factors such as the write-back voltage in active restore and data charge loss due to cell and junction leakage. Under these conditions, data1 (D1) and data0 (D0) charge-shared with the ideally half-Vcc pre-charged reference bit line will result in asymmetric D1 and D0 sensing margins. In the reference bit-line calibration scheme, the reference voltage for an equal D1 and D0 sensing margin is determined with an in-situ calibration using replica cells, and the bit-line voltage
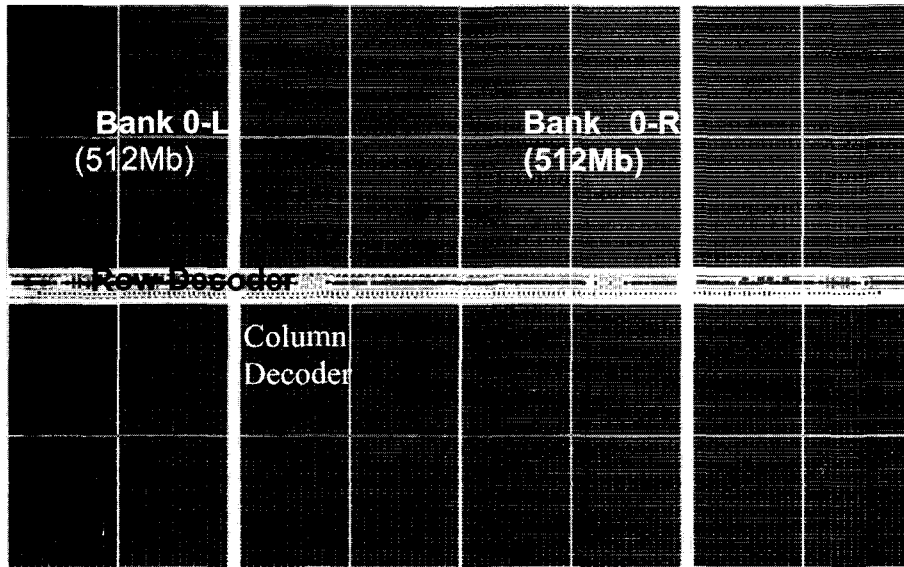
Fig. 12. A die photograph of SDR/DDR 4Gb DRAM which has 650 mm^2 chip size and 0.10 μm^2 cell size. The chip consists of 8 banks of 512Mb mat which is independently operated each other.

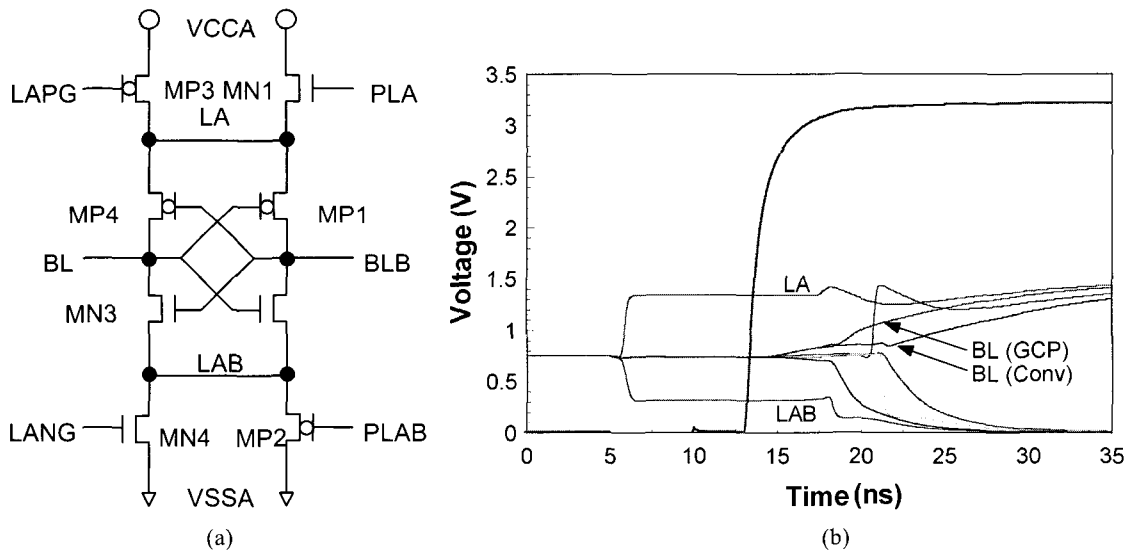(a)   (b)

Fig. 13. The gain control pre-sensing scheme for improving performance of the CMOS latch sense amplifier. (a) shows the simplified circuit schematics of the gain-control pre-sensing scheme. (b) shows that the gain-control pre-sensing scheme enhances the sensing speed compared to conventional scheme.

generator is actively regulated accordingly after a few operation cycles [15].

Together with the chip-size-efficient core signal repeating architecture, gain-controlled pre-sensing and the reference bit-line calibration schemes ensure reliable low-voltage and high-speed cell and core operations.

IV. CONCLUSIONS

A 4Gb DRAM of 645 mm^2 die size and 0.10 μm^2 cell size is developed with 0.11 μm DRAM technology where KrF photolithography is extendedly used from 0.13 μm DRAM technology. The key processes of 0.11 μm DRAM technology generation are as follows: 80 nm

array transistor, novel gap filling technology, sub-80 nm memory cell contact, novel W-bit line technology for borderless metal contact, novel storage landing pad technology, mechanically robust capacitor, triple-level CVD-Al technology. Furthermore, the performance degradation originated from large chip is minimized by novel design approaches such as skew minimization, gain-control pre-sensing, and reference bit-line calibration scheme. The technologies developed in this work have good compatibility for previous generation as well as good extendibility for next generations.

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