W Polymetal Gate Technology for Giga Bit DRAM

Jong Wan Jung, Sang Beom Han, and Kyungho Lee

Abstract— **W polymetal gate technology for giga bit DRAM are presented. Key module processes for polymetal gate are studied in detail. W/WN_x/poly-silicon adopted for a word line of 256Mbit DRAM has good gate oxide integrity and junction leakage characteristics through full integration, which is comparable to those of conventional WSi_x/Poly-silicon gate process. These results undoubtedly show that W/WN_x/poly-silicon is the strongest candidate as a word line for Giga bit DRAM.**

Index Terms– **semiconductor, DRAM, process integration, metal gate process, reliability.**

I. INTRODUCTION

To reduce the chip area of 1Gbit DRAMs and beyond, reducing the area of peripheral circuits is essencial as well as reducing the size of each memory cell. Increased number of columns per word line allows the reduced number of peripheral circuit. Therefore, the RC delay due to the resistance of word line is a key factor to succeed in getting a smaller chip. Conventional W (WSi_x) or Ti polycide($TiSi_x$) have been adopted for 64M, 128M, and 256Mbit DRAM. For productive giga bit DRAM, the sheet resistance must be reduced to below 5 Ω/sq (Fig. 1) [1]. However, conventional polycide such as WSi_x or $TiSi_x$ can not fully satisfy this requirement. When we simply increase the thickness of the stack structure with WSi_x or $TiSi_x$ to reduce the sheet resistance, several issues occur, such as etch profile, BPSG void, and increased parasitic capacitance. Furthermore, sheet resistance of WSi_x and $TiSi_x$ rapidly increases as the width of word line being decreased [2]. These several issues make the conventional polycide improper as a gate electrode for Giga bit DRAM application.

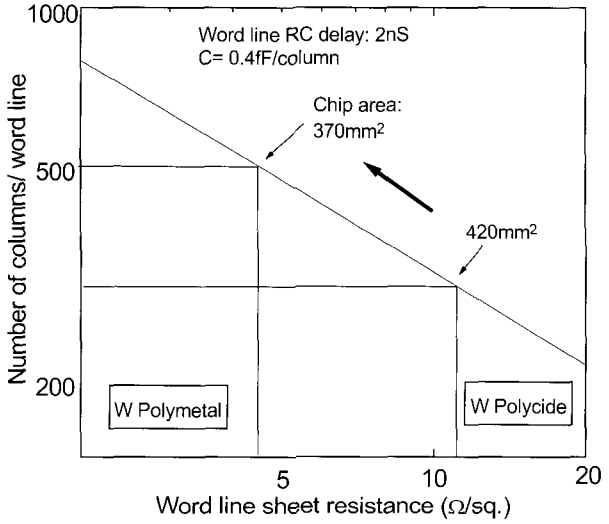

Fig. 1. Dependence of affordable number of columns per word line under criteria of the word line RC delay is 2 ns and capacitance per word line is 0.4 fF [1].

On the contrary, W polymetal gate shows low sheet resistance even at very narrow line width(<0.1μm). Unlike W or Ti polycide, in case of W polymetal gate, a barrier metal layer is needed in order to prevent the forming of silicide layer which shows high contact resistance. Two representative candidates for W polymetal gate are W/WN_x/poly-silicon and W/TiN_x/poly-silicon, and some research works have shown electrical characteristics for them [3-5]. In the case of W/TiN_x/poly-silicon, it has been known to be difficult to selectively reoxidize silicon without oxidizing Ti [6]. Therefore W/WN_x/poly-silicon seems likely most promising technology for polymetal gate of Giga bit DRAM.

Our group has been developing 256Mbit and giga bit DRAM technologies with W/WN_x/poly-silicon as a gate electrode, and recently the full integration has been presented for the first time [7]. In this paper, we will show the full integration technologies with W polymetal

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gate, which includes etching, cleaning, and selective oxidation process.

II. W Polymetal Gate technologies

Full integration scheme for the polymetal gate process is shown in Fig. 2. Polymetal gate technologies can be mainly classified into four modules, which include the gate stack structure, gate etch, cleaning, and post reoxidation [8].

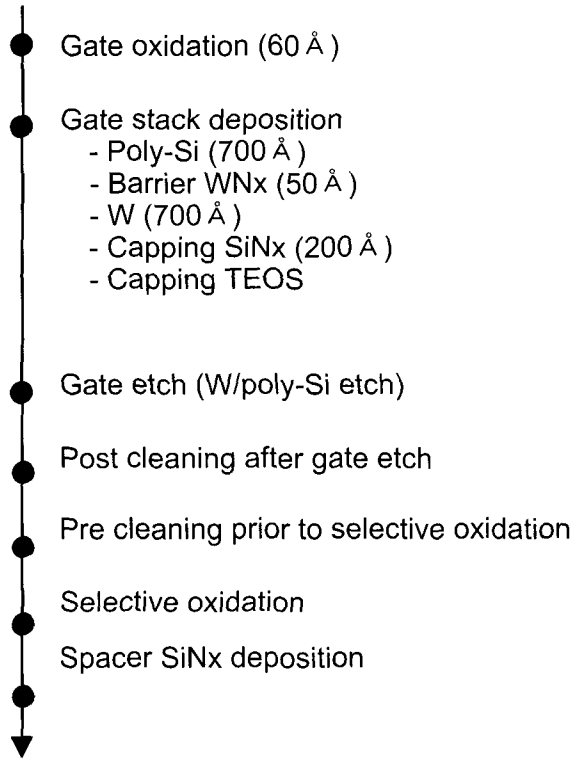


Fig. 2. Process flows for W polymetal gate with the pre poly plug cell scheme technology.

A. *Gate Stack*

The gate stack consists of a gate electrode(W/WNx/poly-silicon) and the capping layers which are used for isolation and a hard mask for the gate etching. The gate electrode used in this paper consists of 700 Å/50 Å, W/WN_x on top of 700 Å- n^+-dope poly-silicon. A 50 Å thick WN_x is used for a barrier film to prevent forming the W silicide between W and poly-silicon[9]. On the gate electrode, 200 Å thick SiN_x film as a first capping layer was deposited for the blocking oxidation of W gate through the following processes. Then, about 3000 Å thick SiO_2 film as a second capping layer was deposited on SiN_x film. A suitable capping film should be chosen depending on the cell integration scheme. To make the self aligned contact process, SiN_x film must be used for the capping and spacer layer. In our work, SiO_2 film was adopted for the pre poly plug(PPP) cell schme[10]. In the PPP cell scheme, as a landing pad, poly-silicon is etched-out. The etch selectivity is high for SiO_2 compared to SiNx during poly-silicon etching. This is why SiO_2 layer is used in the PPP cell scheme. The stack structure is shown in Table 1.

Table 1. Gate stack structure applied for W/WN_x/poly-silicon gate.

Electrode	Poly-Si/WNx/W
Capping layer	• Capping layer1: SiNx 200 Å (for protecting W from oxidizing) • Capping layer2: SiO_2 3000 Å (In the case of SAC, SiNx is used)
Spacer layer	• Spaer1: SiNx (for protecting side W from oxidizing) • Spacer2: SiO_2 (In the case of SAC, SiNx is used)

B. *Gate Etching*

Etching of W polymetal (W/poly-silicon) is somewhat different from that of the conventional W polycide gate (WSix/poly-silicon). The basic difference comes from the etch chemistry. In the case of the conventional W polycide gate, Cl_2 based chemistry is used for etching both WSix and poly-silicon. On the contrary, for the W/poly-silicon gate, two kinds of chemistry should be used, which are SF_6, CF_4 or NF_3 for W etching and Cl_2 for poly-silicon etching. This difference of the etching chemistry also makes the different etching procedure as shown in Table 2. It should be noted that the gate etch with the low damage is required not to degrade the retention time characteristics of DRAM [11].

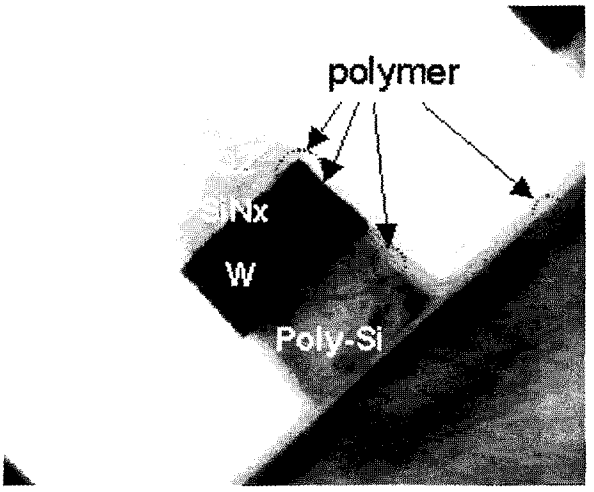
C. *Cleaning*

During the gate etching process, a lot of oxide polymer is usually formed, and these should be removed through cleaning (Fig. 3). Cleaning for W needs a special care because the W exposed on both sides of the gate edge can be easily damaged during the cleaning

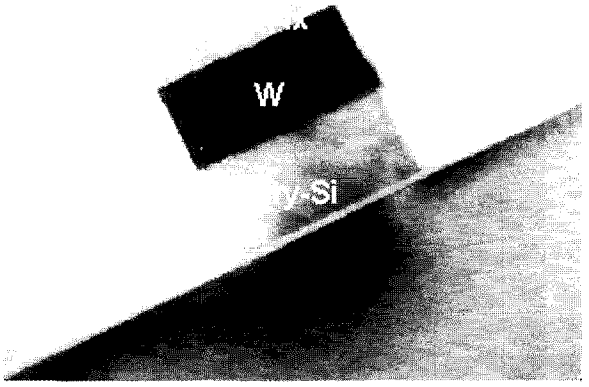
Table 2. Comparison of etching process of conventional W polycide and W/WN_x/poly-silicon gate.

	WSix/poly-Si	W/poly-Si
Gas Chemistry	• WSix etch: Cl_2 base • poly-Si: Cl_2 base	• W etch: SF_6, CF_4, NF_3 • poly -Si etch: Cl_2 base
Etch process flow	• WSix (EPD) • poly-Si (EPD) • Over Etch for poly-Si WSix/poly-Si	• W/WNx (EPD) • Over etch of W/WNx • poly-Si (EPD) • Over etch for poly-Si

(EPD: etch point detection).



(a)



(b)

Fig. 3. Cross sectional TEM view of gate electrode through gate etching (a) before cleaning (b) after cleaning. A lot of oxide polymer are shown before cleaning.

process. Cleaning solution which contains H_2O_2 must be avoided because it easily damages W. In general, HF or BOE is used. For pre-furnace cleaning, we adopted a mixture of H_2SO_4 and deionized water to remove the impurities without damaging oxide and W.

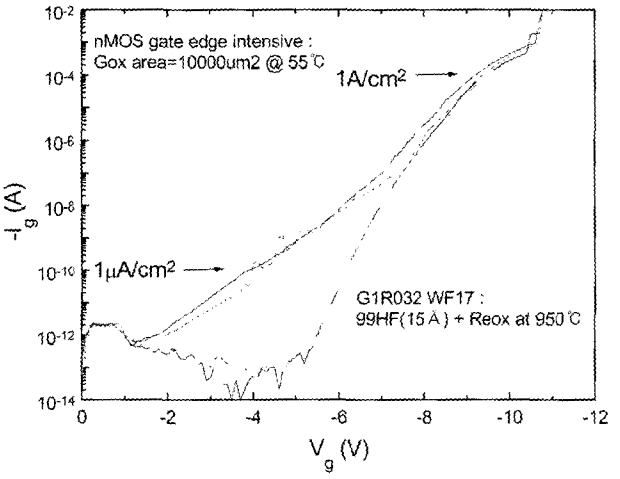


Fig. 4. Degradation of gate oxide reliability caused by insufficient post oxidation, which means the thickness of post oxidation should be thick enough to recover the thin oxide at gate edge.

D. *Post Oxidation (Selective Oxidation)*

Post oxidation is needed to cure the damaged oxide during the gate etching and to increase the thickness of oxide at the gate edge. Also the gate oxide integrity can be degraded by the insufficient post oxidation. Fig. 4 shows the degraded the gate oxide integrity (GOI) characteristics caused by the insufficient post oxidation, which means the thickness of the post oxidation should be thick enough to recover the thinned oxide at the gate edge. Since W is easily oxidized at temperature above 350°C in the oxygen ambient, if W is oxidized, it swelled out, which results in the failure of circuits. Therefore post oxidation in the W/poly-silicon gate process should

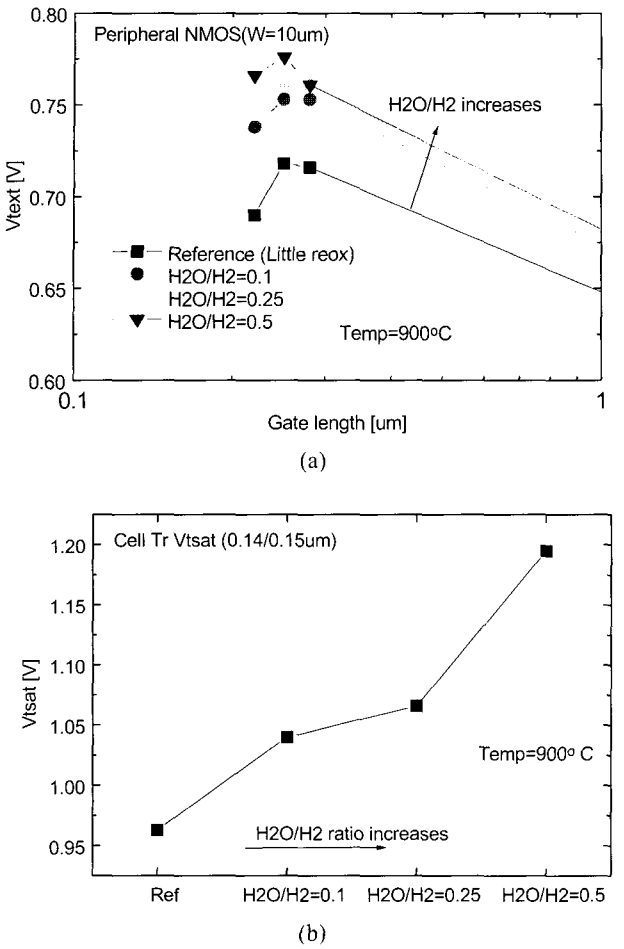


Fig. 5. Change of short channel effect of NMOSFET with H_2O/H_2 ratio. (a) a peripheral NMOSFET and (b) a cell NMOSFET. Short channel effect decreases as H_2O/H_2 ratio increases.

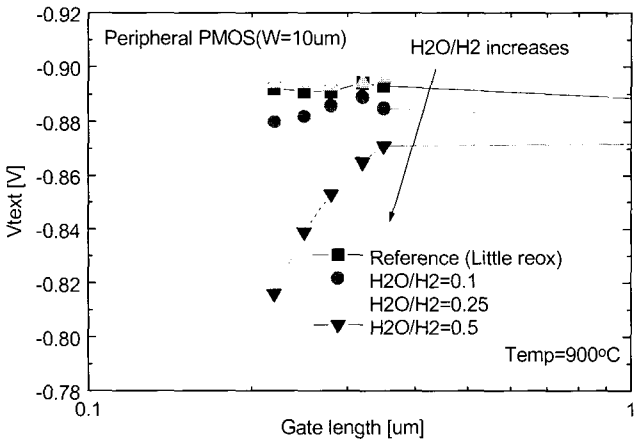


Fig. 6. Change of short channel effect of peripheral PMOSFET with H_2O/H_2 ratio. The threshold voltage of PMOSFET slowly decreases at low H_2O/H_2 ratio, but it abruptly decreases at 0.5 of H_2O/H_2 ratio.

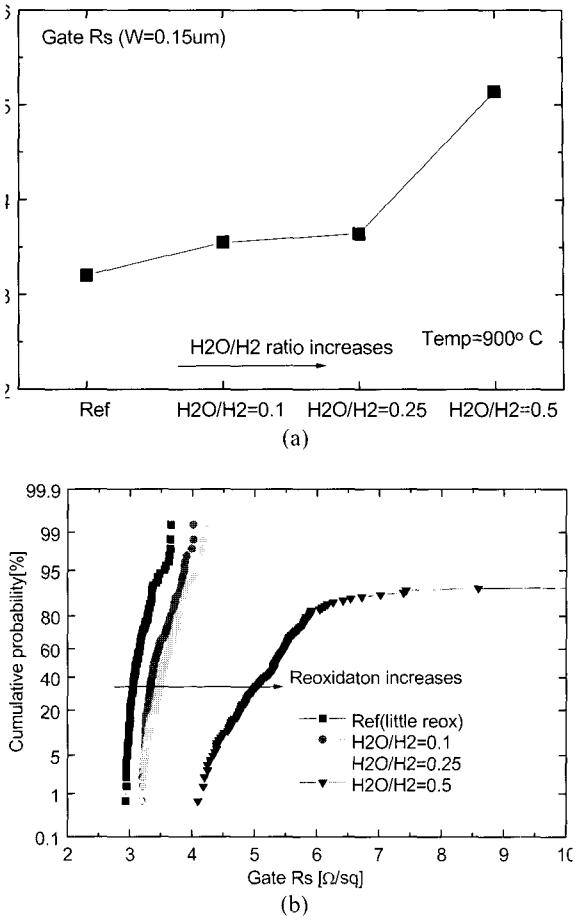
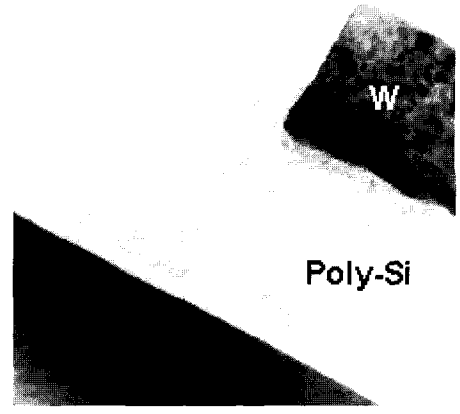


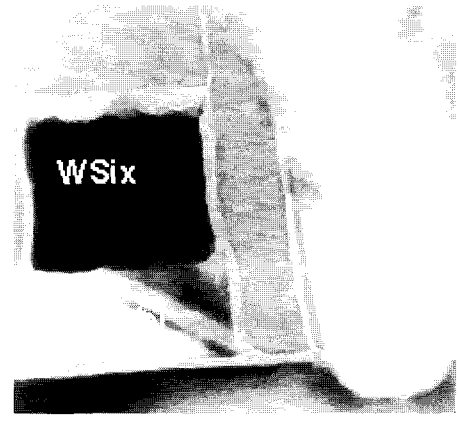
Fig. 7. Change of the sheet resistance of W polymetal gate with H_2O/H_2 ratio. (a) The average and (b) uniformity value slowly increases at low H_2O/H_2 ratio, but they abruptly increase at 0.5 of H_2O/H_2 ratio.

selectively oxidize silicon without oxidizing W. Silicon can be selectively oxidized at the specific H_2O/H_2 ambient [6]. In this work, the selective oxidation was performed using RTA in the optimized H_2O/H_2 mixture ambient. From the device point of view, it should be noted that the post oxidation can severely change the device characteristics. Fig. 5 and 6 show the change of the device characteristics with the H_2O/H_2 mixture ratio. It can be shown that the threshold voltage of the cell and pheripheral NMOSFET gradually increases as the H_2O/H_2 ratio increases. On the contrary, the threshold voltage of PMOSFET gradually decreases at the low H_2O/H_2 mixture ratio, however, it abruptly changes at 0.5 of the H_2O/H_2 mixture ratio. This change of the short channel effect can be thought to be due to the oxidation enhanced diffusion(OED) of boron during the post oxidation. Buried channel PMOSFET is likely to be

more susceptible to the OED. The average and uniformity characteristics of the sheet resitance also shows the same tendancy (Fig. 7). It can be seen that the uniformity and average value of the sheet resistance also abruptly increases at 0.5 of the H_2O/H_2 mixture ratio. These results present that the sufficient and high selective oxidation while maintaining good device characteristics is very important in the post oxidation for the polymetal gate process. Fig. 8 shows the TEM photograph of the W polymetal gate and the W polycide gate after the post oxidation (RTP and furnace are applied for the post oxidation of the polymetal gate and polycide gate, respectively.). After the post oxidation, a blocking SiN_x film with the thickness of 100~200 Å was deposited for preventing the W gate exposed on edge sides from oxidizing.



(a)



(b)

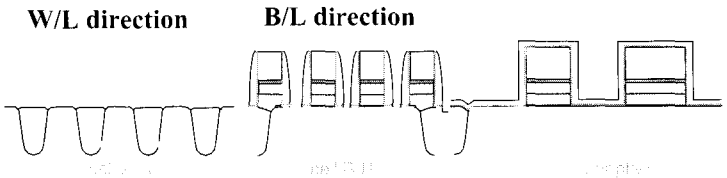
Fig. 8. TEM photograph of W polymetal gate and conventional W polycide gate after post oxidation. W polymetal gate is oxidized by RTP at 900°C and W polycide gate is oxidized by furnace at 850°C.

III. Full Integration & Characteristics

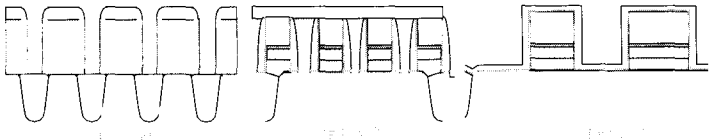
248nm KrF with high NA was applied for critical layers. The thickness of shallow trench isolation was 3000 Å and thin gate oxide (60 Å) was used to prevent the short channel effect of transistors. Tungsten (W) was adopted for both gate line and bit line, and the pre poly plug(PPP) scheme was applied for cell pads and storage contacts [10]. In order to achieve the high capacitance, MIS(metal insulator Si)-Ta_2O_5 with the rugged type inner surface(inner cylinder) was used. Key technologies of $8F^2$, 0.15 μm 256Mbit DRAM were summarized in Table 3. Since the PPP technology forms poly plug ahead of the ILD formation, high selectivity oxide etch to nitride and ILD void problem in the self aligned contact (SAC) process can be basically avoided. Fig. 9 shows the schematic process flow of the PPP process. After the gate and SiNx/SiO_2 spacer formation, poly-silicon for landing pads was deposited and planarized using chemical mechanical polishing (CMP). CP1(Cell plug1, landing pad) was formed by the poly-silicon etching on the field area. Fig. 10 shows the mask pattern of CP1 and the SEM image after fabrication. After the bit lines stacked with barrier /W/oxide were patterned on an ILD layer, the oxide spacer was formed. Then, ILD layer between bit lines was additionally etched away until the top of CP1 poly-silicon was exposed. CP2 (cell pad2, storage node contact) was patterned with the same procedure the CP1 formation. CP2 was separated by the deposition of ILD layer and CMP. Fig. 11 shows the mask pattern of CP2 and the corresponding SEM image after fabrication. As shown in Fig. 11, the PPP process has an advantage in the aspect of the CP2 process since the patterning for the line type CP2 is much easier than that of the conventional hole type in the SAC process. The typical capacitance characteristics of Ta_2O_5 capacitor is 26~30 fF/cell. It exhibits good leakage characteristics, as shown in Fig. 12, which are 0.02 fA/cell and 0.3 fA/cell at 1.0 V and 1.26 V of the plate voltage, respectively. Fig. 13 and 14 show the cross sectional SEM images after full integration. Fig. 15 shows the photograph of a fabricated 256Mbit DRAM. One of the major concerns of the polymetal gate stack is the gate oxide reliability. Comparing the charge to breakdown(QBD) characteristics between the W polymetal gate and the

Table 3. Key technologies of 0.15μm-256Mbit DRAM with W polymetal gate.

Lithography	248nm KrF, I line (PSM)
Isolation	STI (3000 Å)
Gox	60 Å
WL	W/WN_x/poly-Si, L/S = 0.14μm/0.15μm
ILD1(WL spacer)	TEOS (SiNx in the case of SAC)
Cell pads	Pre Poly Plug(PPP) WL spacer +poly deposition +CMP+Etch
Bit line	W
Storage contact	PPP, BL spacer + poly deposition + Etch+ ILD3 deposition+ CMP
Cap dielectric	Ta_2O_5
Plate	TiN

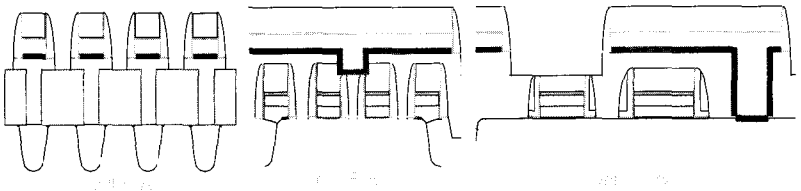


(a) Gate and spacer formation (spacer etch is performed only in cell region)

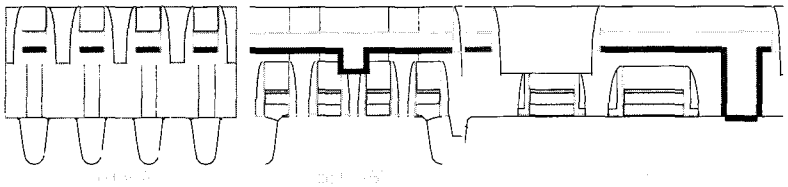


(b) CP1 poly Si deposition and CMP. CP1 pattern and etch

(c) ILD deposition and bit line contact formation

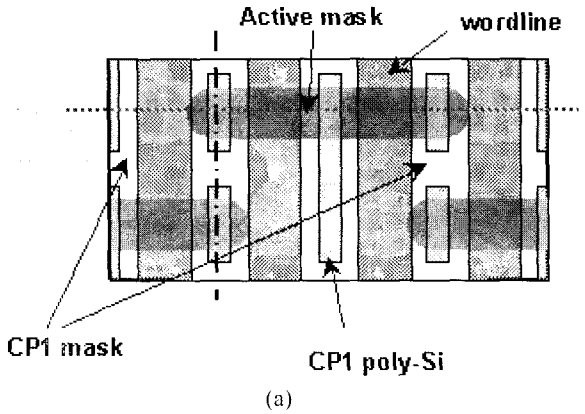


(d) CP2 poly-Si deposition and etch



(e) ILD deposition and CMP

Fig. 9. Process flow of cell formation using PPP(pre poly plug) scheme (W/L direction:A-A', B/L direction:B-B').



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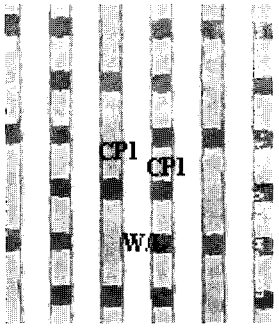

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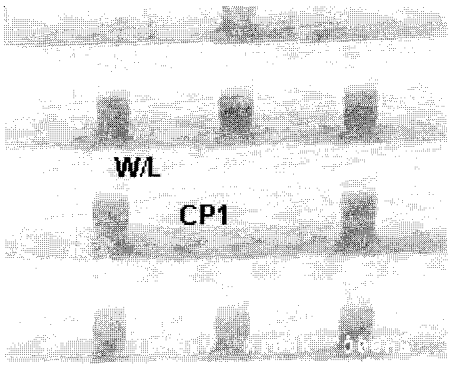
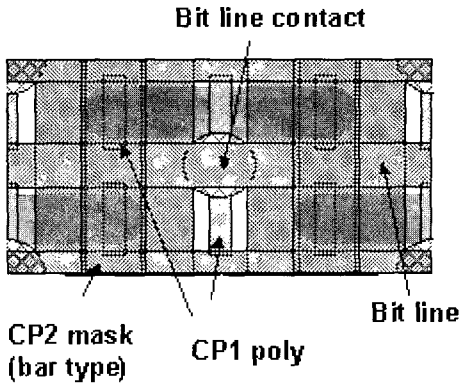


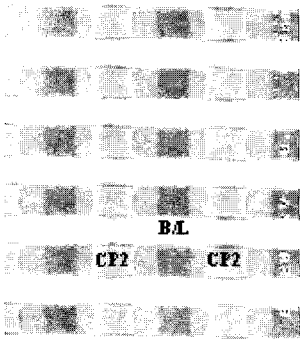
(c)

Fig. 10. (a) Schematic view of CP1 (cell pad) mask, (b and c) Planar SEM view of CP1 after fabrication.

poly-silicon gate, as shown in Fig. 16, no difference was observed. Fig. 17 shows the comparison of n^- to p-well cell junction leakage characteristics. The characteristics of W/WN_x/poly-silicon are comparable to those of the conventional W polycide gate. Fig. 18 compares the activation energy measured by the retention time characteristics versus temperature. The activation energy with W polymetal gate cells is also comparable to that of the conventional W polycide gate cells. These results also exhibits that the contamination by W gate is not a significant problem in our integration technology.



(a)



(b)

Fig. 11. (a) Schematic view of CP2(storage node contact) mask (b) Planar SEM view of CP1 and CP2 after fabrication.

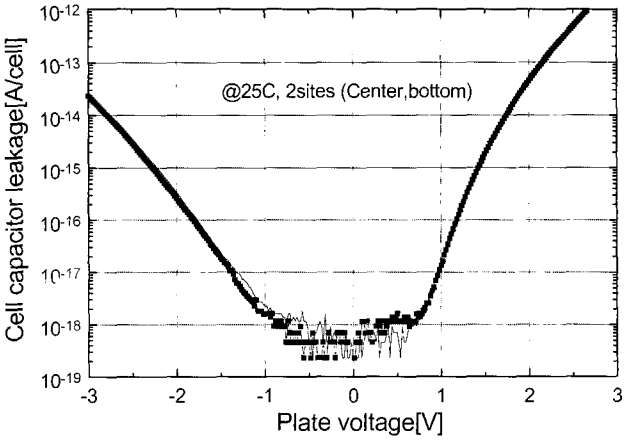


Fig. 12. Leakage characteristics of MIS(metal insulator Si)-Ta_2O_5 with rugged type inner surface(inner cylinder) . The capacitor leakage is 0.02 fA/cell and 0.3 fA/cell at 1.0 V and 1.26 V of plate voltage, respectively.

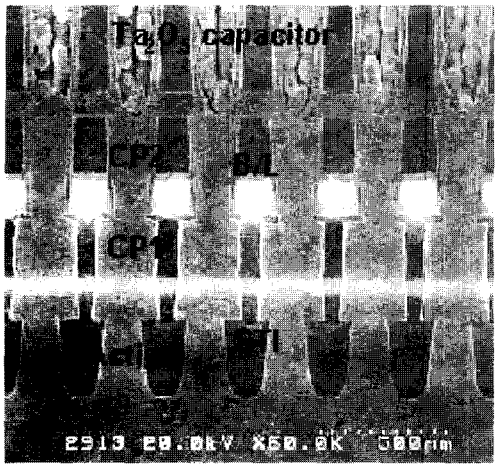


Fig. 13. Cross sectional SEM view of CP1(cell pad) and CP2 (storage node) in the direction of word line.

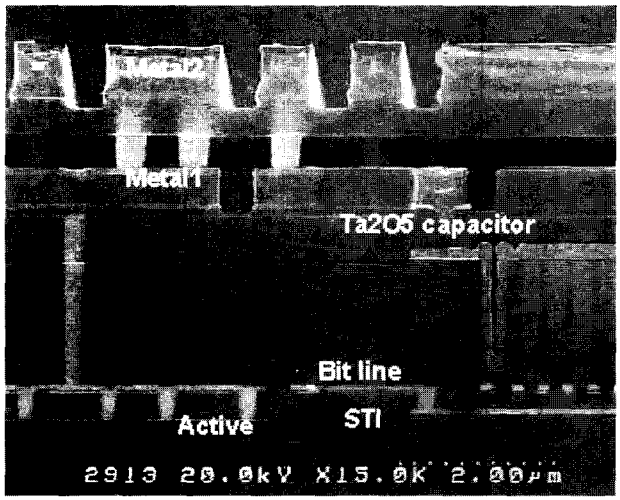


Fig. 14. Cross sectional SEM image of core and peripheral area of fabricated device.

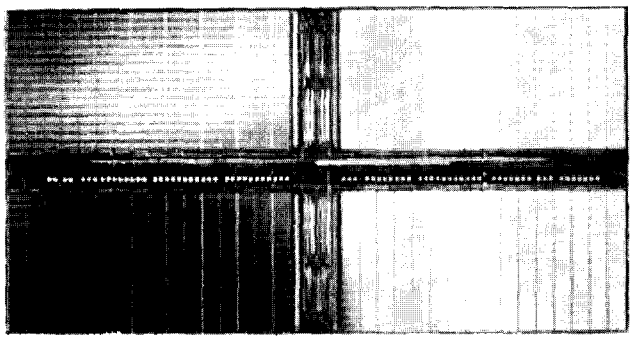


Fig. 15. Photograph of a fabricated 256Mbit DRAM.

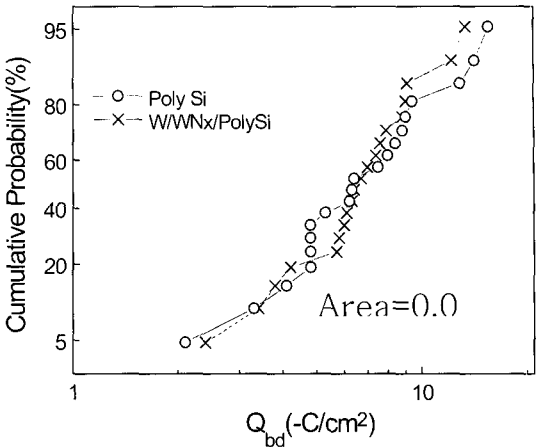


Fig. 16. Comparison of QBD characteristics of poly-silicon gate and W/WN_x/poly-silicon gate. They show comparable QBD characteristics.

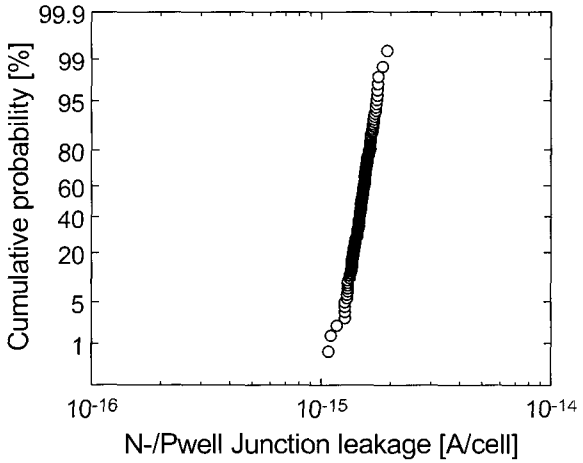


Fig. 17. Comparison of N-/Pwell junction leakage haracteristics of W polymetal gate and W polycide gate. They show comparable leakage characteristics.

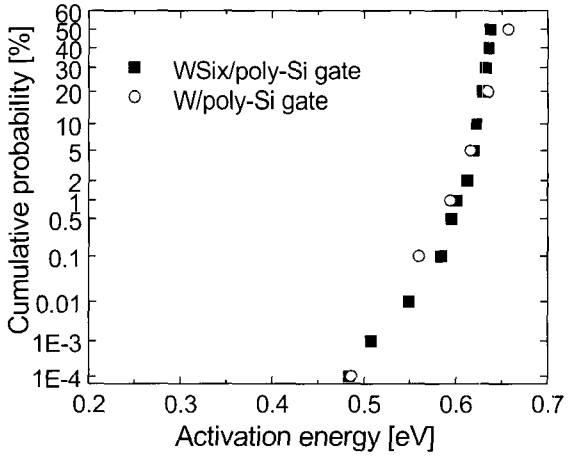


Fig. 18. Comparison of activation energy measured by retention time characteristics versus temperature. Activation energy of W/poly-silicon gate is also comparable to that of conventional WSix/poly-silicon gate.

IV. CONCLUSIONS

W polymetal gate technology for giga bit DRAM are presented. Key module processes for polymetal gate, which include etching, cleaning, and post oxidation are studied in detail. W/WN_x/poly-silicon adopted for a word line of 256Mbit DRAM has good gate oxide integrity and junction leakage characteristics through full integration, which is comparable to those of conventional WSi_x/Poly-silicon gate. These results undoubtedly show W/WN_x/poly-silicon is the strongest candidate as a word line for Giga bit DRAM.

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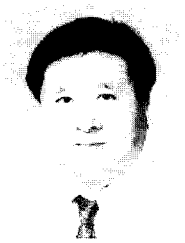

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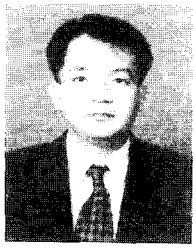

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