Characteristics of Si Nano-Crystal Memory

Kwangseok Han, Ilgweon Kim, and Hyungcheol Shin

Abstract—**We have developed a repeatable process of forming uniform, small-size and high-density self-assembled Si nano-crystals. The Si nano-crystals were fabricated in a conventional LPCVD (low pressure chemical vapor deposition) reactor at 620 °C for 15 sec. The nano-crystals were spherical shaped with about 4.5 nm in diameter and density of 5×10^{11} /cm^2.**

More uniform dots were fabricated on nitride film than on oxide film. To take advantage of the above-mentioned characteristics of nitride film while keeping the high interface quality between the tunneling dielectrics and the Si substrate, nitride-oxide tunneling dielectrics is proposed in n-channel device. For the first time, the single electron effect at room temperature, which shows a saturation of threshold voltage in a range of gate voltages with a periodicity of $\Delta V_{GS} \approx 1.7$ V, corresponding to single and multiple electron storage is reported.

The feasibility of p-channel nano-crystal memory with thin oxide in direct tunneling regime is demonstrated. The programming mechanisms of p-channel nano-crystal memory were investigated by charge separation technique. For small gate program -ming voltage, hole tunneling component from invers- ion layer is dominant. However, valence band elect-ron tunneling component from the valence band in the nano-crystal becomes dominant for large gate voltage.

Finally, the comparison of retention between programmed holes and electrons shows that holes have longer retention time.

Index Terms—**Nano-crystal, coulomb blockade, direct tunnelling, quantum dot, EEPROM.**

I. Introduction

It is expected that memory devices will be scaled down to the nanometer (=10^{-9} m) range in the future. Nanometer-scale devices utilizing the Coulomb blockade effect are promising candidates for becoming the basic elements of solid-state electronics. However, the fabrication of such devices demands cutting-edge nanolithography techniques. One way to create a nanometer range structure without the lithography technique is to use self-assembled nanocrystals. Recently, nanocrystal memory-cell structures with very thin tunnel oxide to increase the write/erase speed at the expense of retention time compared to flash electrically erasable and programmable read only memory (EEPROM) have been introduced [1]. Nanocrystal charge-storage sites embedded within the gate dielectric were proposed and demonstrated. The thin tunneling dielectric separates the inversion surface of a field-effect transistor (FET) from nanocrystals. An injection of an electron occurs from the inversion layer via direct tunneling when the control gate is forward biased with respect to the source and drain. The resulting stored charge effectively shifts the threshold voltage of the device.

The nanocrystal memory operates at low voltage compared to the conventional flash memory due to the thinner tunneling dielectrics since the spacing between the nanocrystals suppresses the charge loss through lateral paths. Therefore, a retention time longer than that expected in a floating-gate device as observed for such thin oxides [2].

The possibility of a charge-storage memory device, which exceeds the performance limits of a conventional floating-gate device, has attracted a great deal of interest and is spurring rapid progress in this area. Also, the devices are promising candidates for multibit storage memory-cells due to the possibility of single electron effects.

Single electron effects in fabricated nanocrystals at 77 K by Tiwari et al. [3] and in naturally formed grains were reported at room temperature by Yano et al. [4]. However, for practical application, room-temperature

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operation in nanocrystal memory is desirable but single electron effects in nanocrystal memory at room temperature have not been observed yet. In this study, we have developed a repeatable process for forming uniform, small and high-density Si nanocrystals on nitride/oxide stack tunneling dielectrics and have fabricated memory devices which exhibited room-temperature single electron effects for the first time. We report that the charging of a single electron to each nanocrystal at room temperature will lead to a quantized threshold voltage shift and a discrete charging voltage.

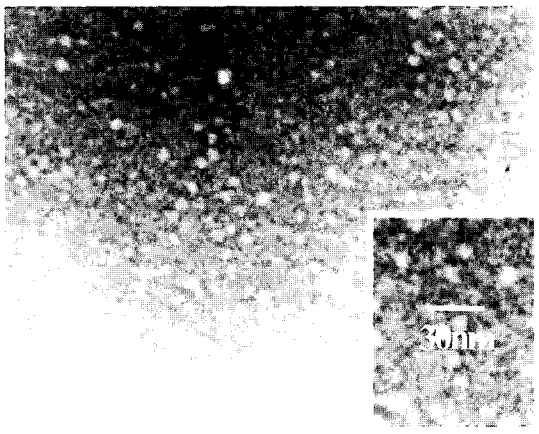
Since the energy barrier of about 4.7 eV for holes is larger than that of 3.1 eV for electrons between silicon and oxide, the Fowler-Nordheim (FN) tunneling component due to holes is many orders of magnitude smaller than electron tunneling component. Therefore, it is almost impossible to use p-channel EEPROM devices in FN tunneling regime. However, the difference between the gate tunneling current in NMOSFETs and PMOSFETs becomes smaller as the oxide thickness is scaled down into direct tunneling (DT) regime, which suggests the possibility of using Flash-type p-channel devices in DT regime [5], [6].

Therefore the programming speed of p-channel nano crystal memory can be comparable to that of n-channel device and it is feasible to use p-channel nano crystal memories in DT regime. In this paper, the various operation characteristics of p-channel nano-crystal memories are demonstrated.

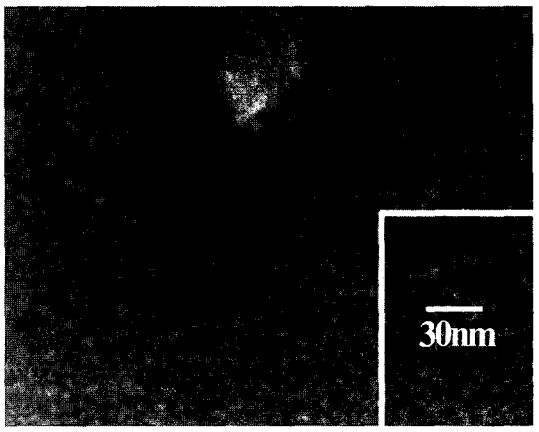
This paper is constructed as follows: Section II explains the method to fabricate nano-crystals and the effects of tunneling dielectrics on dot density and uniformity. Then section III explains the characteristics of nano-crystal memory. This section consists of two subsections. One shows the characteristics of n-channel nano-crystal memory, including the Coulomb blockade effects. The other explains the characteristics of p-channel nano-crystal memory, especially programming mechanism.

II. Device Fabrication

Fig. 1 shows a top-view scanning electron microscopy (SEM) image of the Si nanocrystals fabricated on a SiO_2 layer thermally grown by dry oxidation and a Si_3N_4 layer deposited by LPCVD. The nanocrystals were fabricated



(a)



(b)

Fig. 1. Top-view SEM image of Si nanocrystals on (a) thermally grown SiO_2 and (b) deposited Si_3N_4.

in a conventional LPCVD reactor using 50% SiH_4 in helium as a source gas at 620 °C for 15 sec. The nanocrystals were formed through spontaneous decomposition and assembly during the LPCVD process. A high dot density of about 5×10^{11} /cm^2 was obtained on a nitride surface, and the density is more than three times larger than that on oxide. More uniform dots were fabricated on nitride film than on oxide film, as shown in the atomic force microscopy (AFM) image of Fig. 2. The AFM image shows that the surface of Si_3N_4 is rougher than that of SiO_2. The rms roughness of the nitride film was 0.27 nm while that of the oxide film was 0.12 nm. If the surface is rougher, the area of the reactive site increases and the probability of surface reaction becomes higher.

Therefore, surface chemical reaction easily occurs. This indicates that the surface of Si_3N_4 is suitable for

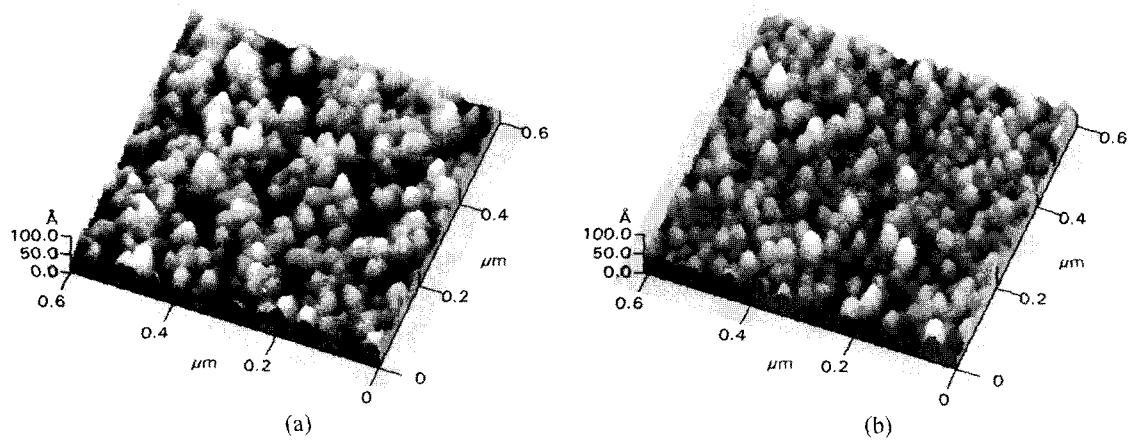


Fig. 2. AFM image of the Si nanocrystals. The dots on Si_3N_4 are more uniform than those on SiO_2. (a) SiO_2. (b) Si_3N_4.

more uniform nanocrystals with high density and small dimensions [7].

Fig. 3 shows the TEM image of fabricated nanocrystals. Spherical shaped Si dots of about 4.5 nm in diameter were obtained. After dot formation, 20 nm interlayer oxide was deposited. The Si dots that remained after gate etch step outside the channel region were removed by the following thermal oxidation step.

III. Electrical Characteristics and Discussions

A. *N-channel Nano-Crystal Memory*

To take advantage of the above-mentioned characteristics of nitride film while maintaining the high interface quality between the tunneling dielectrics and the Si substrate, nitride-oxide tunneling dielectrics is used in n-channel devices. The tunneling dielectrics is composed of 2 nm of Si_3N_4 deposited on 1 nm of SiO_2 thermally-grown. The native oxide was dry-etched by HF before 1 nm thermal oxidation, which was carried out at 850 °C. After thermal oxidation, 2 nm of nitride was deposited on oxide at 750 °C.

The current-voltage characteristics of a nanocrystal memory utilizing the fabricated Si nanocrystals were measured. Fig. 4 shows the operation characteristics of the memory devices with a drain bias of 0.1 V. For the maximum programming voltage of 5 V, the threshold voltage shift was about 0.5 V, which corresponds to about one electron programming per quantum dot [8].

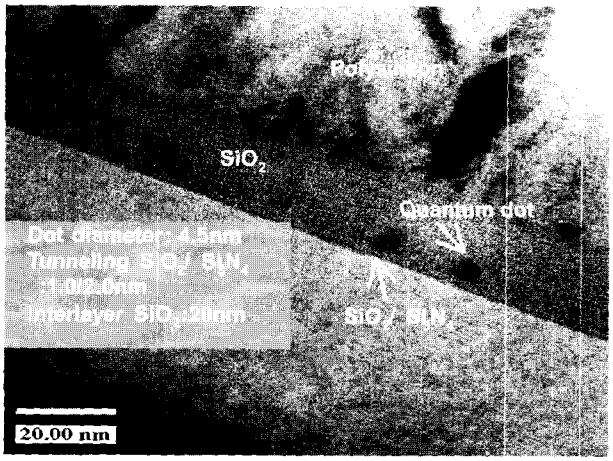


Fig. 3. TEM image of nano crystals. Spherical shaped Si dots of about 4.5 nm in diameter were obtained. The thickness of gate oxide and control oxide was 4nm and 20 nm, respectively.

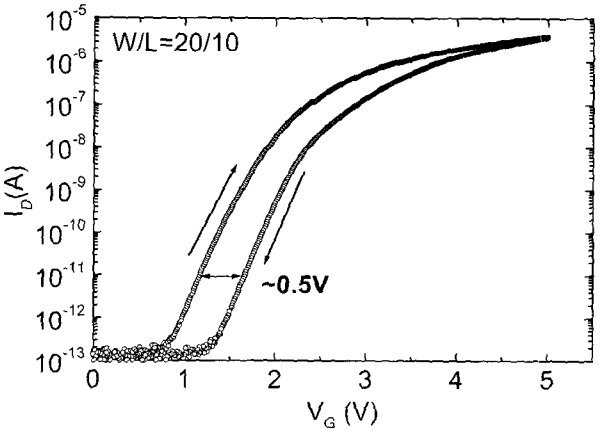


Fig. 4. Hysteresis characteristics of the memory with tunneling oxide-nitride.

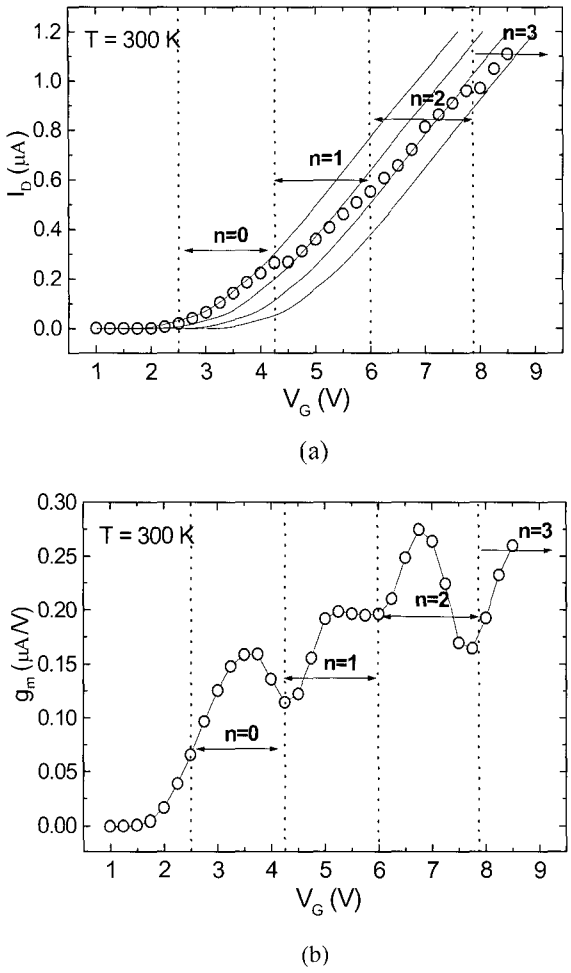


Fig. 5. The Coulomb blockade effect in a device with a tunneling NO layer. (a) Saturation drain current vs static gate bias applied for 10 s sufficient for full programming. Solid lines represent the I_D-V_G curve with zero, one, two or three electrons per quantum dot, respectively. Each region (n=0,1,2,3) represents zero, one, two or three electrons per dot, respectively. (b) The transconductance of the sampled drain current. Clear oscillation of the transconductance was observed.

To observe single electron charging of the nanocrystal, we measured the steady-state drain current after applying static gate bias for 10 sec, sufficient for full programming [Fig. 5(a)]. Each circle represents the data measured at room temperature. An important feature of these characteristics is the staircase plateauing of the steady-state drain currents with a periodicity of $\Delta V_{GS} \approx$ 1.7 V. For comparison, the lines in Fig. 5(a) represent the I-V curve with zero, one, two, and three electrons per dot. The curve with zero electrons per dot (n=0) was obtained by sweeping the I-V with very short pulses to avoid programming during the sweeping. The other I-V curves were obtained by shifting the I-V curve with no electrons by equidistant steps of the calculated ΔV_T value of 0.48 V. Comparison of the I-V curves with the data indicates that the single electron charging effect is observed at room temperature as electrons tunnel into the quantum dots. The first, second, and third electron transfers to the nanocrystal at gate voltages of about 4.2 V, 6.0 V, and 7.9 V, respectively. The relatively large voltage of 4.2 V for the first electron transfer is due to the large initial threshold voltage of 2.5 V, below which no electron transfer is possible. In Fig. 5(a), the measured data are parallel to the solid I-V curves for most of the gate voltages; this is the Coulomb blockade effect. A range of gate voltages with zero, one, two, and three electrons storage per nanocrystal is clearly observable.

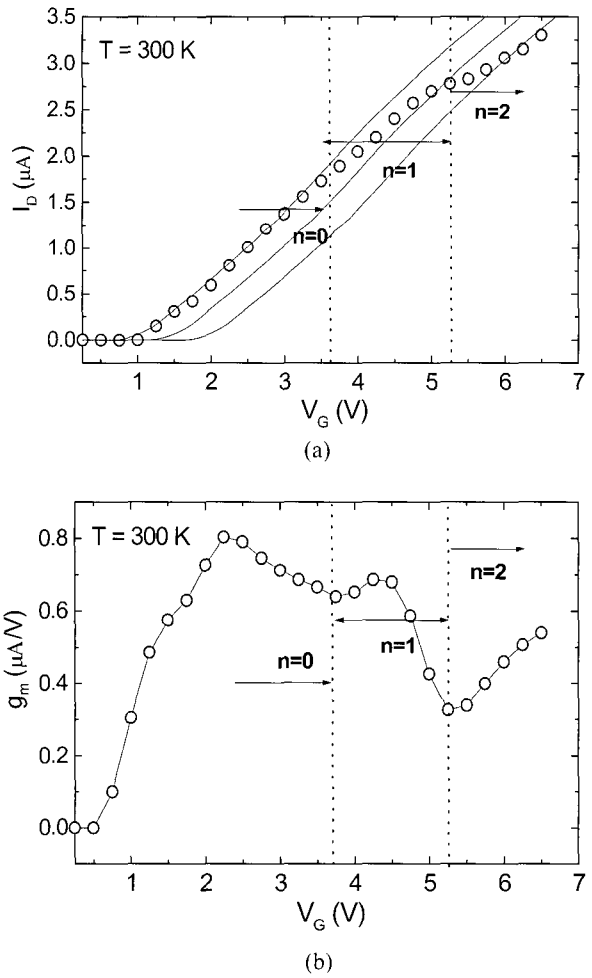
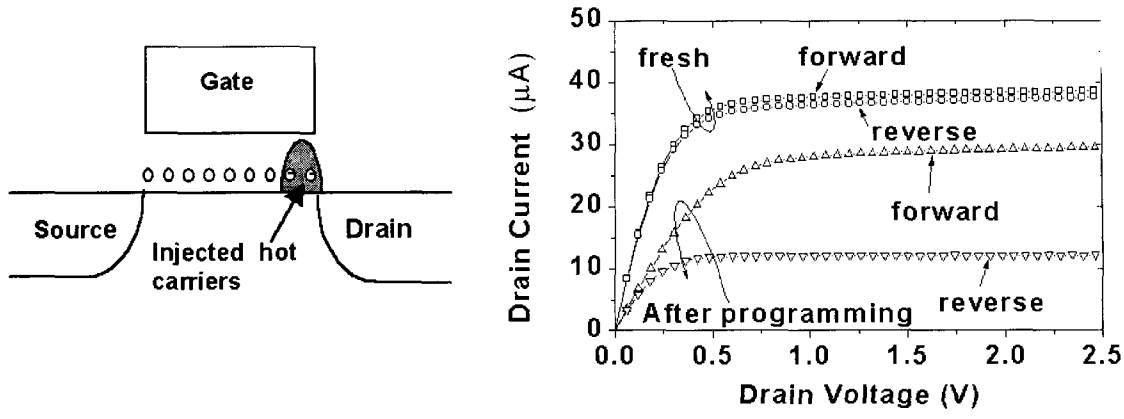


Fig. 6. The Coulomb blockade effect in a device with a tunneling oxide. (a) Saturation drain current vs static gate bias applied for 10 sec is sufficient for full programming. (b) The transconductance of the sampled drain current.



(a) (b)

Fig. 7. (a) Injected hot-carrier localization near the drain region. (b) Asymmetry of the I_D-V_D curve due to the localization of trapped hot carriers near the drain junction.

Also, the periodicity of the staircase plateaus ΔV_{GS} is calculated as follows. The required voltage increase of the control gate ΔV_{GS} for one electron charging into the dot is calculated by the following equation: ΔV_{GS} *=(quantum energy level spacing + charging energy)* $\cdot$ $(1+C_{tt}/C_{CG}) = 210\ mV \cdot (1+C_{tt}/C_{CG})$. Here, the gate-to-dot capacitance C_{CG} is calculated to be 0.17 μF/cm^2, and the dot-to-channel capacitance C_{tt} is calculated to be 1.26 μF/cm^2. Then ΔV_{GS} is calculated to be 1.8 V [9]. Since the measured periodicity of the staircase plateaus is about 1.7 V, the calculation is very close to the measurement data. Fig. 5(b) shows the transconductance ($\equiv \Delta I_D / \Delta V_G$) of the sampled drain current. The clear transconductance oscillation with the period of the single electron transfer confirms the discrete electron charging to dots due to the Coulomb blockade effect. The same measurement was carried out for the devices with dots fabricated on tunneling SiO_2 [Fig. 6]. The devices with quantum dots on SiO_2 also exhibited the same Coulomb blockade effect [Fig. 6(a)] and transconductance oscillation [Fig. 6(b)]. However, since the dots on tunneling oxide are less uniform than those on tunneling NO, the Coulomb blockade effect was not clearly observed in devices with tunneling oxide [10].

The physical separation of the nanocrystals limits the lateral flow of charge. During hot-carrier programming, the magnitude of the electric field is largest at the drain junction and most of the electrons are injected and captured into the dots near the drain junction [Fig. 7(a)].

Therefore, the stressed I-V curves measured after hot-carrier programming have asymmetry when the source and the drain are exchanged, as shown in Fig. 7(b). These asymmetric characteristics remained even after 2 h passed.

B. *P-Channel Nano-Crystal Memory*

4 nm thermal oxide was used as tunneling dielectrics. N^+ polysilicon was used for the gate. For comparison, devices without nano-crystal were also fabricated in same condition. To measure tunneling currents directly, the test patterns with area of 3.86×10^{-4} cm^2, which had source and drain connected together, were fabricated.

Fig. 8(a) shows the hystheresis characteristics of p-channel nano-crystal memory device. The fact that drain current during backward scan is smaller than that during forward scan indicates programming by positive charges. ΔV_T of about 0.7 V was observed for maximum voltage sweep of 6 V. However, no hysteresis was observed in control devices without nano-crystals. This characteristic indicates that the dots play the major role for charge storage, not the interface traps which may exist at the interface between the tunneling oxide and the interlayer oxide. Fig. 8(b) shows the steady state threshold voltage shift vs. programming gate voltage. The threshold voltage shift increased with the programming gate voltage for memory devices with nano-crystals, whereas no V_T shift was observed in control devices. This figure also shows corresponding electric field across the tunneling oxide. Since the programming mechanism is

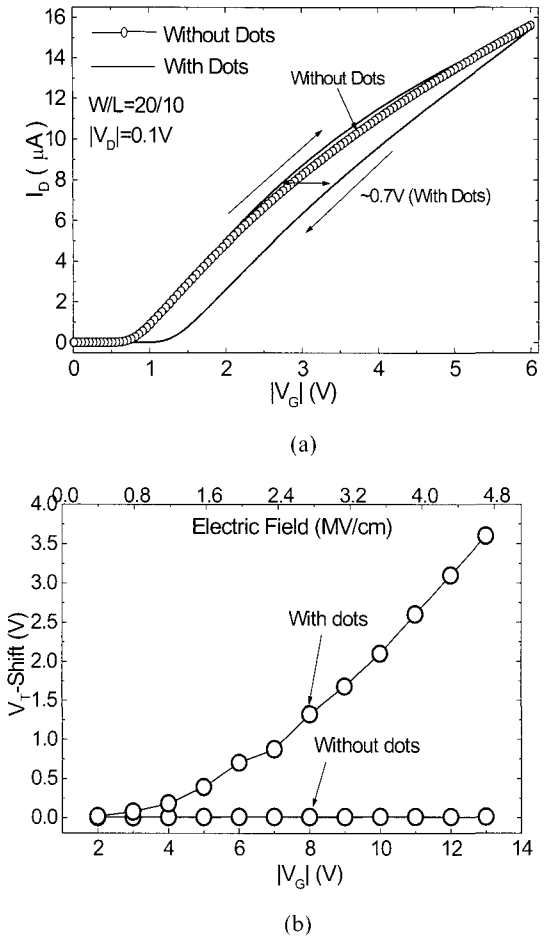


Fig. 8. Hysteresis characteristics of the p-channel nano crystal memory. No hysteresis was observed in control devices (a). The threshold voltage shift at steady state versus the programming voltage (b). These characteristics shows the dots play a major role to store charge, not the traps.

direct tunneling in thin oxide, the large threshold voltage shift is obtained with small electric field(~2.4 MV/cm).

Fig. 9 shows the measured drain current during programming. The drain current was shown in linear and logarithmic time scale. The voltages of $|V_G|$ = 8 V and $|V_D|$ = 0.1 V were used. A short and a long time constant were observed in these measurements, i.e., after an initial rapid change, the drain current changed slowly. The density of traps and defects at the internal/surface of silicon nanocrystals is enhanced due to large surface-to-volume ratios, and high surface roughness and compositional disorders [11]. The existence of two time-constant is indicative of possible role for interface states of dots, although the most injection occurs into the nano-crystals which has a large capture cross-section [12].

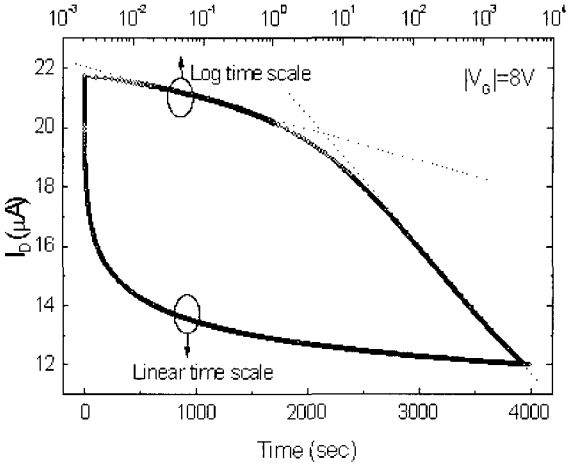


Fig. 9. Measured drain current during programming was showed in linear and logarithmic time scale. The drain current was decreased due to positive charge programming. The two time-constants were observed.

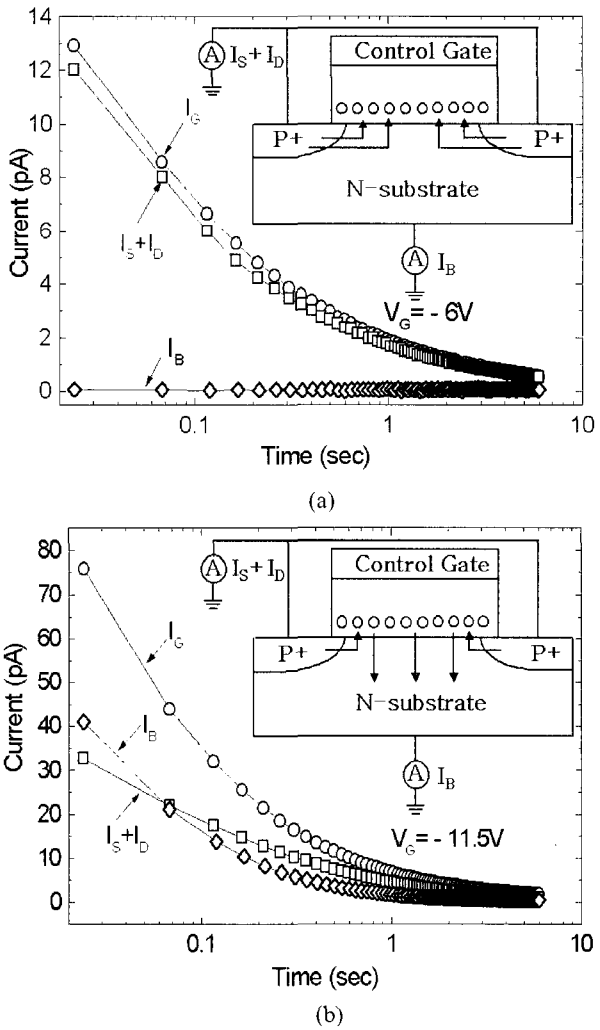


Fig. 10. Transient tunneling current during programming in time domain in MOS capacitor pattern for the gate constant voltage of (a) – 6 V and (b) – 11.5 V.

To investigate the programming mechanism of the p-channel nano-crystal memory, time-resolved charge separation technique was used. All terminal currents were measured at the same time with the MOS structure as shown in inset of Fig. 10 by using Semiconductor Parameter Analyzer HP4155. Fig. 10(a) shows the tunneling currents in time domain when the gate was biased to $|V_G| = 6$ V. The tunneling current was measured from 24 msec due to the limited resolution of measurement equipment. The size of the gate current was the same as the source/drain current while no body current was detected, which indicates that the holes in the channel region tunnel into dot during programming and there is no electron tunneling component from the dot into the substrate. The programming tunneling current decreased exponentially as programming procedure continued, which eventually reached zero after programming is complete. However, different behavior was observed at higher programming voltages. Fig. 10(b) shows the transient current at $|V_G| = 11.5$ V. In this case, significant amount of the body current flows during the programming in addition to the source/drain current. Each tunneling component was measured with different programming voltages. The body current started to be detected from $|V_G| = 9$ V and increased steadily with gate voltage. Below $|V_G| = 8$ V, the source/drain current was dominant and the body current was negligible [13], [14].

Fig. 11(a) shows the energy band diagram when the gate was biased to $|V_G| = 6$ V. The band gap of SiO_2 was assumed to be 8.9 eV and that of Si to be 1.1 eV. The tunneling barrier height of conduction band electron and hole are assumed to be 3.1 eV and 4.7 eV, respectively. For simplicity, the band gap of dots is assumed to be equal to that of silicon substrate, although the band gap of dots can be slightly larger than that of substrate due to three-dimensional quantum confinement effect [11]. The substrate doping concentration of $N_D = 10^{17}/cm^3$ and the oxide charge density of $10^{10}/cm^2$ was assumed. The mobile charges in dots were neglected. The surface potential of substrate was fixed at $2\phi_F = -2kT/q \cdot \ln(N_D/n_i)$. The energy barrier for the electrons in the conduction band of nano-crystal is lower than that for the holes in the inversion layer. However, since the nano-crystals are undoped, the number of electrons in the conduction band of the nano-crystals is so small that the electron tunneling is negligible. These facts were confirmed by zero body current as indicated in Fig. 10(a). Therefore, the hole tunneling from the channel into the dots is the dominant mechanism for programming with gate voltages less than 9 V. For gate voltage larger than 9 V, the band alignment is such that the valence band electrons in the nano-crystal can tunnel into the substrate, which causes the body current to flow [Fig. 11(b)]. Simple calculation also showed that the band alignment starts from $|V_G|=8$ V. For the case of conventional EEPROM, the minimum thickness of tunneling oxide is about 7 nm and the valence band electron tunneling current can be detected (≥ 10 pA) only with very high electric field larger than 10 MV/cm, which is close to oxide breakdown field.

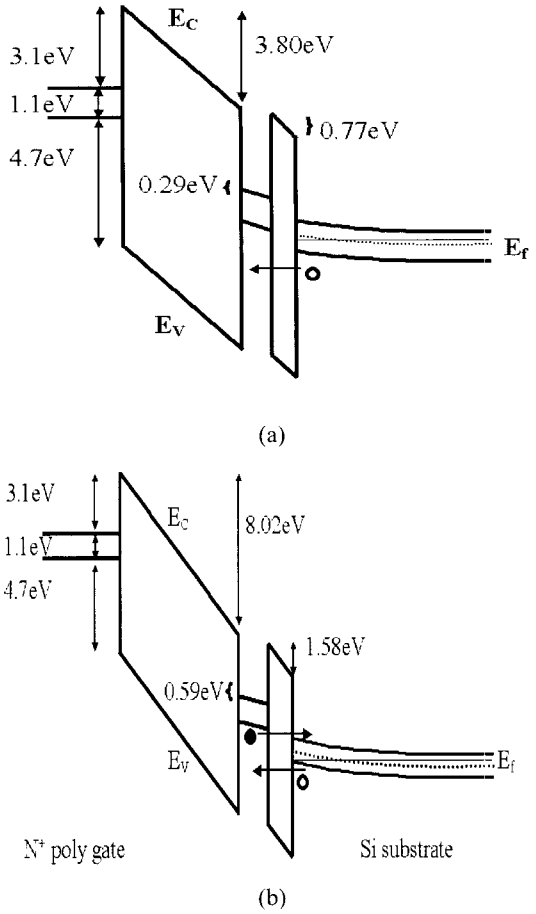


Fig. 11. Energy band diagram during programming when the gate is biased to –6 V (a) and –11.5 V (b). The substrate doping concentration of $N_D=10^{17}/cm^3$ and the oxide charge density of $10^{10}/cm^2$ was assumed. The tunneling barrier height of conduction band electron and hole is 3.1eV and 4.7eV, respectively.

Fig. 12 shows the endurance characteristics until 10^5 write/erase cycles. The pulses with ± 5 V amplitude were applied to the gate until 10^5 cycles. Direct tunneling results in the good endurance characteristics. The subthrehold slope was also extracted during the endurance test. The subthrehold slope did not change until 10^5 cycles, which indicated significant interface trapping and detrapping did not occur.

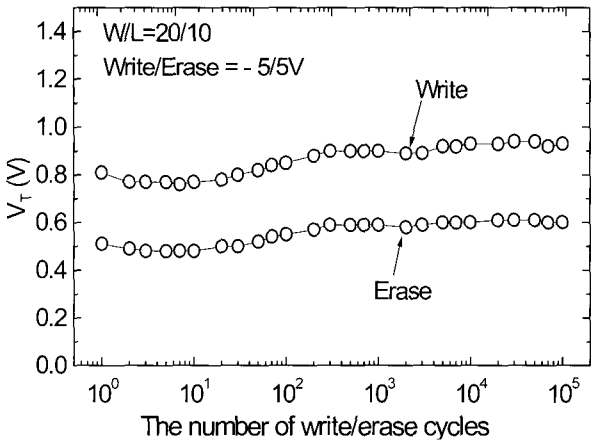


Fig. 12. Endurance characteristics until 10^5 write /erase cycles. Since low energy holes and electrons tunneled in direct tunneling regime, the memory was free from hot carrier degradation.

Fig. 13(a) shows the retention characteristics of the memory for write state and erase state. After holes were programmed from the inversion layer into dots with the gate voltage of −8 V, retention characteristics was measured. The hole-loss rate was observed to be 0.075 V/decade. The retention characteristics of electrons was also measured after erasing with the gate voltage of 8 V. The magnitude of the electron loss rate was 0.302 V/decade. Both the programmed charges (electrons and holes) tunneled back logarithmically with time. Fig. 13(b) shows that the loss rate of holes is about four to five times smaller than that of electrons. The small loss rate for holes results from the higher tunneling barrier [15].

IV. Conclusion

Spherical Si nanocrystals with a 4.5 nm average diameter and a density of $5\times10^{11}/cm^2$ on tunneling

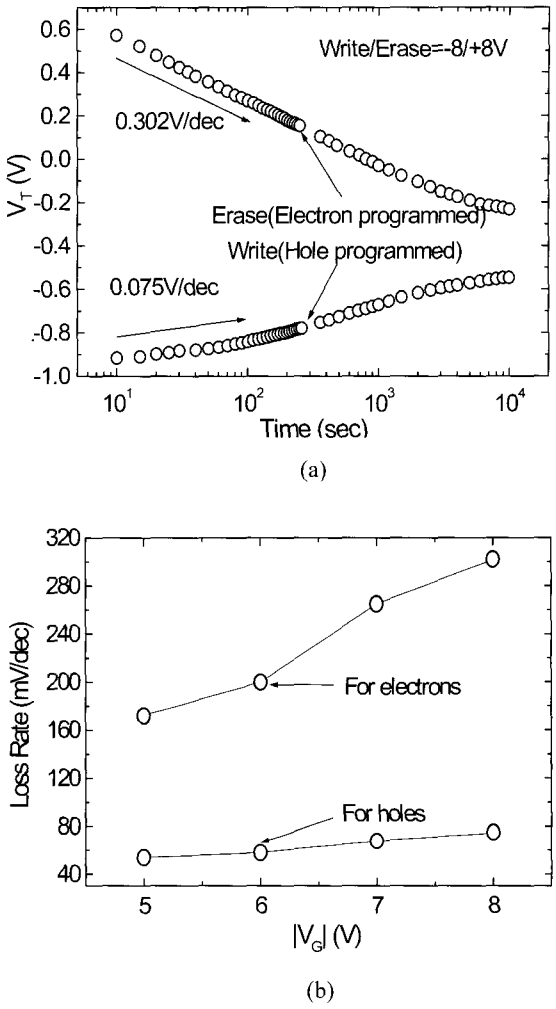


Fig. 13. Retention characteristics of programmed hole and electrons (a) and the loss rates of holes and electrons with various programming voltages (b). The loss rate of electrons is about four to five times larger than that of holes.

nitride/oxide stack dielectrics are fabricated by LPCVD at 620 °C for 15 sec. A nitride/oxide stack dielectrics provides uniform dots with higher dot density while maintaining an excellent interface along the channel.

We have demonstrated the room-temperature Coulomb blockade effect in nanocrystal memory for the first time. The quantized shift in threshold voltage and quantized charging voltage has been observed at room temperature, which is attributed to the single electron charging.

The programming mechanisms of p-channel nanocrystal memory were investigated by measuring the transient tunneling current directly. During programming, the tunneling mechanism changes from hole tunneling to valence band electron tunneling as the gate voltage

increases. The hole programming is advantageous compared to electrons in keeping the information longer. This proves the feasibility of p-channel nano-crystal memory.

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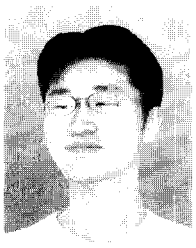
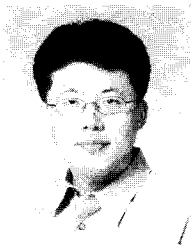


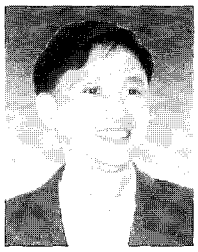
Kwangseok Han was born in Korea on December 6, 1976. He received the B.S. degree and the M.S. degree in Electrical Engineering and Computer Science at Korea Advanced Institute of Science and Technology (KAIST), Taejon, Korea, in 1998 and 2000, respectively. Now he pursuits the Ph.D. degree in same department and university. His current research activities include the characterization of nano-crystal memory and the noise modeling of RF CMOS.

He received the Best Student Award for the Outstanding Paper in the Silicon Technology on IEEE International Conference on VLSI and CAD in 1999. He received the splendor prize on IEEE Korea Council Student Paper Contest in 1999. In 2001, he also received the Second Best Paper Award from Applied Materials Korea (AMK).



Ilgweon Kim was born in Korea on October 21, 1965. He received the B.S. degree in Metallurgical engineering at Korea University, Seoul, Korea, in 1990 and the M.S degree in Electrical Engineering and Computer Science at Korea Advanced Institute of Science and Technology, Taejon, Korea, in 1998, respectively.

In 1990, he joined LG Semicon Company, Ltd., Cheongju-Si, Korea, where he was involved in Diffusion, LP CVD and Ion Implantation process for semiconductor device fabrication. In 1998, he joined the Hyundai Electronics Company, Ltd., Cheongju-Si, Korea. From 1998 to 1999, he was involved in the development of 0.2um technology DRAM's. Since 1999, he has been engaged in the development of 0.18um technology DRAM's. His research interests include the device design and the retention time for sub-micron technology DRAM's, nano-crystal memory. His current major activity is focused on the development and the transfer of mass production for DRAM's and derivatives using 0.18um technology.



Hyungcheol Shin received the B.S. degree (Magna Cum Laude) and the M.S. degree in Electronics Engineering from the Seoul National University, Seoul, Korea, in 1985 and 1987, respectively, and the Ph.D. degree in Electrical Engineering at the University of California, Berkeley, in 1993. Between 1994 and 1996, he was with Motorola Advanced Custom Technologies, as a senior device engineer. In 1996, He joined Department of Electrical Engineering and Computer Sciences at KAIST, Taejon, Korea in 1996 as an assistant professor and he was promoted to an associate professor in 1999. His current research interests include nano CMOS, CMOS RF modeling, and RF circuits. He has published over 130 technical papers in international journals and conference proceedings and also wrote one chapter in a Japanese book on plasma charging damage. He has served as a committee member of several international conferences, including IEEE Silicon Nanoelectronics Workshop and IEEE Symposium on Plasma-Process Induced Damage (P2ID). In 2000, Prof. Shin became a Senior Member of IEEE. He is also a lifetime member of IEEK.

He received the Second Best Paper Award from American Vacuum Society in 1991. He also received the Excellent Teaching Award from the Department of Electrical Engineering and Computer Sciences at KAIST in 1998. In 1999, he received The Haedong Paper Award from The Institute of Electronics Engineers of Korea (IEEK). He has been listed in the "Marquis Who's Who in the World" and "THE OUTSTANDING PEOPLE OF THE 20^{TH} CENTURY-Second Edition". He will also be listed in the "International Personality of the Year" in 2001.