Effect of Hydrogen Treatment on Electrical Properties of Hafnium Oxide for Gate Dielectric Application

Kyu-Jeong Choi, Woong-Chul Shin, and Soon-Gil Yoon

Abstract— **Hafnium oxide thin films for gate dielectric were deposited at 300℃ on p-type Si (100) substrates by plasma enhanced chemical vapor deposition (PECVD) and annealed in O_2 and N_2 ambient at various temperatures. The effect of hydrogen treatment in 4% H_2 at 350℃ for 30 min on the electrical properties of HfO_2 for gate dielectric was investigated. The flat-band voltage shifts of HfO_2 capacitors annealed in O_2 ambient are larger than those in N_2 ambient because samples annealed in high oxygen partial pressure produces the effective negative charges in films. The oxygen loss in HfO_2 films was expected in forming gas annealed samples and decreased the excessive oxygen contents in films as-deposited and annealed in O_2 or N_2 ambient. The CET of films after hydrogen forming gas anneal almost did not vary compared with that before hydrogen gas anneal. Hysteresis of HfO_2 films abruptly decreased by hydrogen forming gas anneal because hysteresis in C-V characteristics depends on the bulk effect rather than HfO_2/Si interface. The lower trap densities of films annealed in O_2 ambient than those in N_2 were due to the composition of interfacial layer becoming closer to SiO_2 with increasing oxygen partial pressure. Hydrogen forming gas anneal at 350℃ for samples annealed at various temperatures in O_2 and N_2 ambient plays critical role in decreasing interface trap densities at the Si/SiO_2 interface. However, effect of forming gas anneal was almost disappeared for samples annealed at high temperature (about 800℃) in O_2 or N_2 ambient.**

Index Terms— **Gate dielectrics, HfO_2, PECVD, hydrogen annealing, MOSFET.**

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I. INTRODUCTION

There is considerable interest in replacement dielectrics for SiO_2 in metal/oxide/semiconductor (MOS) devices with channel lengths below 100 nm. Conventional SiO_2 and oxynitrides will be phased out due to excessive leakage current and reliability concerns. Thus, high dielectric constant thin films offer potential for increased capacitance in physically thicker films, providing a possible way to reduce direct tunneling [1]. Due to their thermodynamic stability in contact with silicon, ZrO_2, HfO_2, and their silicates have attracted a lot of attention recently [2-4]. HfO_2, especially, has desirable properties such as high dielectric constant (~30), high heat of formation (271 kcal/mol), and relatively large band gap (5.86 eV) [5]. HfO_2 is also very resistive to impurity diffusion and intermixing at the Si interface because of its high density (9.68 g/cm^3) [5]. These properties make HfO_2 one of the most promising candidates for alternative gate dielectric application.

So far, HfO_2 thin films have been prepared by sputtering [6-7] and thermal chemical vapor deposition (CVD) [8]. Thermal CVD method has actually produced pertinent HfO_2 thin film quality at a temperature above 500℃ using $Hf[OC(CH_3)_3]_4$. The lower deposition temperature for HfO_2 films should be ensured to avoid the formation of SiO_2 at HfO_2/Si interface. Compared with thermal CVD method, the PECVD technique has an advantage that the deposition at low temperature is possible. It should be noted that a PECVD method for HfO_2 thin films has not been reported.

In this study, HfO_2 gate dielectric thin films were deposited at 300℃ on Si (100) substrates by plasma-enhanced chemical vapor deposition (PECVD) using $Hf[OC(CH_3)_3]_4$ precursor. Effects of hydrogen treatment

on physical and electrical properties of Pt/HfO_2/Si structures were evaluated.

II. EXPERIMENTAL

The HfO_2 films were deposited on p-type Si (100) substrates by PECVD in O_2 ambient at 300℃. The Hf[OC(CH_3)$_3$]$_4$ was vaporized in the bubbler kept at 30℃ and was carried to the reactor using argon as the carrier gas. The chamber was maintained at 1 Torr during deposition. The detailed deposition conditions for PECVD-HfO_2 are summarized in Table I. As-deposited samples were annealed at 600 to 800℃ for 3 min in O_2 and N_2 ambient in the RTA (rapid thermal anneal) chamber. The samples as-deposited and annealed at various temperatures in O_2 or N_2 ambient were treated in 4% hydrogen and 96 % nitrogen mixture gases at 350°C for 30 min. Pt top electrodes to measure the electrical properties were sputter deposited, patterned, and wet-etched using an aqua regia solution (1HNO_3: 9HCl: 10H_2O) at 100℃. The capacitor area for the MOS (Pt/HfO_2/Si) structure was 3.0×10^{-4} ㎠. After gate patterning, the backside of the samples was etched to expose silicon substrate and metallized with Pt to reduce the series resistance.

TABLE 1. Deposition conditions of HfO_2 thin films by PECVD

Parameter	Condition
Deposition temperature	300℃
Deposition pressure	1 Torr
RF power	40 W
Bubbling temperature of Hf[OC(CH_3)$_3$]$_4$	30℃
Ar gas flow rate of Hf source	100 sccm
O_2 gas flow rate	100 sccm
Deposition time	30 min
Substrate	*p*-type Si(100)
Rapid thermal annealing	O_2, N_2, 600~800℃, 3 min
Forming gas annealing	4% H_2, 350℃, 30 min

Physical thickness of HfO_2 thin film was measured using high-resolution transmission electron microscopy (TEM, CM20T/STEM, Philips). Carbon impurities included in HfO_2 thin films were analyzed using auger electron spectroscopy (AES, VG Scientific Microlab 310-D). The capacitance-voltage (C-V) curves of the MOS capacitor were measured using a HP4194A impedance/gain-phase analyzer. Capacitance equivalent oxide thickness (CET) was extracted from the accumulation capacitance at 1 MHz and quantum mechanical correction was not applied. Keithley 617 programmable electrometer was used for leakage current density characteristics.

III. RESULTS AND DISCUSSION

Figure 1 shows the high-resolution transmission electron microscopic (HR TEM) images of HfO_2 thin films as-deposited and annealed at 800℃ for 3 min in O_2 and N_2 ambient. The SiO_2 interfacial layers having about 19 Å thickness were formed at HfO_2/Si interface because, at the initial stage of deposition, Si substrates were exposed at O_2 ambient. The thickness of interfacial layers after RTA treatment in O_2 and N_2 ambient did

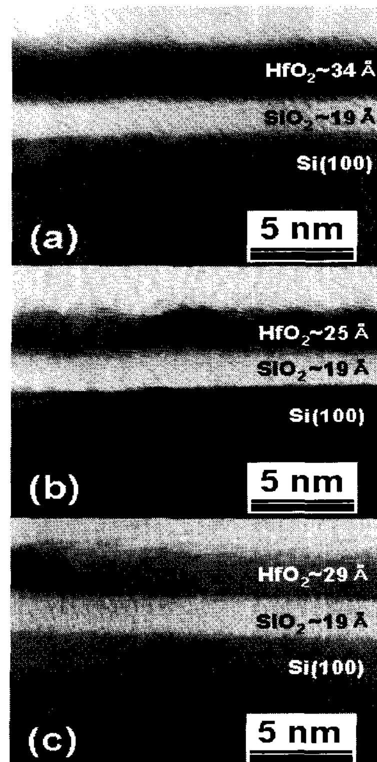
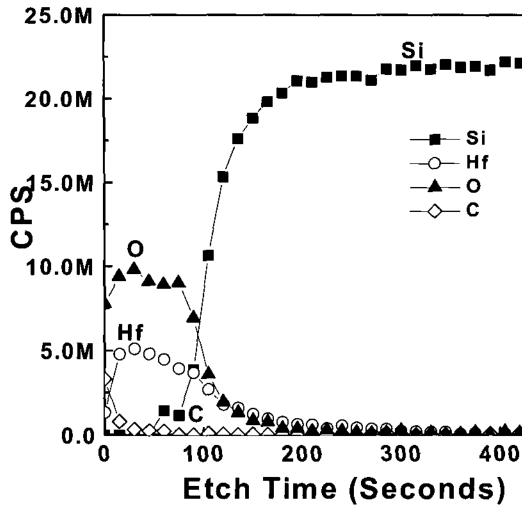


Fig. 1. TEM images of HfO_2 thin films (a) as-deposited, (b) annealed in O_2, and (c) in N_2 ambient at 800℃ for 3 min.



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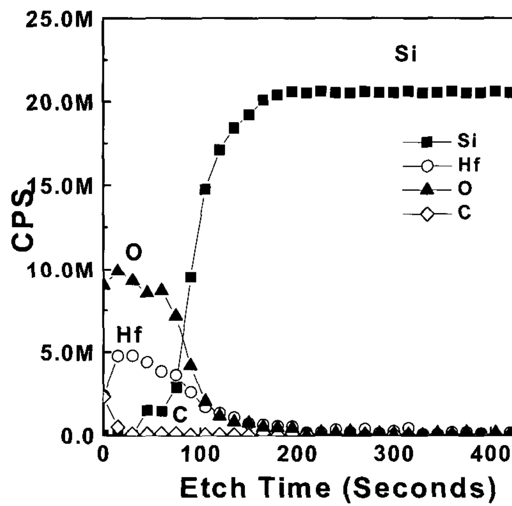

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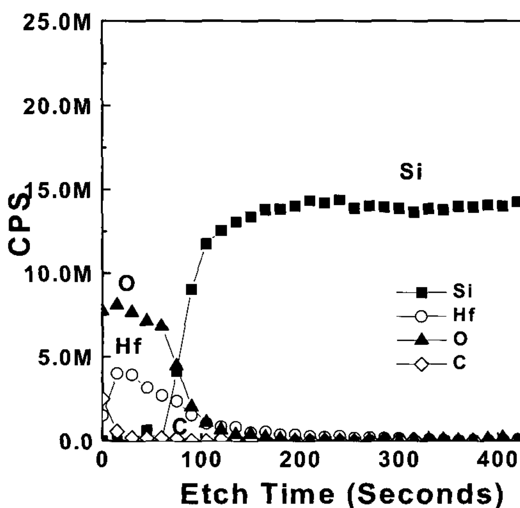


(c)

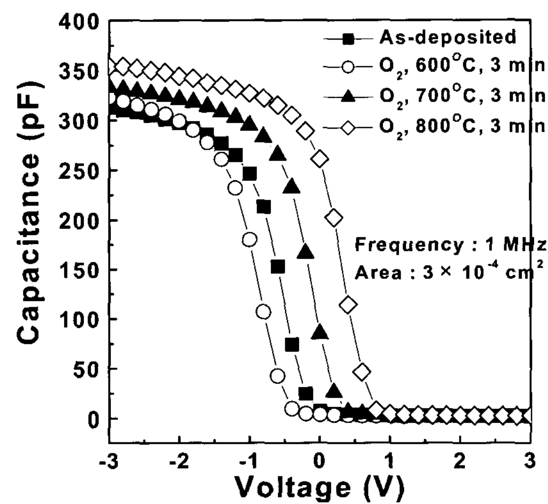
Fig. 2. AES depth profiles of HfO_2 thin films (a) as-deposited, (b) annealed in O_2, and (c) in N_2 ambient at 700°C for 3 min.

not change compared with as-deposited samples. Therefore, crystallization of HfO_2 films can exclude the impact on the interfacial layers during the annealing treatment in O_2 or N_2 ambient. The thickness of as-deposited HfO_2 thin films decreased in samples annealed at 800℃ in O_2 and N_2 ambient because HfO_2 had a high density. As-deposited HfO_2 films showed almost amorphous structure, but samples annealed in O_2 showed the increase of crystallinity compared with those in N_2 ambient at 800℃. The densification of pure oxide materials depends on annihilation of oxygen vacancies if volatile elements are absent in bulk materials. The densification rate of samples annealed in O_2 ambient is higher than that in N_2, resulting in higher crystallinity.

Figure 2 shows AES depth profiles of HfO_2 films as-deposited and annealed in O_2 or N_2 ambient at 700℃ for 3 min to analyze the carbon contamination in films. The deposition of films by PECVD using organometallic compounds produced the carbon contamination in films because PECVD was performed at low temperature. However, carbon contents at film surface were approximately 10 at. % and decreased abruptly with increasing depth in films. These results suggested that the carbon contamination came from the handling of samples. Even though PECVD was performed at low temperature, carbons dissociated from the precursors in plasma atmosphere are activated enough to react with oxygen and easily evaporated as carbon monoxide or carbon dioxide. Carbon contents in films as well as the surface of HfO_2 films annealed in O_2 or N_2 ambient are also low enough to be neglected.

Figure 3 shows capacitance-voltage characteristics of $Pt/HfO_2/Si$ structures annealed at various RTA temperatures in (a) O_2 and (b) N_2 ambient. The $Pt/HfO_2/Si$ structures showed clear accumulation, depletion and inversion regions. The capacitances of $Pt/HfO_2/Si$ structures increased with increasing annealing temperature because the thickness of HfO_2 thin films decreased. As-deposited HfO_2 films had excessive oxygen content compared with the stoichiometric composition from RBS analysis (not shown here). As shown in Fig. 3 (a), flat-band voltage shifts of HfO_2 capacitors annealed in O_2 ambient are larger than those in N_2 ambient (shown in Fig. 3 (b)). The excess oxygen concentration in HfO_2 films annealed in high oxygen partial pressure (in O_2 ambient) produced

the effective negative charges coming from excessive oxygen interstitial defects and they increased with increasing annealing temperature, resulting in large shift to positive side of flat-band voltage. However, flat-band voltages of HfO_2 films annealed at 600℃ in O_2 and N_2 ambient were shifted to negative side compared with those of as-deposited films. Further work is underway to elucidate the nature of these results. In case of samples annealed in N_2 ambient (in low oxygen partial pressure), the effective positive charges by oxygen vacancies increased with increasing annealing temperature and were compensated by effective negative charges. In



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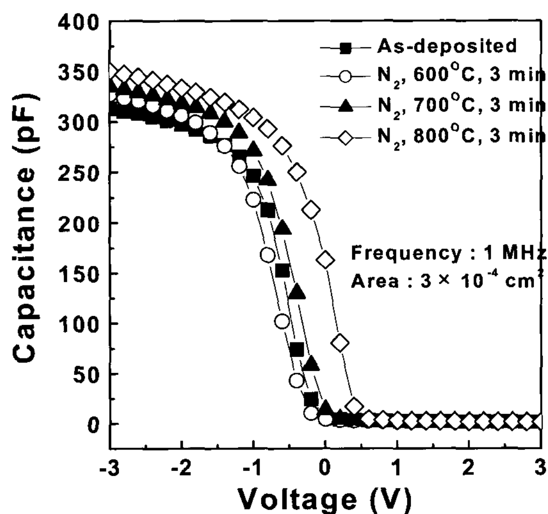
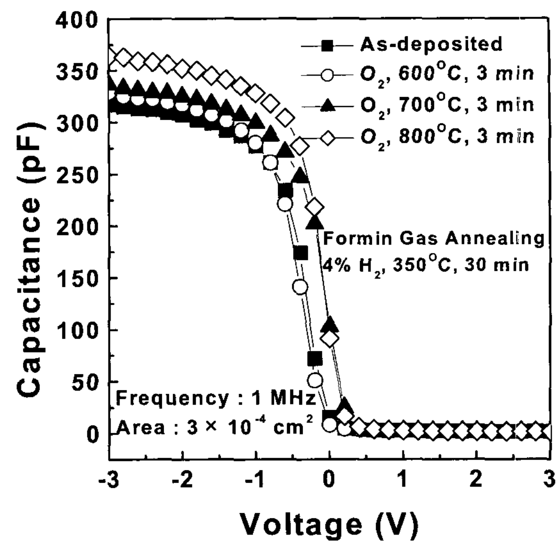


(b)

Fig. 3. Capacitance-voltage characteristics of $Pt/HfO_2/Si$ structures annealed at various RTA temperatures in (a) O_2 and (b) N_2 ambient.

order to elucidate the impact of oxygen defects in HfO_2 films on C-V characteristics, samples annealed in O_2 and N_2 ambient at various temperatures were annealed at 350℃ for 30 min in 4 % H_2 ambient.



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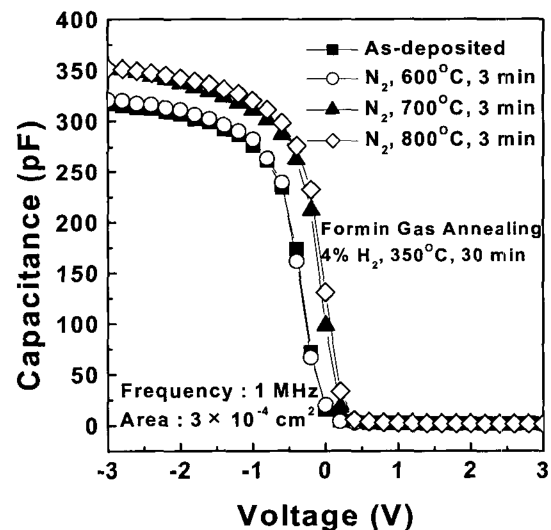


(b)

Fig. 4. Capacitance-voltage characteristics of Fig. 3 samples annealed in 4 % H_2 ambient at 350°C for 30 min.

Figures 4 (a) and (b) showed capacitance-voltage characteristics of $Pt/HfO_2/Si$ structures annealed in 4 % H_2 ambient at 350°C for 30 min. The oxygen partial pressure due to the reducing ambient created by forming gas is about 10^{-16} Torr. The oxygen loss in HfO_2 films was expected in forming gas annealed samples and decreased the excessive oxygen contents in films as-

deposited and annealed in O_2 or N_2 ambient. Therefore, shifts of flat-band voltage were abruptly decreased in forming gas annealed samples.

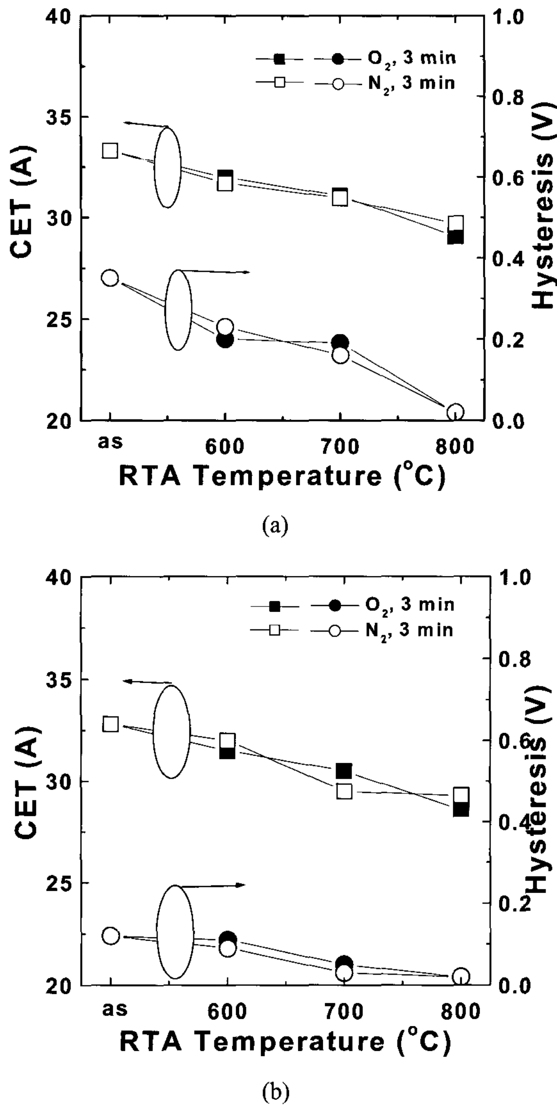


Fig. 5. Capacitance equivalent oxide thickness and hysteresis of Pt/HfO_2/Si structures (a) annealed at various RTA emperatures in O_2 and N_2 ambient and (b) annealed samples of Fig. 5 (a) in 4% H_2 at 350℃ for 30 min.

Figure 5 (a) shows the variations of capacitance equivalent oxide thickness (CET) and hysteresis of Pt/HfO_2/Si structures as a function of annealing temperature in O_2 and N_2 ambient. The CET of HfO_2 thin films slightly decreased with increasing annealing temperature and showed about 30Å in samples annealed at 800℃ in N_2 and O_2 ambient. Hysteresis in C-V curves needs to be minimized for high-k materials. The counterclockwise hysteresis of C-V curve is believed to be due to charge trapping at the negative gate bias. Hysteresis of as-deposited gate dielectric is quite large, but rapidly decreases with increasing RTA temperature in O_2 and N_2 ambient. The hysteresis in samples annealed at 800℃ in O_2 and N_2 was reduced to a negligible level of about 20 mV. Figure 5 (b) shows capacitance equivalent oxide thickness (CET) and hysteresis of Pt/HfO_2/Si structures annealed in 4 % H_2 ambient at 350℃ for 30 min. The CET of films after hydrogen forming gas anneal almost did not vary compared with that before hydrogen gas anneal because capacitance of films did not depend on hydrogen forming gas anneal at low temperature. Hysteresis of HfO_2 films abruptly decreased by hydrogen forming gas anneal because hysteresis in C-V characteristics depends on the bulk effect rather than HfO_2/Si interface. Oxygen loss by hydrogen forming gas anneal in HfO_2 films having excessive oxygen contents decreases the effective negative charges produced by excessive oxygen interstitial defects, resulting in decreasing the hysteresis of HfO_2 films.

Interface trap densities of Pt/HfO_2/Si structures were measured by a high frequency method developed by Terman.[9] The method relies on C-V measurement at a sufficiently high frequency that interface traps are assumed not to respond to the ac probe due to response to the varying dc voltage, causing the C-V curve to stretch out along the voltage axis. Figure 6 shows the variation of trap densities of samples annealed at various temperatures in O_2 and N_2 ambient and annealed at 350℃ in 4 % H_2 ambient for 30 min. The interface trap densities of HfO_2 thin films abruptly decrease with increasing RTA temperature in O_2 and N_2 ambient. The lower trap densities of films annealed in O_2 ambient than those in N_2 were due to the composition of interfacial layer becoming closer to SiO_2 with increasing oxygen partial pressure. A low-temperature forming gas anneals ties up dangling bonds at the Si/SiO_2 interface, thus reducing trap sites. As shown in Fig. 6, hydrogen forming gas anneal at 350℃ for samples annealed at various temperatures in O_2 and N_2 ambient plays critical role in decreasing interface trap densities at the Si/SiO_2 interface. However, effect of forming gas anneal was almost disappeared for samples annealed at high

temperature (about 800℃) in O_2 or N_2 ambient. This result suggested that the Si/SiO_2 interface annealed at 800℃ in O_2 or N_2 ambient showed a stable state without dangling bonds. Interface trap density of HfO_2 thin films annealed at 800℃ in O_2 was about 5.5×10^{11} $cm^{-2}eV^{-1}$. The interface trap densities of HfO_2 films by PEMOCVD are competed with those reported by reactive sputtering [10].

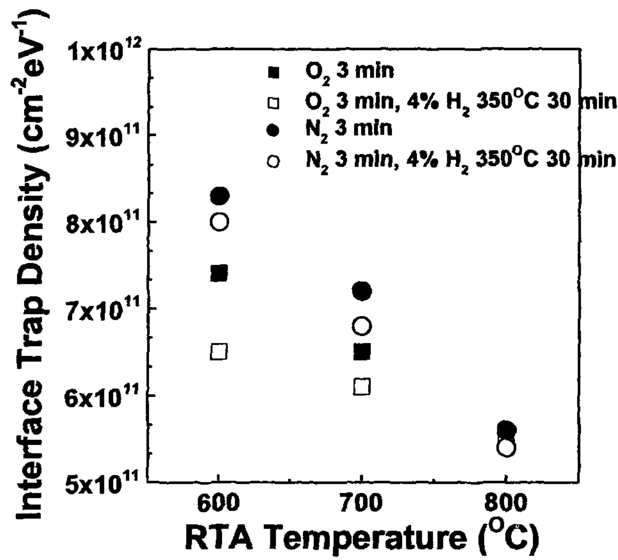
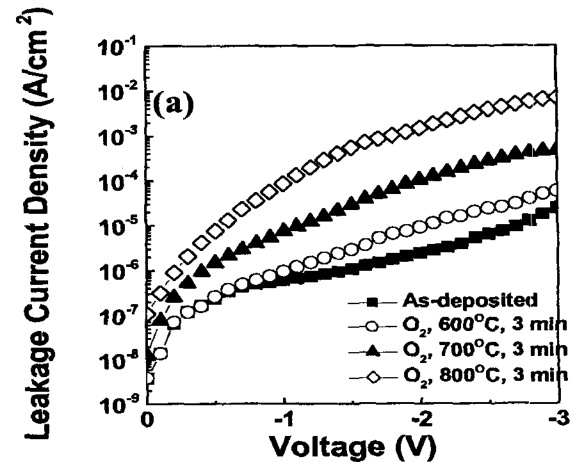


Fig. 6. Interface trap densities of $Pt/HfO_2/Si$ structure annealed at various RTA temperatures in O_2 and N_2 ambient and annealed at 350℃ in 4 % hydrogen forming gas.

The leakage current characteristics of $Pt/HfO_2/Si$ structure annealed in O_2 and N_2 ambient were shown in Fig. 7. The leakage current densities of the films increased with increasing annealing temperatures in O_2 and N_2 ambient. The leakage current densities of films annealed at 800℃ in O_2 and N_2 were about 8×10^{-5} and 3×10^{-6} A/cm^2 at −1 V, respectively. The higher leakage current densities of films annealed in O_2 ambient than those in N_2 were due to the increase of crystallinity of HfO_2 films, as shown in Fig. 1. Figure 8 shows the variation of leakage current densities of samples annealed in hydrogen ambient at 350℃. The leakage current densities were abruptly increased by hydrogen forming gas anneal because oxygen loss in HfO_2 films during forming gas anneal increases oxygen vacancies and then increases charge carriers such as electron to achieve the charge neutrality.



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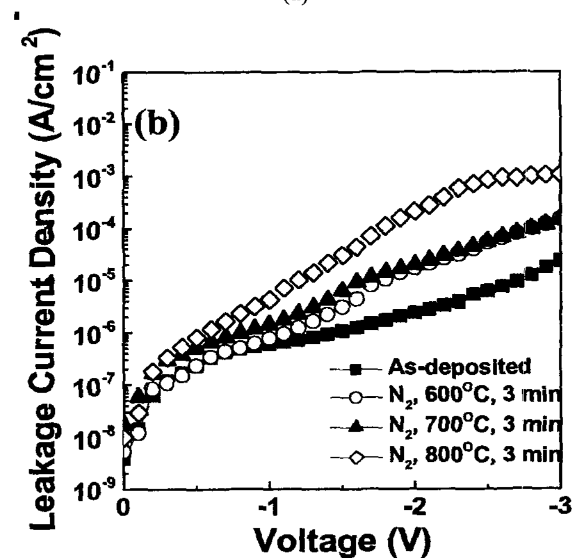
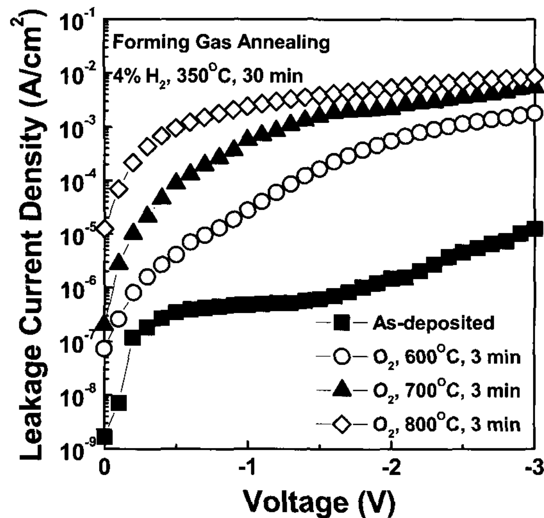


b)

Fig. 7. Leakage current densities of $Pt/HfO_2/Si$ structure annealed at various RTA temperatures in (a) O_2 and (b) N_2 ambient.

IV. Conclusion

Hafnium oxide thin films for gate dielectric were deposited at 300℃ on p-type Si (100) substrates by plasma enhanced chemical vapor deposition. The effect of hydrogen treatment in 4% H_2 at 350℃ for 30 min on the electrical properties of HfO_2 for gate dielectric was investigated. As-deposited HfO_2 films showed almost amorphous structure, but samples annealed in O_2 showed the increase of crystallinity compared with those in N_2 ambient at 800℃. The flat-band voltage shifts of HfO_2



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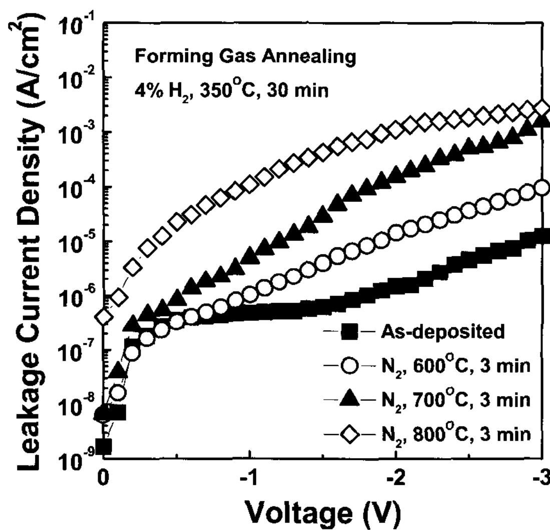

(b)

Fig. 8. Leakage current characteristics of Fig. 7 samples annealed at 350℃ in 4 % hydrogen forming gas.

capacitors annealed in O_2 ambient are larger than those in N_2 ambient because samples annealed in high oxygen partial pressure produces the effective negative charges in films. The oxygen loss in HfO_2 films was expected in forming gas annealed samples and decreased the excessive oxygen contents in films as-deposited and annealed in O_2 or N_2 ambient. Therefore, shifts of flat-band voltage were abruptly decreased in forming gas annealed samples. The CET of films after hydrogen forming gas anneal almost did not vary compared with that before hydrogen gas anneal because capacitance of films did not depend on hydrogen forming gas anneal at low temperature. Hysteresis of HfO_2 films abruptly decreased by hydrogen forming gas anneal because hysteresis in C-V characteristics depends on the bulk effect rather than HfO_2/Si interface. Oxygen loss by hydrogen forming gas anneal in HfO_2 films having excessive oxygen contents decreases the effective negative charges produced by excessive oxygen interstitial defects, resulting in decreasing the hysteresis of HfO_2 films. The lower trap densities of films annealed in O_2 ambient than those in N_2 were due to the composition of interfacial layer becoming closer to SiO_2 with increasing oxygen partial pressure. Hydrogen forming gas anneal at 350℃ for samples annealed at various temperatures in O_2 and N_2 ambient plays critical role in decreasing interface trap densities at the Si/SiO_2 interface. However, effect of forming gas anneal was almost disappeared for samples annealed at high temperature (about 800℃) in O_2 or N_2 ambient. The leakage current densities were abruptly increased by hydrogen forming gas anneal because oxygen loss in HfO_2 films during forming gas anneal increases oxygen vacancies and then increases charge carriers such as electron to achieve the charge neutrality.

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REFERENCES

[1] G. D. Wilk and R. M. Wallace, Appl. Phys. Lett. **74**, 2854 (1999).

[2] B. H. Lee, L. Kang, W. J. Qi, R. Nieh, Y. Jeon, K. Onishi, and J. C. Lee, Tech. Dig. Int. Electron Devices Meet. 133 (1999).

[3] G. D. Wilk and R. M. Wallace, *Appl. Phys. Lett.* **76**, 112 (2000).

[4] G. D. Wilk, R. M. Wallace, and J. M. Anthony, J. Appl. Phys. **87**, 484 (2000).

[5] M. Balog, M, Schieber, M. Michman, and S. Patai, *Thin Solid Films*, **41**, 247 (1977).

[6] L. Kang, K. onishi, Y. Jeon, B. H. Lee, C. Kang, W. Qi, R. Nieh, S. Gopalan, R. Choi, and J. C. Lee, Tech. Dig. Int. Electron Devices Meet. 35 (2000).

[7] B. H. Lee, R. Choi, L. Kang, S. Gopalan, R. Nieh, K. Onishi, Y Jeon, W. Qi, C. Kang, and J. C. Lee, Tech. Dig.

Int. Electron Devices Meet. 39 (2000).

[8] S. J. Lee, H. F. Luan, W. P. Bai, C. H. Lee, T. S. Jeon, Y. Senzaki, D. Roberts, and D. L. Kwong, Tech. Dig. Int. Electron Devices Meet. 31 (2000).

[9] L. M. Terman, *Solid-State Electron*, **5**, 285 (1962).

[10] L. Kang, B.H. Lee, W. J. Qi, and J. C. Lee, *IEEE Electr. Dev. Lett.* **21**, 181 (2000).

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