The 2-dimensional Discharge Cell Simulation for the Analysis of the Peset and Addressing of an Alternating Current Plasma Display Panel

Joong Kyun Kim, *Student Member*, Woo Jun Chung, Jeong Hyun Seo, *Student Member* and Ki Woong Whang, *Member*

Abstract

The characteristics of the reset and the address discharges of an alternating current Plasma Display Panel (ac PDP) were studied using 2-dimensional numerical discharge cell simulation. We investigated the wall charge variations during the reset discharge adopting ramping reset pulse and the subsequent addressing discharge. The roles of the ramping reset scheme can be divided into two stages, each electrode gathers wall charges during ramping-up of the initial stage and the built-up wall charges are lost during ramping-down of the later stage. Address discharge does not only change the wall charge distributions on the address and the scan electrodes but also on the sustain electrode. The increase in the wall charges on the sustain electrode was observed with the variation of the applied voltage to the sustain electrode during the address period. The increase of the applied voltage to the sustain electrode during the address period is expected to induce the decrease of the sustain voltage during the display period.

Keywords : Ac PDP, wall charge, ramping reset pulse, address discharge

1. Introduction

Alternating current Plasma Display Panel (ac PDPs) is a prominent candidate for the large size, wall hanging flat panel display. The gray scale in an ac PDP is expressed through the sub-field method. A single TV frame consists of several (8~12) sub-fields, and the reset and the address period precede the display period to ensure uniformity of the wall charge states of the cells and discharge selection. During the display period, the plasma in each selected display cell produces Vacuum Ultraviolet (VUV) rays to activate phosphor layers. The sustain electrode and the scan electrodes of a coplanar ac PDP are covered with glassy material to limit the discharge current, and the address electrode, covered with phosphor layers, runs orthogonal to the coplanar electrodes. During the address period, the display data are applied to selected cells through the address electrodes, which are put on the opposite glass plate. The wall charge states of the display cells at the addressing time depend on the discharge history of the previous sub-field. To reduce address-failure without regard to the discharge history, a wall voltage set-up period or a reset period is required before addressing.

Due to the complex characteristics of the discharge in a small volume, it is difficult to predict the precise operation characteristics of an ac PDP. In recent years, various reset schemes for the wall charge set-up were reported but detailed analysis of the mechanism of the reset scheme are as yet insufficient [1-2]. In this study, we investigated the mechanism of the reset scheme with the ramping reset pulse through a 2-dimensional numerical simulation. We can only observe the light emission and current flows containing the displacement component in the experiment. To understand the variations in the wall charges on each electrode, the information on the discharge currents into each electrode is required and a numerical simulation is a useful method to obtain the wall charge information.

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2. Description of the Simulation

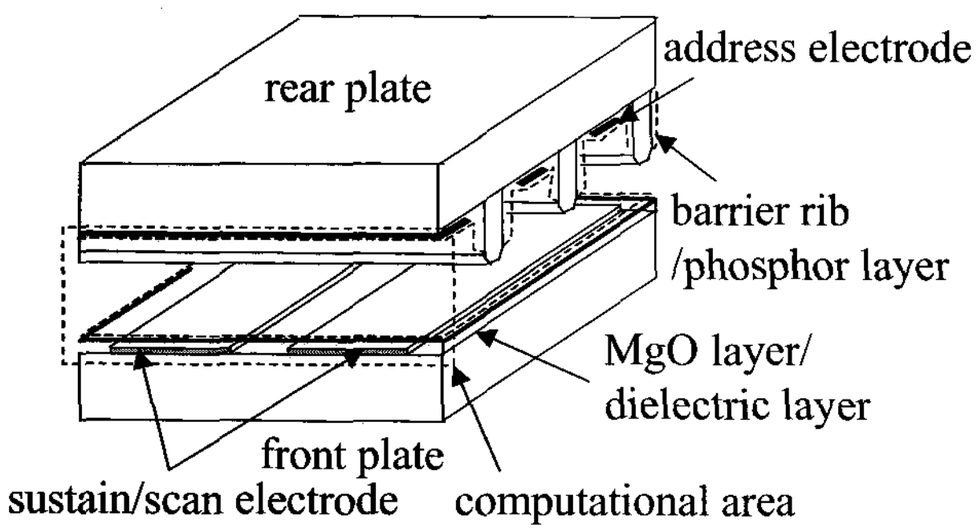


Fig. 1. Schematic diagram of coplanar three electrode ac PDP and calculation domain in the 2-dimensional simulation.

Fig. 1 shows the conventional coplanar three-electrode ac PDP cell structure and computational area used for numerical simulation. The gap between the sustain and the scan electrode is 60 μm, and the width of the sustain/scan electrode is 200 μm. A periodic discharges are assumed along the sustain and the scan electrode in the 2 dimensional simulation. The upper and the lower glass plates are separated by barrier ribs of 150 μm in height and filled with a Ne-3 %Xe mixture gas of 500 torr. The secondary electron emission coefficients (γ_i) of the magnesium oxide layer were assumed to be 0.8 for He ions, 0.2 for Ne ions and 0.05 for Xe ions, and those of the phosphor layer to be 0.27 for He ions, 0.067 for Ne ions and 0.0167 for Xe ions according to the experimental results. The detailed method for γ_i value observation can be found in references [3] and [4]. The γ_i value of the phosphor layer plays an important role when ions impinge on the layer, i.e. when the phosphor layer participates in the discharge as a cathode, by supply electrons to enhance the discharge. The simulation model consists of Poisson, continuity, and drift-diffusion equations. The set of equations for electrone, *e* and ion, *i*, respectively, are as follows;

$$\nabla\cdot(\varepsilon\vec{E}) = e(n_i - n_e)$$

$$\frac{\partial n_{e,i}}{\partial t} + \nabla\cdot(n_{e,i}\vec{v}_{e,i}) = S_{e,i}$$

$$\frac{\partial M}{\partial t} = D_M\nabla^2 M + S_M$$

$$n_{e,i}\vec{v}_{e,i} = -n_{e,i}\mu_{e,i}\vec{E} - D_{e,i}\nabla n_{e,i}$$

where $\vec{E}$, ε, e, $\vec{v}$, n, M, μ, D and S are the electric field, dielectric permittivity, charge, fluid velocity, charged particle density, excited species number density, mobility, diffusion coefficient and source function, respectively. The electric field for drift motions and gas reactions was calculated by local field approximation. Details in modeling and gas reactions for Ne-Xe mixture can be found in ref. [5] and ref. [6].

3. Results & Discussion

2.1 Discharge characteristics of the ramping reset pulse

Fig. 2 shows the applied pulse waveforms for the driving of one sub-field. The first pulse into the sustain electrode is referred to as the erase pulse in this study, and the large amplitude ramping pulse into the scan electrode between the time t1 and t4 in Fig. 2 is referred to the reset pulse. The ramp rate of the erase pulse was 6 V/μs and that of ramping pulses was 2.2 V/μs. To investigate the steady state of the operation, we considered that the discharge cell maintained the sustain discharge prior to the erase pulse application. Fig. 3(a) shows the wall charge distributions at the initial stage of the time t0. The positive wall charges are built up on the dielectric surface of the sustain electrode, and negative wall charges on that of the scan electrode, because the last sustain discharge is generated by the positive pulse application into the scan electrode. However, the discharges induced by the erase pulse diminish the amount of the wall charges built-up on each electrode, hence the wall voltage between the scan and the sustain electrodes are decreased at time t1, as shown in Fig. 3(b).

During the reset period, the discharge current shows multiple small peaks. It is known that the discharge by simple square pulse induces one strong pulse of discharge current, and that self-erase discharge occurs at the fall time of the applied pulse. Strong discharge deteriorates the contrast ratio, and wall charge loss by self-erase results in the decrease of the wall charges hence increasing the address voltage during the subsequent addressing period. However, the contrast ratio and the address voltage are enhanced by the multiple weak discharges induced by the ramping pulse application [1-2]. Fig. 4 shows the pulse waveforms and current flows through each electrode. The scan electrode plays the roles as an anode during the ramping-up period

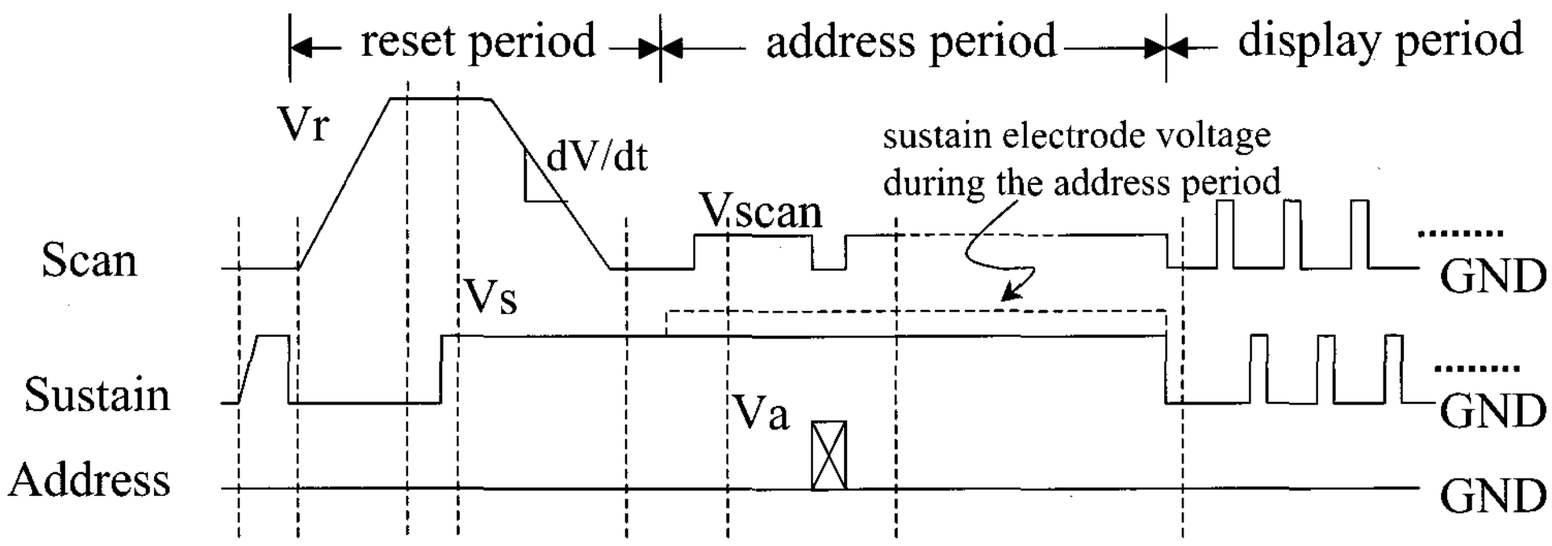
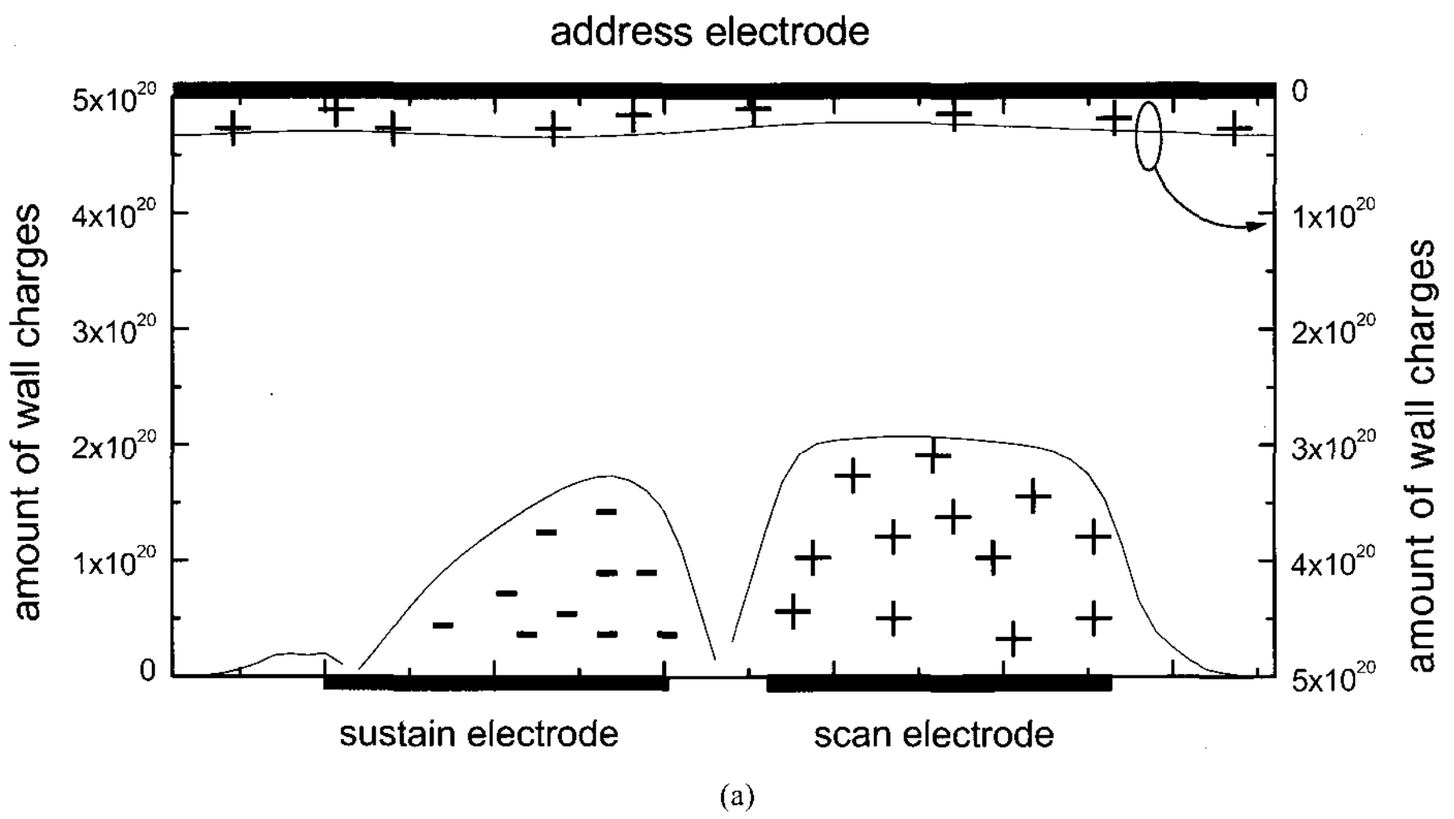
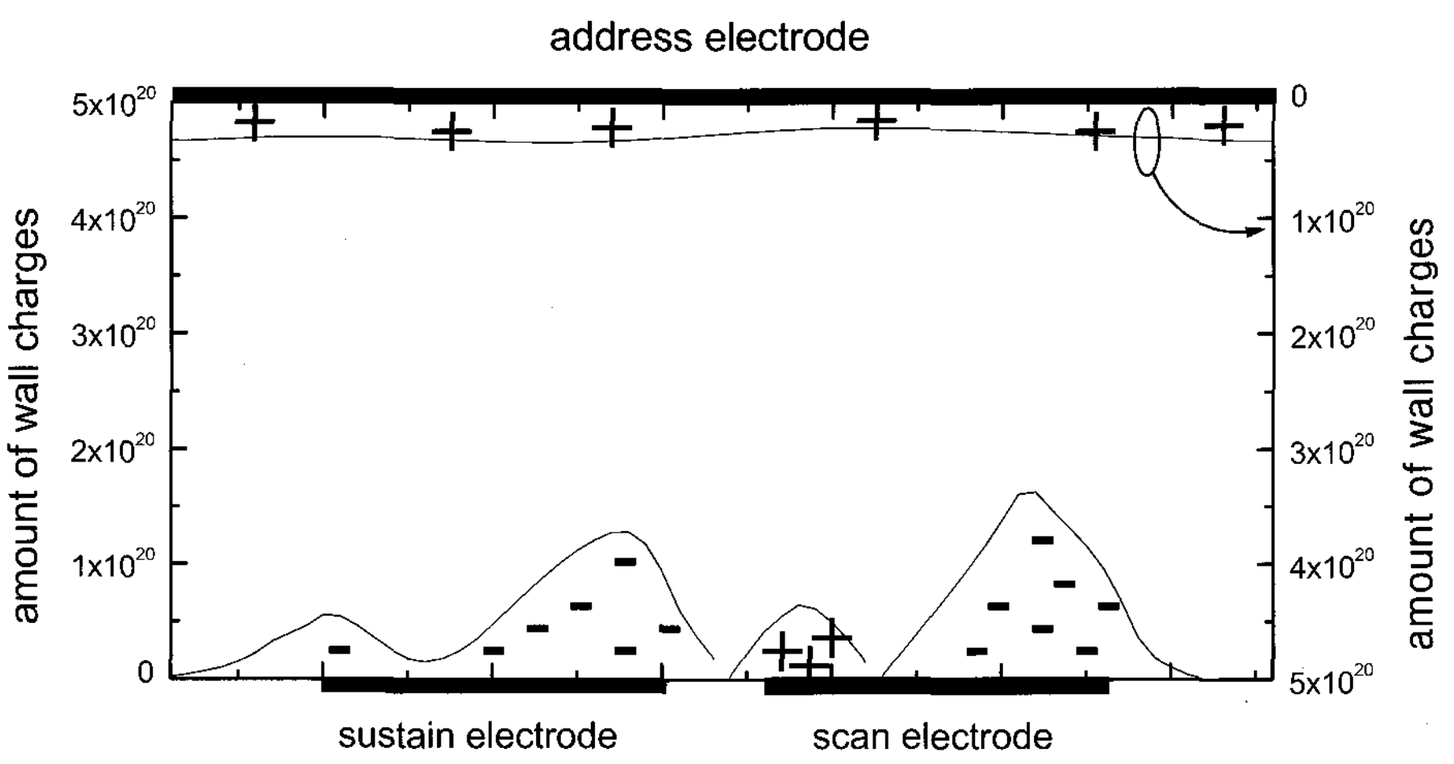


Fig. 2. The used driving waveforms.



(a)



(b)

Fig. 3. Wall voltage distributions (a) before and (b) after the erase pulse application.

and as a cathode during the ramping-down period. The roles are reversed for the sustain and address electrodes. The wall charge distributions on each electrode after ramping-up are shown in Fig. 5(a). The scan electrode gathers negative wall charges and sustain/address electrodes positive wall charges. It is evident that there is no changes in wall charge distributions by the pulse application Vs into sustain electrode while scan voltage is maintained at write voltage Vr because there is no discharge current during the transition from t2 to t3. Fig. 5(b) shows the wall charge distributions after ramping-down of the scan voltage. There is large wall voltage

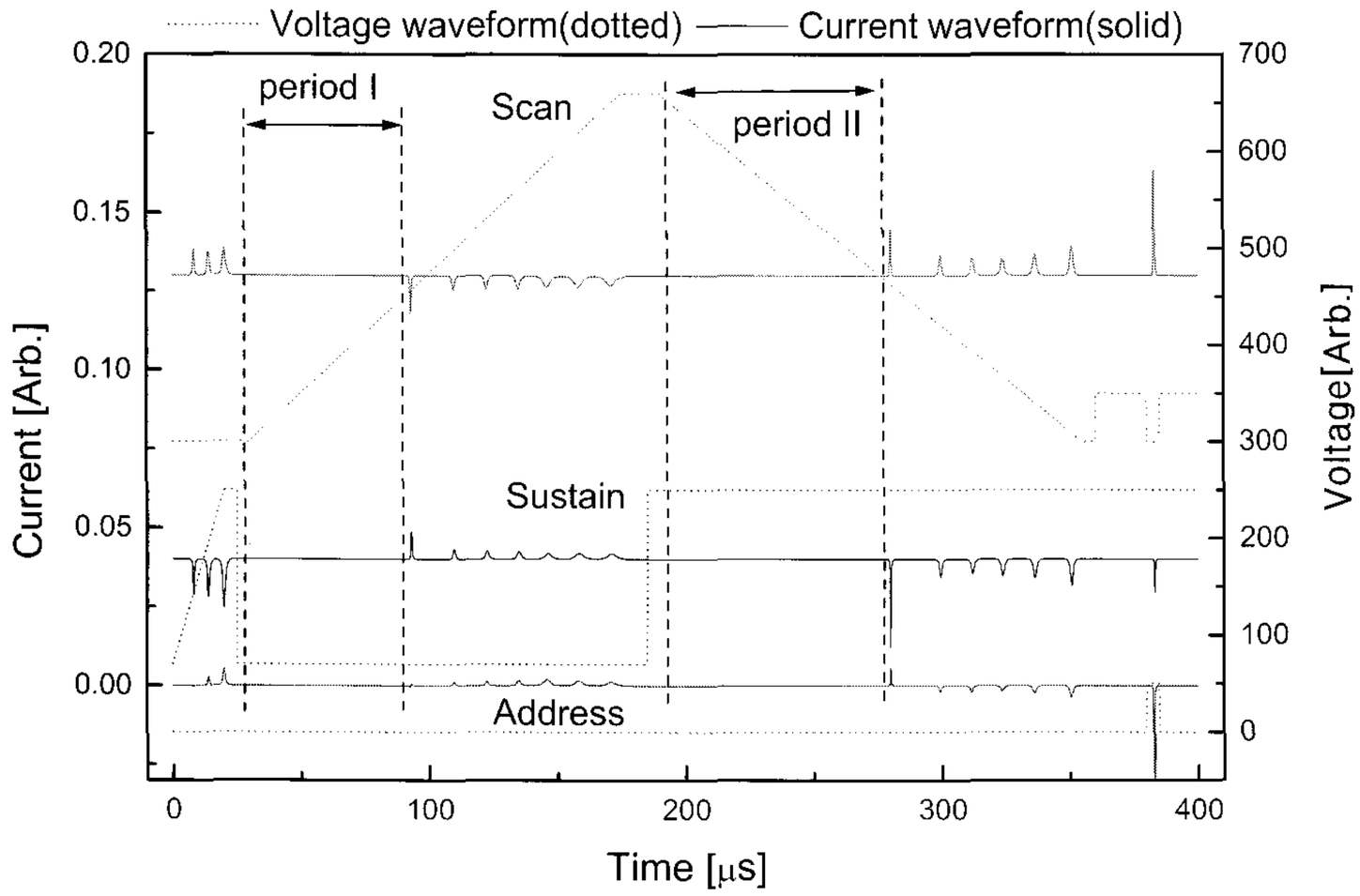
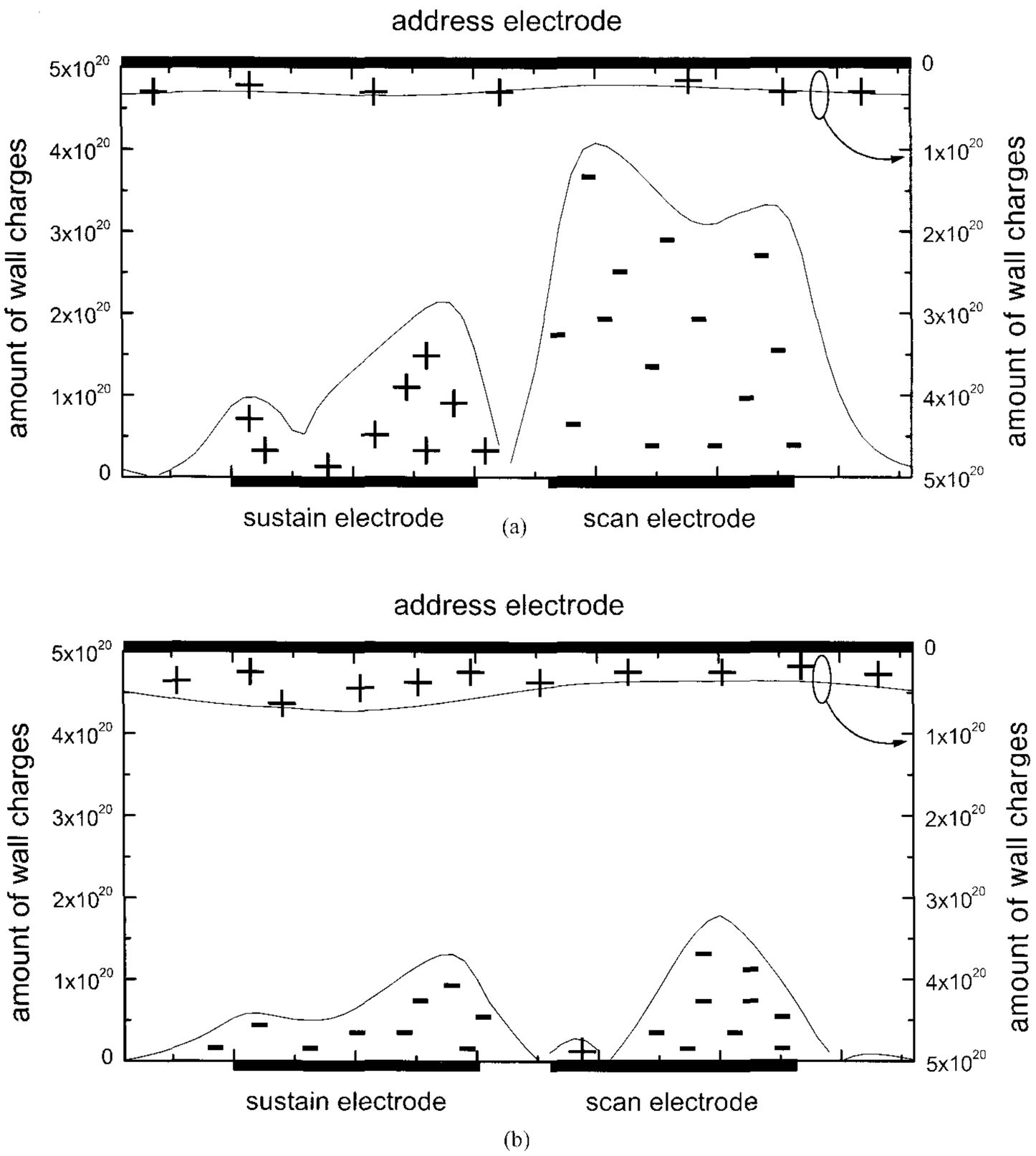


Fig. 4. Current flows during the erase, the reset, and the address period .



Wall voltage distributions (a) after the ramping-up, at time t2, and (b) after the ramping-down, at time t4, of the scan p

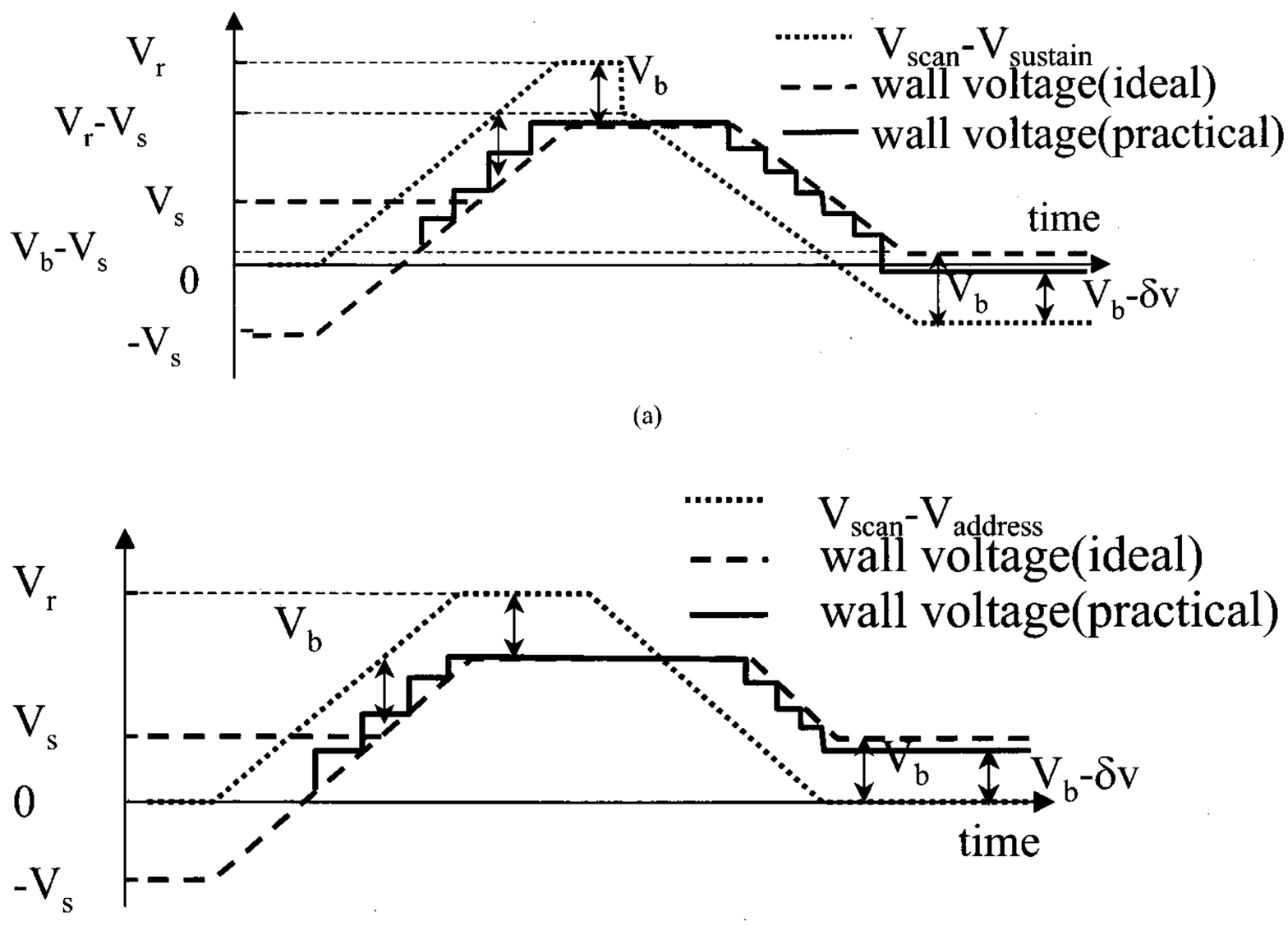


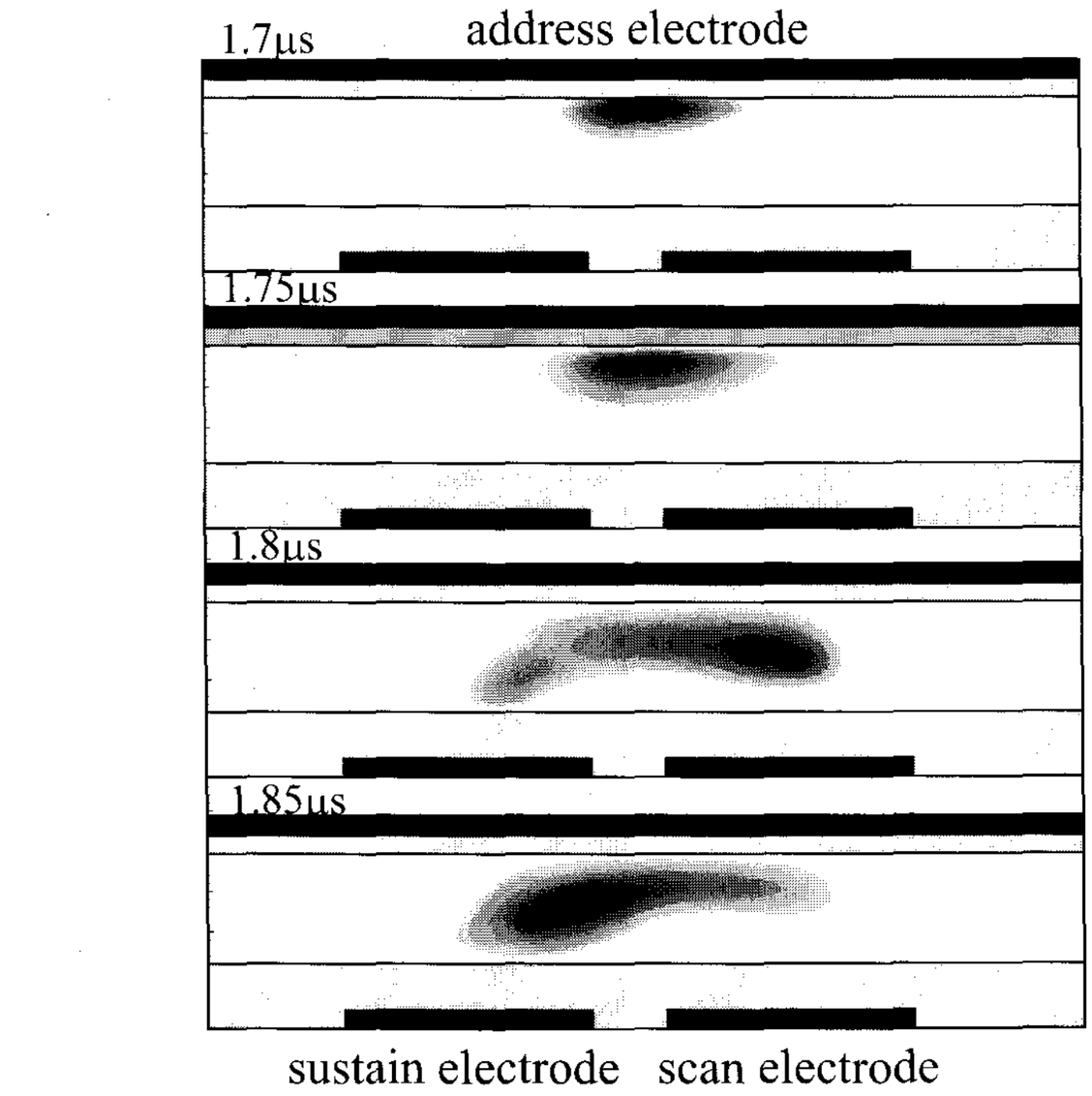
Fig. 6. Wall voltage variations in ideal and practical cases (a) between the scan and the address electrodes, and (b) between the scan and the address electrodes.

differences between the scan and the address electrodes, but small differences between the scan and the sustain electrodes. The gap voltage established between sustain and scan electrodes, however, is large because the sustain electrode is maintained at Vs. The voltage shift of scan electrode to the scan voltage Vscan, also, does not change the wall voltage distributions. Thus, the wall charge distributions during the address period at time t5 is the same as those set up after the reset period at time t4, but the gap voltage between the scan and the address electrodes is lowered by the scan voltage. The roles of each pulse can be summarized as follows;

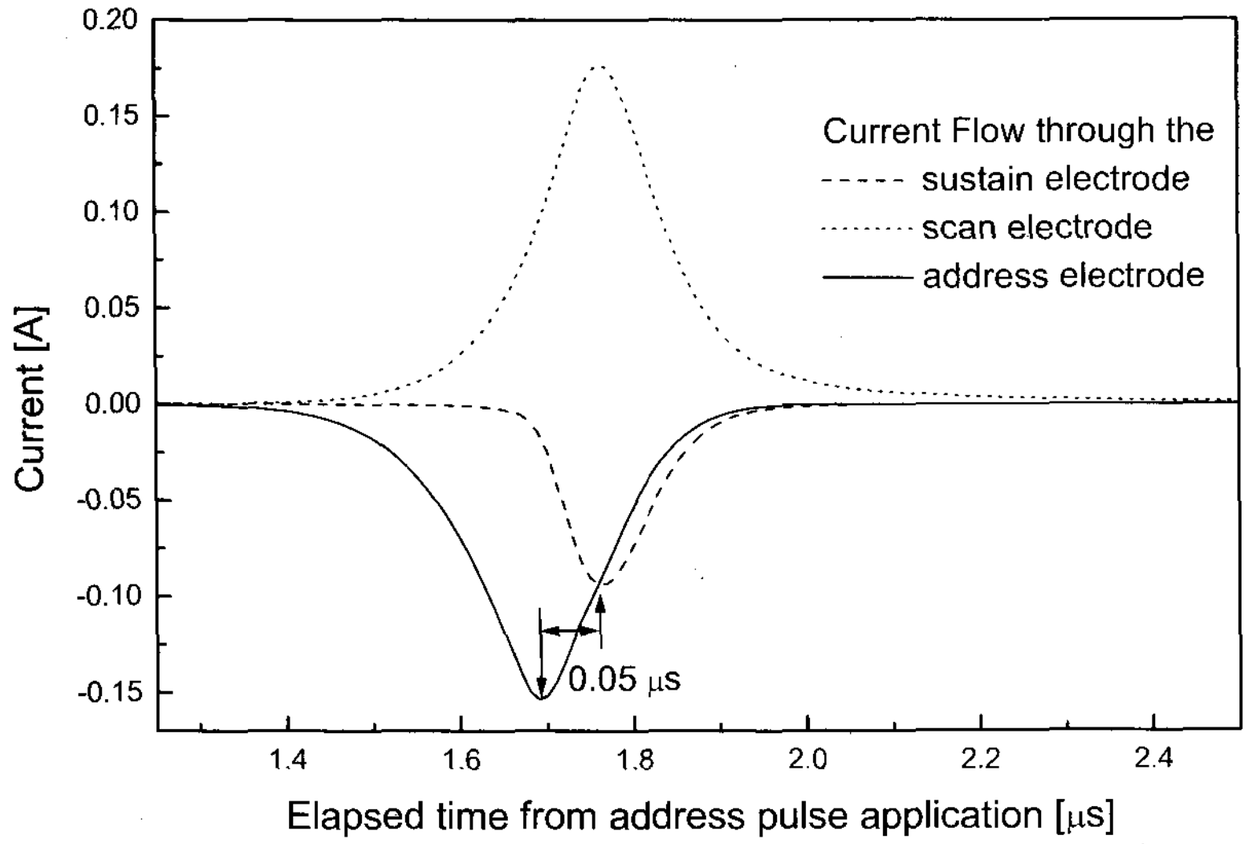
(1) the erase pulse clears the wall charge history,
(2) the ramping-up pulse supplies the negative wall charges onto scan electrode and the positive wall charges onto sustain and address electrodes,
(3) the ramping-down pulse diminishes the setup wall charges on each electrode according to the voltages applied to each electrode.

Hence, the same wall charges are set up onto each electrode regardless of the discharge history in all the discharge cells. We can know that, in practical use, the ramping pulse application during period I and period II, in Fig. 4 can be omitted to save the time for the display period. Even abrupt voltage shift during period I and the period II will not bring about any changes in wall charge distributions because discharge currents are not found during the periods.

We have reported that the wall voltage changes during the ramping reset pulse application can be estimated by considering two sets of wall voltage variations using voltage transfer curve analysis; one between the scan and the sustain electrodes, and the other between the scan and the address electrodes according to the roles of each electrode [7-8]. In an ideal case, where wall voltage shift is very small due to the application of infinitely long ramping pulse, the wall voltages will change along the dashed lines as in Fig. 6(a) and Fig. 6(b) [8]. Considering the discharge characteristics during the ramping reset, the wall voltage variations can be corrected as solid lines as in Fig. 6(a) and Fig. 6(b). The staircase variations in wall voltages are the result of the characteristics of the discharge, which is based on the avalanche processes of gas ionization. The final gap voltage between the scan and the address electrodes is lower than V_b, i.e. V_b-δv



(a)



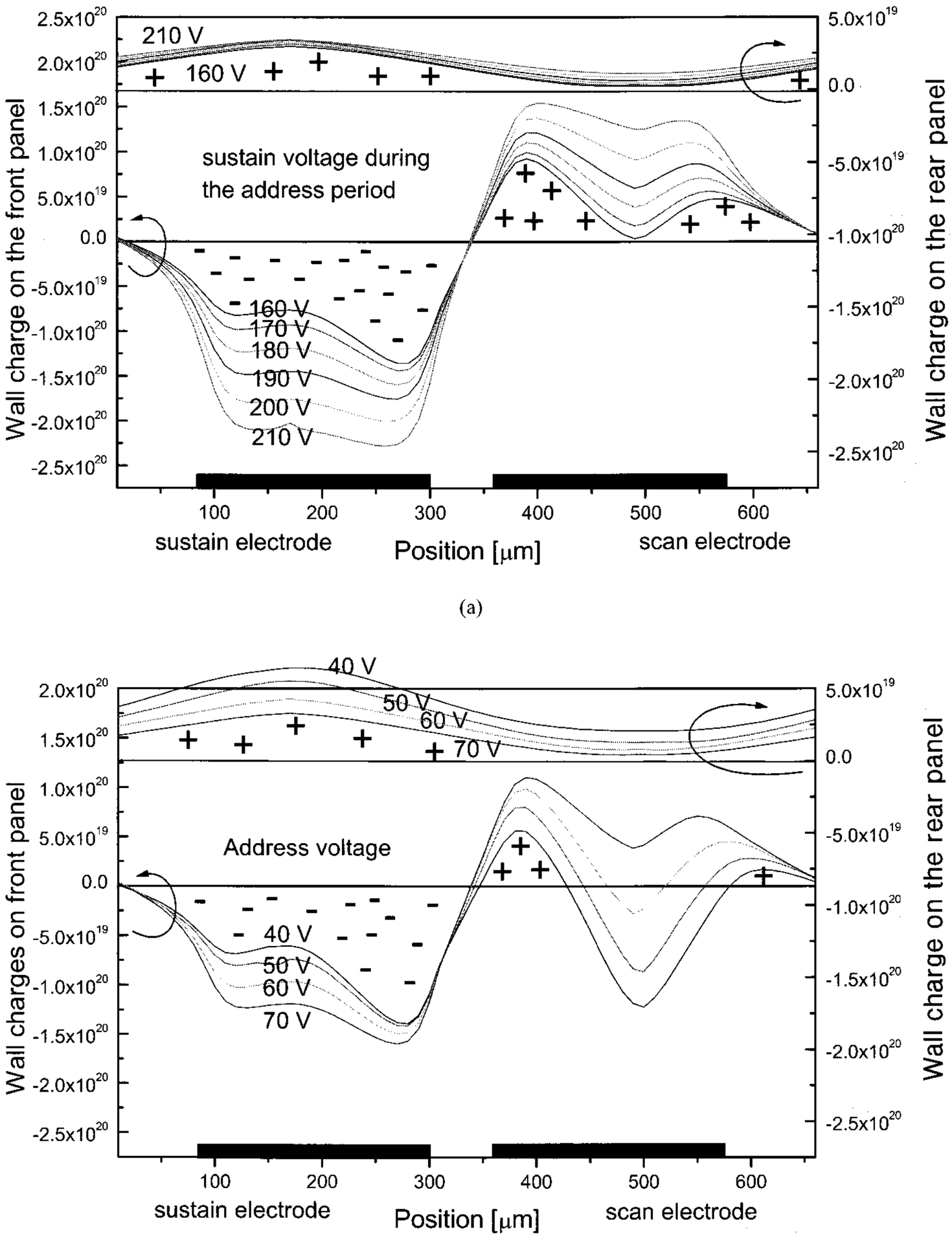
(b)

Fig. 7. (a) Time evolution of the electron distribution, and (b) current flows during the address period

where V_b is the breakdown voltage between the scan and the address voltage and δv is the positive value depending on the wall voltage shift between multiple discharges during the pulse ramping. In this study, δv is estimated to be about 40 V because at least 40 V of the address voltage was needed to form address discharge. The set up wall charges by the address discharge affect the subsequent sustain discharges, so we closely observed the changes in the setup wall charges with the variations of the sustain electrode voltage and the address voltage during the address discharge.

2.2 The characteristics of the address discharge

It is considered that the address discharge is generated only between the scan and the address electrodes.

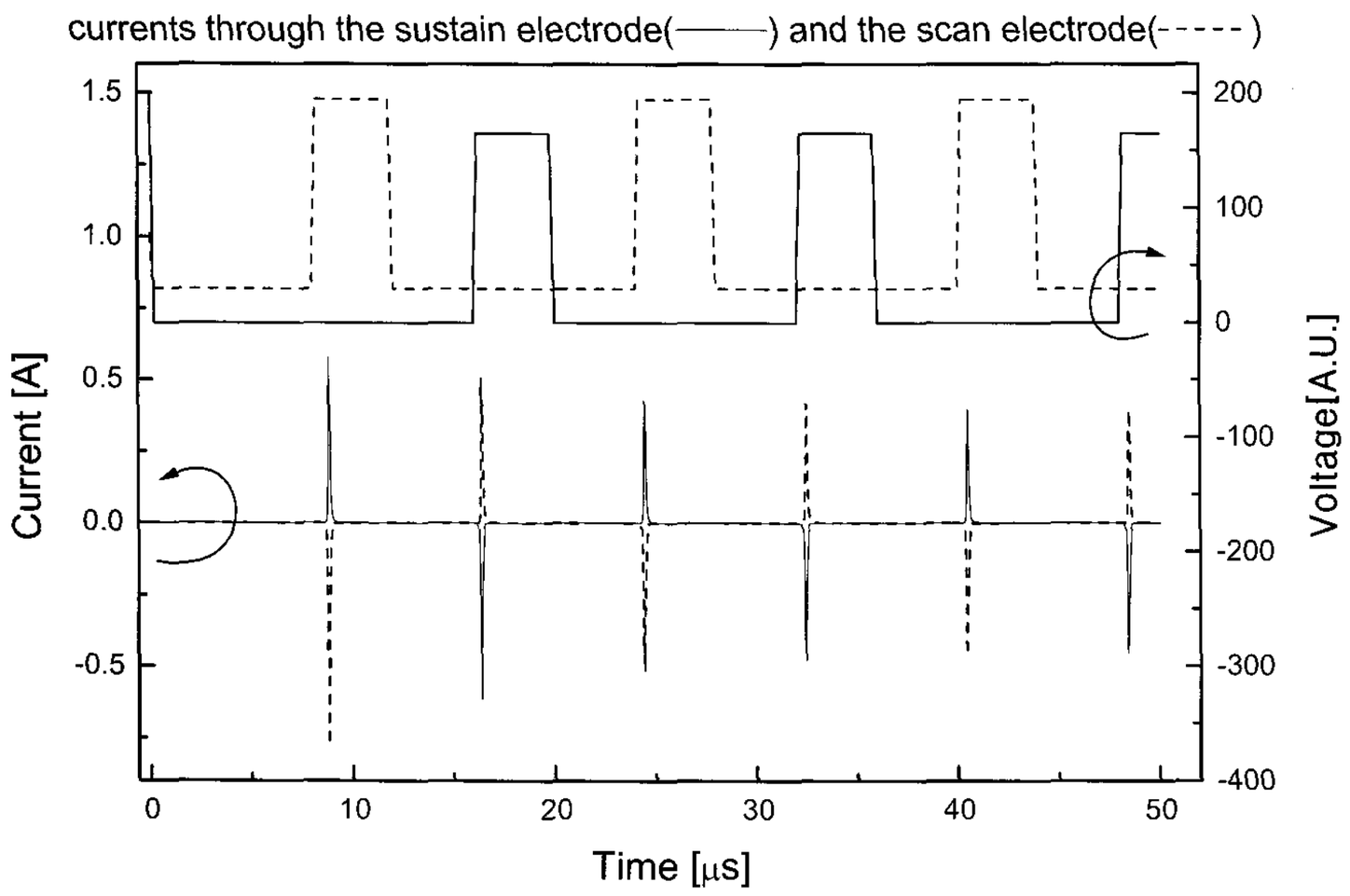


(a)

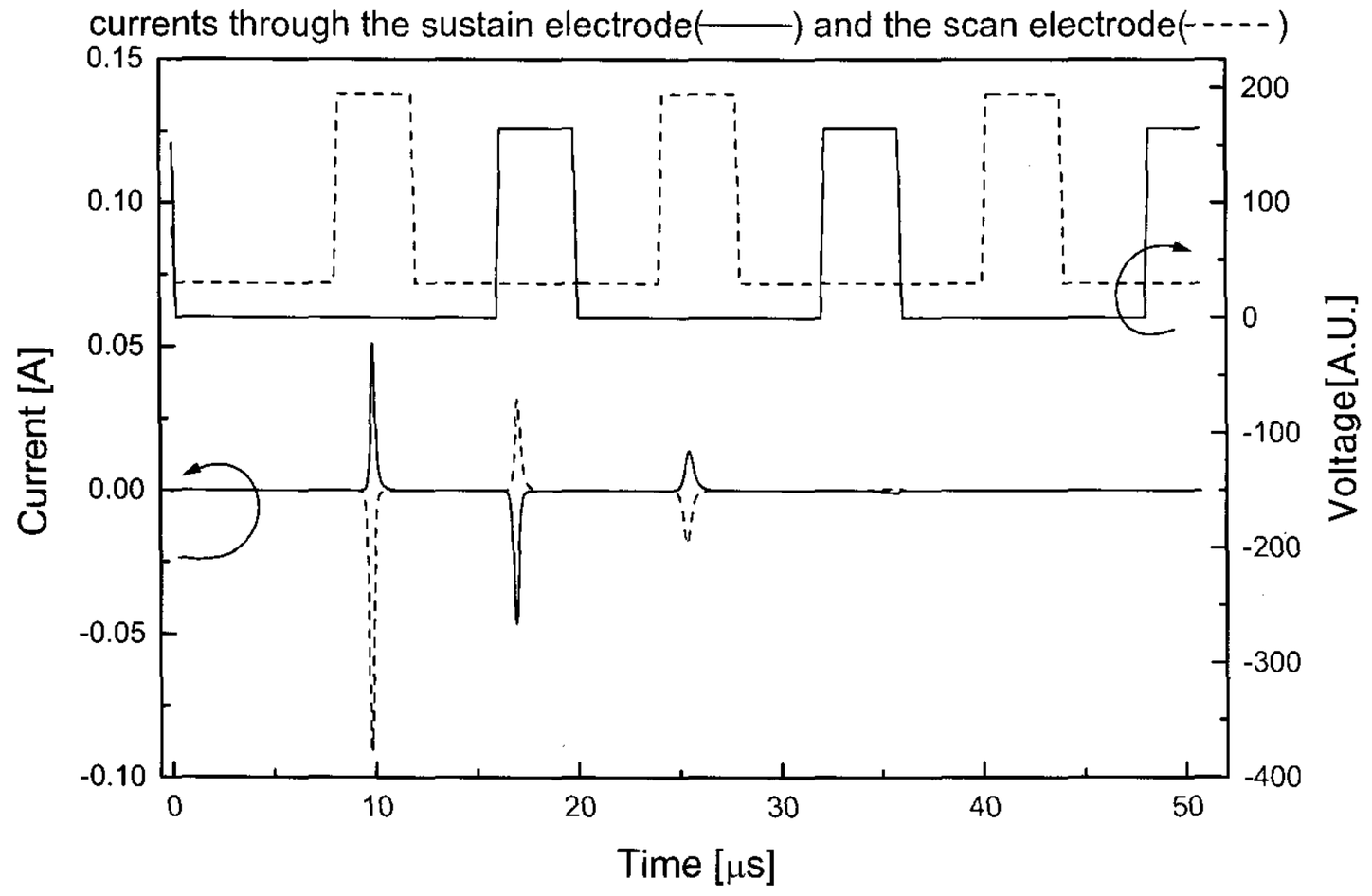
(b)

Fig. 8. Changes in wall charge distributions with the changes in (a) the voltages applied to the sustain electrode during the address period [address voltage: 70 V], (b) the address voltage [the sustain electrode voltage during the address period: 180 V].

However, close observation of the current flows during the address period revels that the contributions of sustain electrode is also not ignorable. We investigated the characteristics of the address discharge by observing the time evolution of electrons. Fig. 7(a) shows that the discharge ignited in the vicinity of the address electrodes because the address electrode plays the roles of an anode during address discharge. However, the address discharge changes its path to being between the scan and the sustain electrodes because the built-up gap voltage between the scan and the sustain electrodes is also large enough. This dynamic phenomenon induces the changes in current peaks through each electrode. Fig. 7(b) shows that the earlier current peaks appear through the address and the scan electrodes, and the current flow through sustain electrode is delayed. The amount of wall charges on the sustain electrode is also changed because the electrode contributes to the address discharge. We can estimate that the wall charge changes will be varied according to the sustain electrode voltages during the address period. Fig. 8(a) shows the changes in the wall charge distributions with the changes of the sustain



(a)



(b)

Fig. 9. The current flows during the display period in case the sustain electrode maintained (a) 210 V, and (b) 160 V during the address period [sustain voltage : 165 V].

electrode voltage during the address period, while address voltage is kept the same at 70 V. By the nature of an ac PDP, the increased amount of wall charges will affect the subsequent discharges. We can estimate that the sustain voltage can be reduced during display period by increasing the sustain electrode voltages during the address period. The sustain voltage, however, must evidently be larger than the minimum sustain voltage which is determined by the voltage transfer characteristics between the scan and the sustain electrodes. Also, the more increment of wall charges on the sustain electrode is expected as the address voltage increases because more intense discharge will supply sufficient wall charges to the sustain electrode, as shown in Fig. 8(b).

Fig. 9 shows the voltage waveforms and current flows through the sustain and the scan electrodes during the display period. The sustain voltage goes to zero from the voltage applied to sustain electrode during the address period in 0.2 μs initial stage of the display period, and

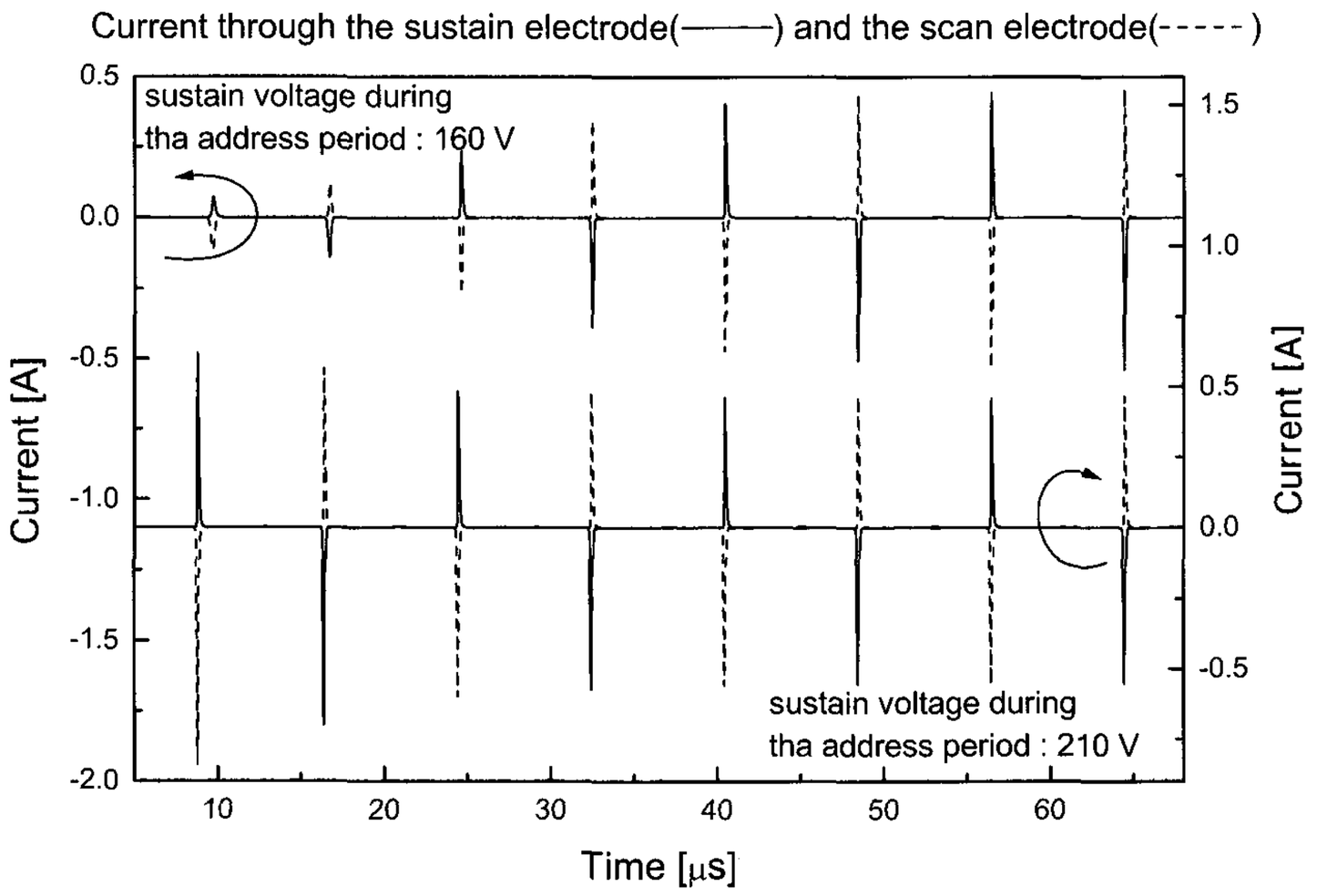


Fig. 10. The current flows during the display period in case the sustain electrode maintained (a) 210 V, and (b) 160 V during the address period [sustain voltage : 165 V].

the subsequent sustain pulses are alternatively applied to scan and the sustain electrodes. The amplitude of the sustain voltage was 165 V, and the rise and the fall time of the pulses were the same as 200 ns. Fig. 9(a) shows the current flows during the display period in the case where the sustain electrode is maintained at 210 V during the address period. The sustain discharge was stabilized after three or four pulse applications. However, the sustain discharge was not properly generated in the case the sustain electrode was maintained at 160 V during the address period. This can be explained by the wall voltages built-up through the address discharge as shown in Fig. 8. The analysis of the voltage transfer curve suggests that the sequent sustain discharge requires sufficient initial wall voltage setup. In other words, the insufficient wall voltage can induce discharge failure during display period. Even in the case where a large enough sustain voltage is applied during the display period, the discharge current could show different behaviors, as in Fig. 10. In the case where the initial wall voltage is sufficient, the wall voltage converges to the stable point of the voltage transfer curve along the right side path, but along the left side path in the case where the wall voltage is insufficient.

3. Conclusions

In the driving scheme adopting ramping reset pulse, the roles of each pulse applications were investigated using a 2-dimensional discharge cell simulation of an ac PDP. The erase pulse diminishes the wall charges setup on each electrode. The ramping pulse induced the multiple weak discharges. During the ramping-up, the negative wall charges were set up on the dielectric surface of the scan electrode, and positive wall charges on that of the sustain and the address electrodes. After reset pulse application, large amount of wall charges were set up between the scan and the address electrodes to decrease the subsequent address voltage.

The address discharge did not generate simply between the scan and the address electrodes, i.e. the sustain electrode also contributed to the discharge. From the observation of the discharge and current flows, it was found that the address discharge is first ignited in the vicinity of the address electrode, and it changes its path to being between the scan and the sustain electrodes. The amount of the wall charges on the sustain electrode increased during the address period, and this increment usually depends on the contributions of the sustain electrode to the address discharge. The increment grows larger with the increase of the sustain electrode voltage during the address period. Consequently, it is expected that the increase of the sustain electrode voltage during the address period will reduce the sustain voltage during display period. In other words, the minimum address voltage required for proper sustain discharge can be

reduced with the increase of the sustain electrode voltage during the address period.

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