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Staggered Voting for TMR Shift Register Chains in Poly-Si TFT-LCDs

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Abstract

This paper presents the idea of staggered voting for the efficient TMR implementation of shift register chains for improving the yield of Poly-Si TFT-LCD driving circuits. The paper discusses the characteristic features of staggered voting and performs a quantitative evaluation of its effectiveness. Staggered voting allows us to improve the reliability of a single-voter TMR chain significantly when the probability of a voter failure is not negligible.

Keywords : Poly-Si TFT-LCD, yield, staggered voting, TMR, shift register chain.

1. Introduction

The Poly-Si TFT-LCD technology allows us to integrate driving circuits and pixels on a single glass substrate. Such an integration can save the cost of external driving ICs in conventional TFT-LCDs at the expense of increasing the number of steps necessary to process a substrate. The technology has replaced conventional TFT-LCD in small-screen applications [1-2]. However, there are several challenges in developing large-screen, high-quality Poly-Si TFT-LCDs. One of the challenges is that the size of driving circuits can be enormous. Then, the yield of driving circuits would be a serious problem.

We can address the issue of yield from several directions. For example, we can improve the architecture of driving circuits to reduce the size of driving circuits. This will help improve the yield. Alternatively, we can improve the manufacturing technology or rely on robust implementation of driving circuits. This paper discusses the use of circuit-level redundancies to improve the yield of driving circuits. Specifically, we present a new triple-modular-redundant (TMR) structure for the robust implementation of shift register (S/R or SR) chains in Poly-Si TFT-LCDs.

2. Background

We can classify the driving circuits for Poly-Si TFT-LCDs into two types: analog and digital. Digital driving is essential for large-screen, high-quality Poly-Si TFT-LCDs. Figure 1 illustrates the structure of a digital Poly-Si TFT-LCD. The S/R chain of the gate driver generates scan pluses to sequentially enable the gate lines. When a gate line is enabled, all pixel transistors in the corresponding line of pixels are turned on. Then, the image signals stored in the latch chain in the data driver are passed on to the line of pixels. The S/R chain in the data driver generates the timing signal necessary for the latch chain to read in the image signals coming from an external controller. A D/A converter converts the digital image signal stored in a latch into an analog voltage.

One of the key issues in designing driving circuits for large-screen, high-quality Poly-Si TFT-LCDs is the size

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of driving circuits and the resulting yield. The minimum feature size supported by the TFT-LCD fabrication process is typically a few microns, and Poly-Si TFTs have very limited driving capability. Also, a data driver can consist of thousands of S/Rs, latches, D/A converters, and current buffers. As a result, for example, the height of the data driver (Figure 1) for 14.1″ XGA 6-bit Poly-Si TFT-LCD can be in the order of centimeters. With this size, the yield of driving circuits can be a serious problem. If the yield of driving circuits drops, Poly-Si TFT-LCDs may not be able to compete with conventional TFT-LCDs. This is a reason why only the gate driver, which is much simpler than the data driver, is integrated on the panel in today's mid-size Poly-Si TFT-LCDs [3-4].

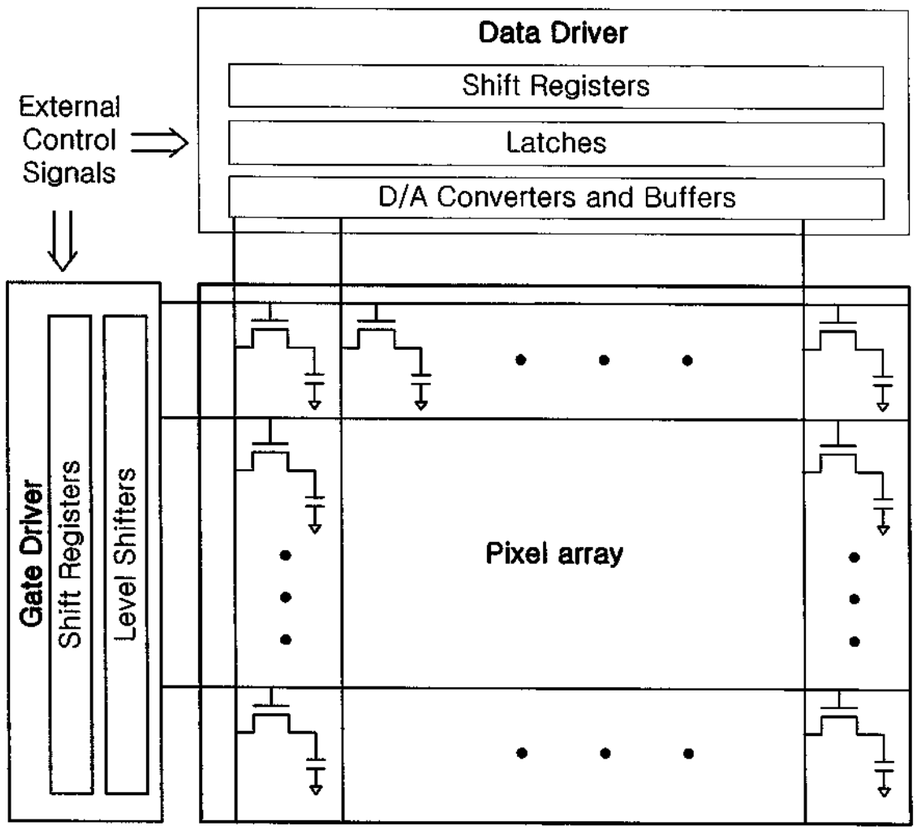
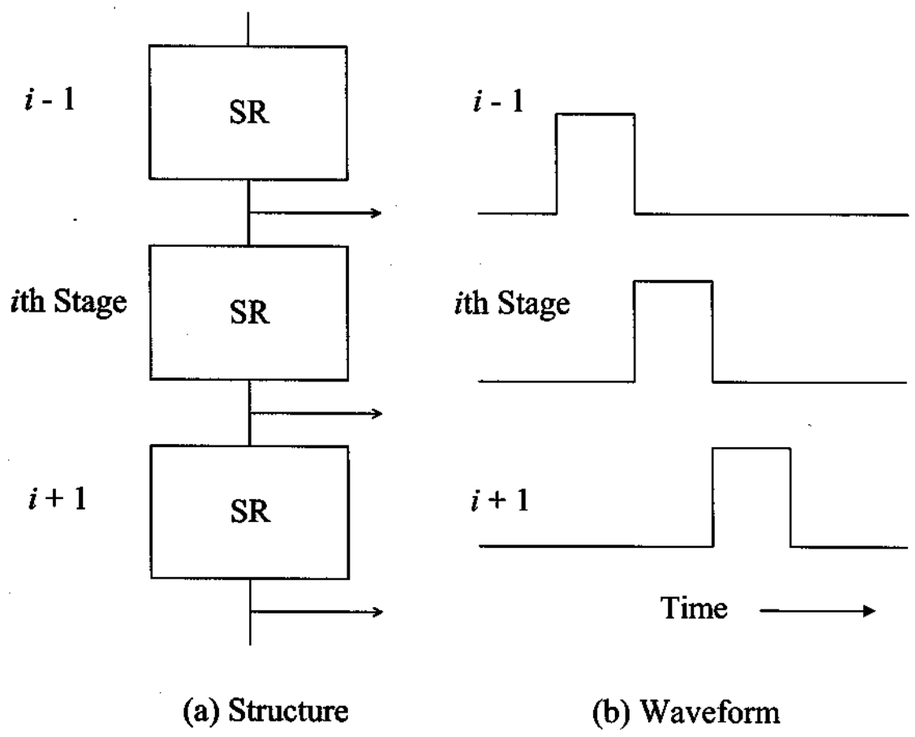


Fig. 1. Structure of fully-integrated digital Poly-Si TFT-LCD.



(a) Structure (b) Waveform

Fig. 2. Shift register chain: (a) structure and (b) output waveform.

This paper focuses on the yield of S/R chains in Poly-Si TFT-LCDs. As shown in Figure 1, both the data and gate drivers contain S/R chains. A S/R chain is nothing but a serial of connection of multiple S/Rs (Figure 2). In a Poly-Si TFT-LCD, given a timing pulse from an external controller, a S/R chain sequentially moves the pulse to the next stage at every clock cycle. In the gate driver, the output of each S/R stage is connected to a gate line; in the data driver, the output of each S/R stage is used to enable a latch. In the case of an XGA-resolution Poly-Si TFT-LCD, there are 768 S/Rs in the gate driver chain and 1024 S/Rs in the data driver chain. Note that if any S/R in a chain does not work, it means that the entire driving circuits will not work.

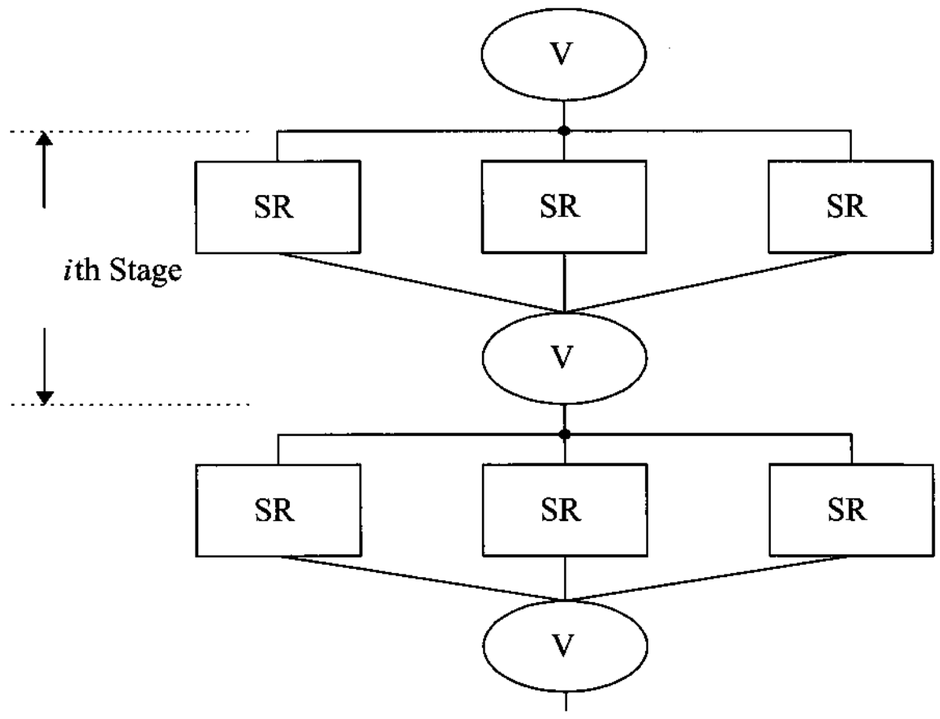


Fig. 3. TMR S/R chain with a single voter per stage.

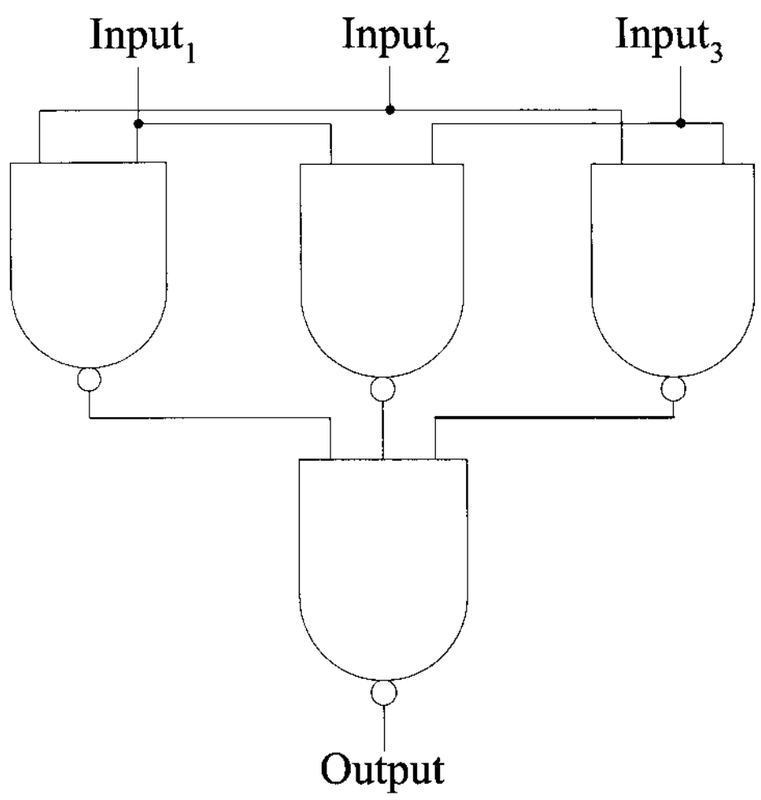


Fig. 4. Logic diagram of two-out-of-three majority voter.

Toshiba uses a TMR structure to implement the gate driver S/R chain in its 10.4″ XGA Poly-Si TFT-LCD [3]. In this conventional TMR structure, as shown in Figure 3, each S/R stage consists of three S/Rs and a majority

voter. The majority voter is a combinational circuit that takes the outputs of three S/Rs, which is either "high" or "low," and chooses the majority of them (Figure 4). The voter output is used in all three S/Rs in the next stage. Note that a S/R stage in Figure 3 can function correctly even if one of the three S/Rs does not work, which is why the TMR structure is used.

In typical TMR applications, a voter is much simpler and thus is much more reliable than a module to be voted, which justifies the use of a single voter. However, this is not the case in the TMR S/R chain. It takes 18 transistors to implement the two-out-of-three majority voter in Figure 4, while it takes 16 transistors to implement a typical static S/R. Then, the question is: what if a voter does not work? Since the probability of a voter failure is comparable to that of a S/R failure, the structure in Figure 3 does not make sense unless we somehow make a voter much more reliable than a S/R.

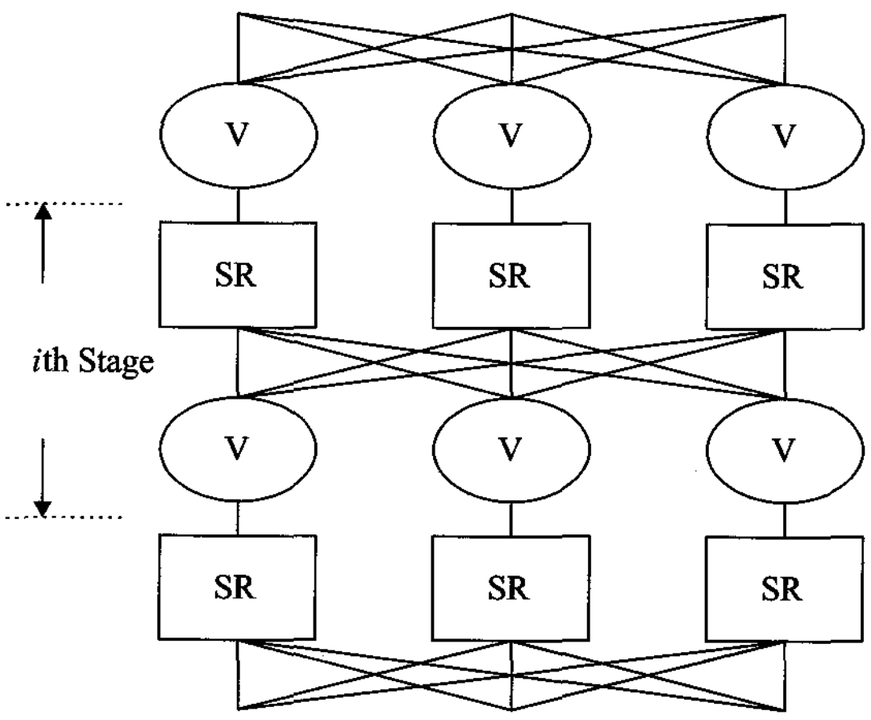


Fig. 5. TMR S/R chain with three voters per stage.

To protect against voter failures, we can use three voters in a stage [5]. In Figure 5, a S/R stage can function correctly even if one of the three voters in the stage does not work. However, the structure uses 500 % more hardware than its non-redundant counterpart in Figure 2, which is a substantial overhead. (The structure in Figure 3 uses 300 % more hardware.) Clearly, we need a better solution.

3. Staggered Voting for TMR S/R Chains

This section presents a new voting structure, called staggered voting, to deal with voter failures while using the same amount of hardware as in the single-voter TMR. Figure 6 illustrates the idea of staggered voting. The characteristic features of staggered voting are two-fold. First, the output of a voter is connected to the input of only one S/R in the next stage. The rationale is that a voter failure should not affect all three S/R chains, in which case the effect of the failure can be masked if the S/Rs and voters in the other two chains near the faulty voter work. Second, the location of voter (i.e., the S/R chain to which a voter's output is connected) differs from stage to stage, which is why we call the structure staggered voting. The rationale is that, if all voters are located in a single S/R chain, we can not protect against the possible defects in the remaining two S/R chains. We can think of many ways to change the voter location from stage to stage. Figure 6 shows a canonical connection topology.

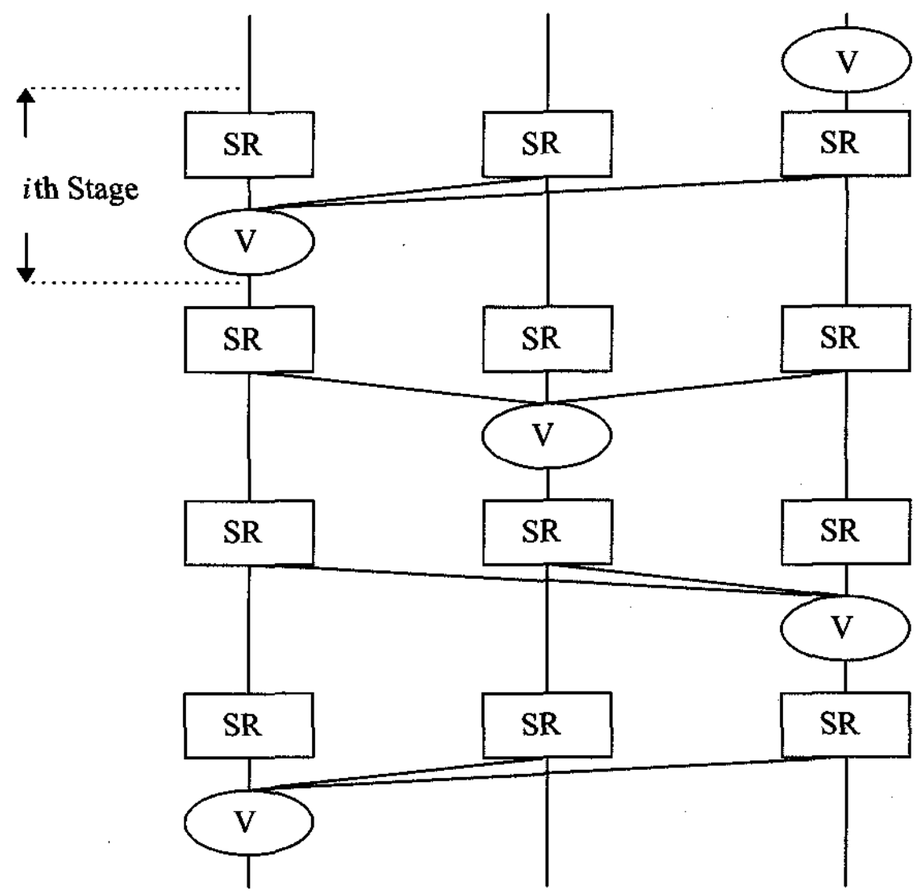


Fig. 6. Canonical connection topology in staggered voting TMR.

We investigate the reliability of the TMR S/R chain with staggered voting, in comparison with those of other S/R chain structures discussed in the previous section. Since our focus is on manufacturing defects, the terms reliability and yield are used interchangeably. To simplify the analysis, we assume that the probability of S/R failure is identical to that of voter failure; we use A to denote this probability. We also assume that all S/R and voter failures are independent of each other.

Let's first consider the plain S/R chain with no redundancy (Figure 2). The reliability of a stage in the plain S/R chain is simply:

TABLE 1. Reliability of a stage in staggered voting TMR S/R chain.

Cases for the *i*th Stage	Circuit Blocks That Must Work			Probability
	*i*th Stage	Earlier Stages	Later Stages	
All SRs and Voter Work	V_i, $SR_{i,1}$, $SR_{i,2}$, $SR_{i,3}$	-	-	$(1-A)^4$
V_i Fails	$SR_{i,1}$, $SR_{i,2}$, $SR_{i,3}$	V_{i-1}, V_{i-2}, $SR_{i-1,2}$	V_{i+1}, $SR_{i+1,2}$, $SR_{i+1,3}$, V_{i+2}, $SR_{i+2,2}$, $SR_{i+2,3}$, V_{i+3}, $SR_{i+3,2}$, $SR_{i+3,3}$	$A(1-A)^{15}$
$SR_{i,1}$ Fails	V_i, $SR_{i,2}$, $SR_{i,3}$	V_{i-1}, V_{i-2}, $SR_{i-1,2}$	-	$A(1-A)^6$
$SR_{i,2}$ Fails	V_i, $SR_{i,1}$, $SR_{i,3}$	V_{i-1}, V_{i-3}, $SR_{i-2,1}$, $SR_{i-1,1}$	V_{i+1}, $SR_{i+1,1}$, $SR_{i+1,3}$	$A(1-A)^{10}$
$SR_{i,3}$ Fails	V_i, $SR_{i,1}$, $SR_{i,2}$	V_{i-2}, $SR_{i-1,2}$, V_{i-3}, $SR_{i-2,1}$, $SR_{i-1,1}$	V_{i+1}, $SR_{i+1,1}$, $SR_{i+1,2}$, V_{i+2}, $SR_{i+2,1}$, $SR_{i+2,2}$	$A(1-A)^{14}$
V_i and $SR_{i,1}$ Fail	$SR_{i,2}$, $SR_{i,3}$	V_{i-1}, V_{i-2}, $SR_{i-1,2}$	V_{i+1}, $SR_{i+1,2}$, $SR_{i+1,3}$, V_{i+2}, $SR_{i+2,2}$, $SR_{i+2,3}$, V_{i+3}, $SR_{i+3,2}$, $SR_{i+3,3}$	$A^2(1-A)^{14}$

$$P_1 = 1 - A \quad (1)$$

The reliability of a stage in the single-voter TMR S/R chain in Figure 3 is:

$$P_2 = \text{Prob (voter works) Prob (2 out of 3 S/Rs work)}$$
$$= (1 - A) \times 3A(1-A)^2 \quad (2)$$

Note that P_2 is smaller than P_1, which is natural when the voter and S/R failures are equally likely. The reliability of a stage in the three-voter TMR structure in Figure 5 is:

$$P_3 = \text{Prob (2 out of 3 voters and 2 out of 3 S/Rs work)}$$
$$= [\,(1-A)^3 + 3(1-A)^2A\,]^2 \quad (3)$$

Finally, we calculate the reliability of a stage in the staggered voting TMR, which is redrawn in Figure 7. In the figure, V_i refers to the voter in the ith stage, and $SR_{i,1}$ refers to the S/R in the ith stage of the leftmost chain. In this structure, the probability that the defects in the ith

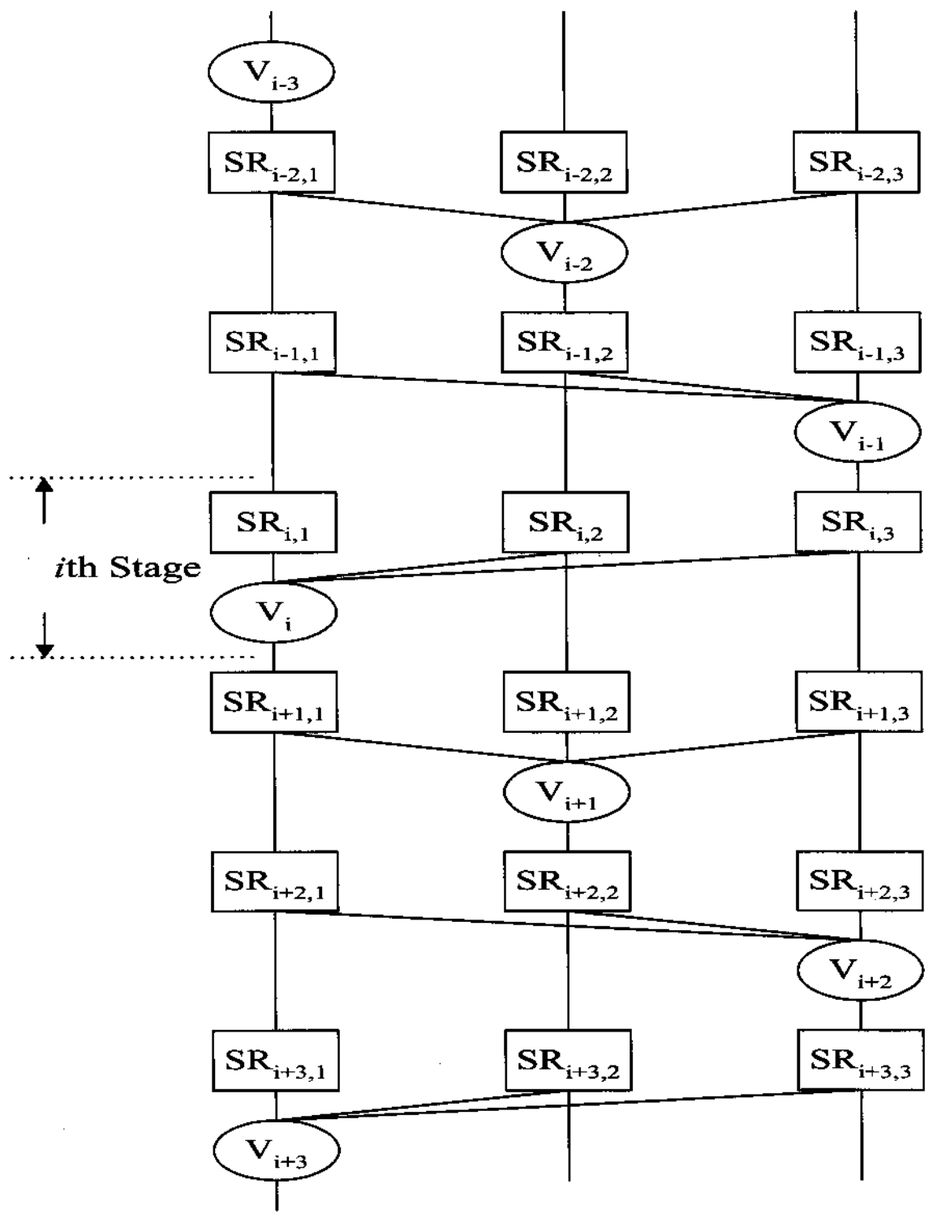


Fig. 7. Structure of staggered voting TMR S/R chain.

stage do not cause a failure of the entire S/R chain is the sum of the probabilities for the six cases in Table 1. The first column of the table lists the six possible cases, and the second column shows the circuit blocks in Figure 7 that must work to mask the defect(s) in each case. For example, consider the case where only V_i does not work. In this case, the circuit blocks $SR_{i+1,2}$, $SR_{i+1,3}$, V_{i+1}, $SR_{i+2,2}$, $SR_{i+2,3}$, V_{i+2}, $SR_{i+3,2}$, $SR_{i+3,3}$, and V_{i+3} must work to completely mask the effects of the failure of V_i. Further, since $SR_{i,2}$ and $SR_{i,3}$ must work, the circuit blocks V_{i-2}, $SR_{i-1,2}$, and V_{i-1} must also work. Given the failure of V_i, the probability that all these circuit blocks will work is quite high, which explains why the staggered voting TMR can tolerate a voter failure. The last column of the table shows the probability that each case happens.

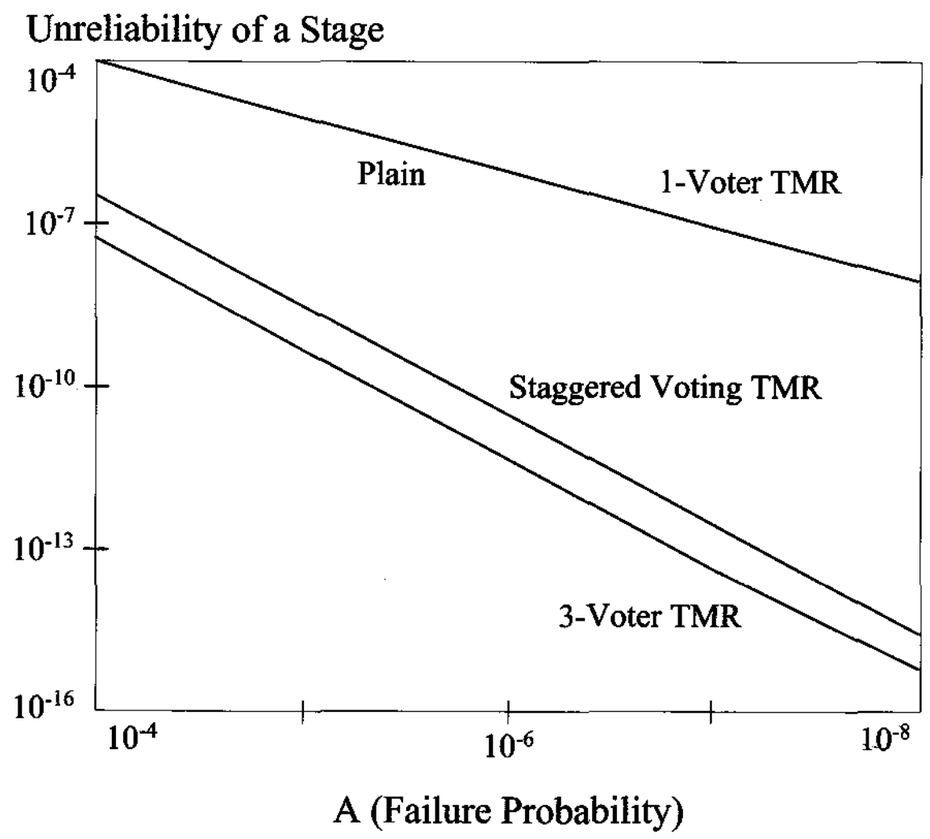


Fig. 8. Unreliability of a stage in staggered voting TMR S/R chain as a function of the failure probability of a S/R.

Figure 8 shows the unreliability (i.e., 1–reliability) of a stage in the four structures as we vary the value of *A*. Note that the single-voter TMR does not make much sense because it is less reliable than the non-redundant S/R chain. (However, the difference is very small and is unnoticeable in the figure.) The figure clearly shows that the TMR S/R chain with staggered voting is more reliable than the single-voter TMR S/R chain by orders-of-magnitude in the investigated range. Further, the TMRS/R chain with staggered voting makes sense because it is more reliable than the non-redundant S/R chain. In fact, the reliability of the staggered voting TMR S/R chain is quite close to that of the three-voter TMR implementation. These results clearly show the effectiveness of staggered voting.

4. Conclusions

In this paper, we presented a new voting structure, called staggered voting, for the robust TMR implementation of S/R chains in Poly-Si TFT-LCDs. We discussed the characteristic features of staggered voting and evaluated its effectiveness. What is special about the staggered voting is that, in contrast with the traditional single-voter TMR structure, it allows us to tolerate a voter failure with the same amount of hardware. As a result, we can improve the reliability of the TMR S/R chain significantly with staggered voting when the probability of a voter failure is not negligible.

The paper discussed staggered voting in the context of the TMR structure. However, the idea can be generalized to *n*-modular redundant architectures, and as *n* increases, diverse connection topologies and the use of multiple voters in a stage can be considered. Such a generalization can allow us to have more freedom in making cost-reliability trade-offs. Staggered voting is applicable to circuits that consist of a serial connection of many components.

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