Reducing the Poly-Si TFT Non-Uniformity by Transistor Slicing

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Abstract

Transistor slicing refers to the use of multiple smaller transistors in implementing a large MOS transistor. What is special about transistor slicing is that it can reduce the effects of device non-uniformity introduced during the fabrication process. The paper presents the idea of transistor slicing and analyzes the benefits of using transistor slicing in the context of Poly-Si TFT-LCD driving.

Keywords: Poly-Si TFT-LCD, digital driving, TFT non-uniformity, transistor slicing.

1. Introduction

In a Poly-Si TFT-LCD, we use poly-silicon TFTs to implement the driving circuits so that the driving circuits and panel (i.e., pixel array) can be fabricated on a single glass substrate. Such an integration allows us to save the cost of external driving ICs in conventional TFT-LCDs at the expense of adding a few more processing steps, which can be attractive. However, due to the lower driving capability of a poly-silicon TFT, compared with that of a single-crystal MOSFET, the technology is primarily used for small-screen TFT-LCDs [1-2]. Another factor that limits the use of the technology for large-screen TFT-LCDs is the device non-uniformity. When we fabricate a large number of poly-silicon TFTs on a substrate, there is a significant level of random fluctuation in both the mobility and the threshold voltage of poly-silicon TFTs [3-4]. While digital driving is imperative in large-screen Poly-Si TFT-LCDs, the TFT non-uniformity makes it difficult to design analog functions (specifically, current buffers) necessary to implement the digital driving.

This paper presents a circuit-level technique, called transistor slicing, to reduce the driving errors caused by the TFT non-uniformity in Poly-Si TFT-LCDs. After introducing the digital driving of Poly-Si TFT-LCDs, we quickly define what transistor slicing is and focus on analyzing the benefits of using transistor slicing. We then illustrate the effectiveness of transistor slicing by applying it in the design of current buffer for 14.1" XGA 6-bit Poly-Si TFT-LCD.

2. Digital Driving of Poly-Si TFT-LCDs

Figure 1 shows a digital Poly-Si TFT-LCD. All the functional blocks in the figure are implemented on a single glass substrate. The gate driver generates scan pluses to sequentially enable the gate lines. When a gate line is enabled, all pixel transistors in the corresponding line of pixels are turned on. Then, the image signals stored in the latch chain in the data driver are passed onto the line of pixels. The shift register chain in the data driver generates the timing signal necessary for the latch chain to capture the image signals coming from an external controller. A D/A converter converts the digital image signal stored in a latch into an analog voltage. When the output of a D/A converter is not sufficient for

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driving the panel, a current buffer is used to enhance the driving capability of the D/A converter. As the panel size (i.e., the panel load) increases, a larger current buffer is necessary.

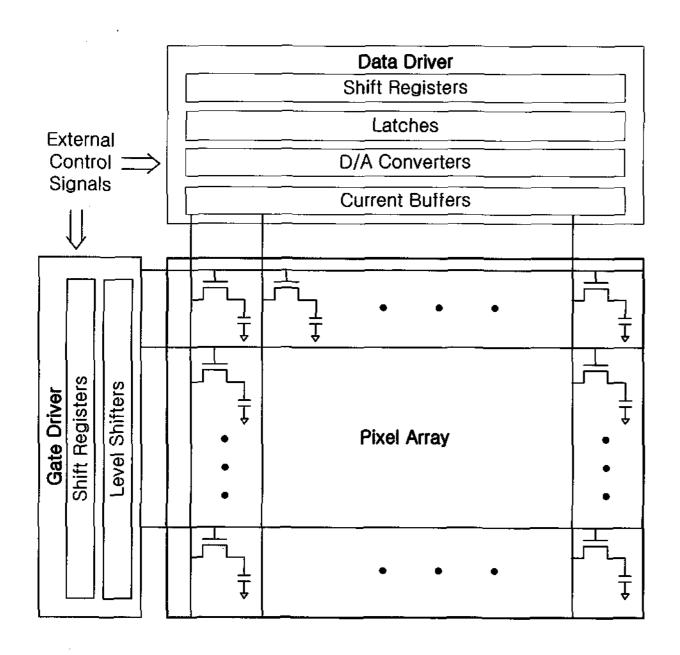


Fig. 1. Structure of digital Poly-Si TFT-LCD.

All the driving-circuit blocks, except for the D/A converters and current buffers, implement digital functions. If we look at a D/A converter in Poly-Si TFT-LCDs, it is typically the simple R-string, C-type, or a R-C hybrid type of converter. In such a D/A converter, a poly-silicon TFT is used only as a digital switch. Therefore, the performance of a D/A converter is relatively insensitive to TFT non-uniformity. However, designing a current buffer, which implements an analog function, is a challenge because of the non-uniformity of poly-silicon TFTs.

In conventional TFT-LCDs, we can design a high-performance current buffer using operational amplifiers because we use single-crystal MOSFETs to implement a buffer. However, we can use only the simple current buffer in Poly-Si TFT-LCDs because it must be implemented with poly-silicon TFTs. Consider the simplest form of current buffer that uses a single poly-silicon TFT (Figure 2). The purpose of a current buffer is to quickly charge or discharge the pixel capacitance so that the voltage across the capacitance becomes equal to V_{in} , which is the output voltage of a D/A converter. (To finish this job within a few microseconds, the width of a buffer should be in the order of 1000 microns in large-

screen Poly-Si TFT-LCDs; the minimum feature size supported in Poly-Si TFT-LCDs is typically a few microns.) Note the V_T drop between the gate and the source. The V_T drop itself is not a problem because we can compensate for the drop. The real problem is the non-uniformity of V_T . That is, if several thousands of current buffers in a Poly-Si TFT-LCD have all different V_T drops, it becomes difficult to compensate for the V_T drop.

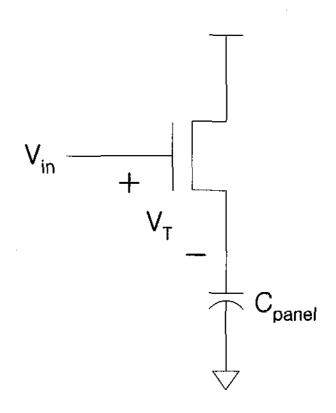


Fig. 2. Single-TFT current buffer.

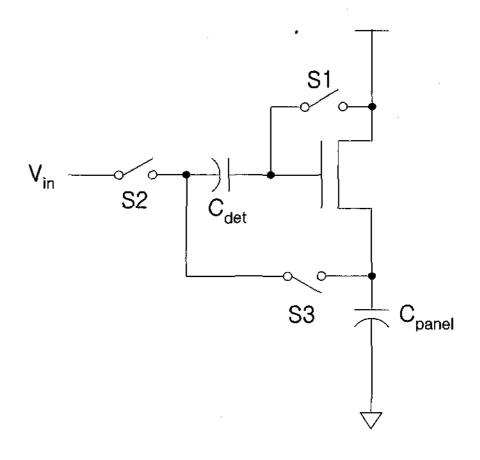


Fig. 3. Structure of V_T-compensating current buffer.

Figure 3 shows a buffer structure that was proposed for dealing with the problem [5]. The operation of this buffer is divided into two phases: detection and compensation phases. In the detection phase, we close the switches S1 and S3 and open the switch S2. Then the capacitor C_{det} is charged up to the threshold voltage of the TFT. In the compensation phase, we open the switches S1 and S3 and close the switch S2. Then, V_{in} plus V_{Cdet} is applied to the gate, and C_{panel} is charged up to V_{in} because of the V_{T} drop. (The figure shows only the n-channel side of CMOS circuits; in this paper, we

consider only the n-channel side because the idea of transistor slicing does not differentiate n-channel or p-channel TFTs.) As a result, in an ideal condition, the V_T term disappears and the V_T -compensating current buffer can significantly improve the accuracy of the driving in the presence of TFT non-uniformity. However, in real circuits, the buffer cannot perfectly detect and compensate for V_T of a TFT. Some portion of the V_T fluctuation may remain at the output of the buffer, which in turn can affect the accuracy of driving, and this is important in large-screen, high-gray-scale Poly-Si TFT-LCDs. The next section presents transistor slicing to reduce the effects of TFT non-uniformity further.

3. Transistor Slicing

The idea of transistor slicing is quite simple. Transistor slicing refers to the use of multiple smaller transistors in implementing a large transistor to deal with device non-uniformity. The technique is useful in designing poly-silicon TFT circuits that require large TFTs such as current buffers for Poly-Si TFT-LCDs.

Figure 4 illustrates the idea of transistor slicing. Specifically, Figure 4a shows a single large TFT (of width W), and Figure 4b shows the parallel connection of multiple smaller TFTs of equal size (i.e., the width of W/n). Each small TFT is called a TFT slice. The total currents flowing through the circuits in Figure 4 are:

$$I = \frac{1}{2} C_{ox} \mu_0 \frac{W}{L} (V_{GS} - V_{T0})^2$$
 (1)

$$I_{S} = \frac{1}{2} C_{ox} \frac{1}{n} \frac{W}{L} \sum_{i=1}^{n} \mu_{i} (V_{GS} - V_{Ti})^{2}$$
 (2)

In the above equation, C_{ox} is the oxide capacitance per unit area, L is the channel length, and μ and V_T represent the mobility and threshold voltage of a TFT, respectively. Also, n is the number of TFT slices, and i represents the ith TFT slice. Note that μ_i and V_{Ti} are random variables because we cannot accurately control the mobility and threshold voltage of poly-silicon TFTs. Therefore, I and I_s are also random variables.

The two equations (i.e., I and I_s) may look similar. However, the probability distributions of I and I_s can differ significantly from each other. We will investigate this difference in more detail. To be able to keep track of

the analysis mathematically, we assume that μ_i and V_{Ti} (i = 0, 1, ..., n) are mutually independent and identically distributed, respectively. This assumption implies that the random variations in the mobility and threshold voltage of poly-silicon TFTs do not depend on the size of a TFT.

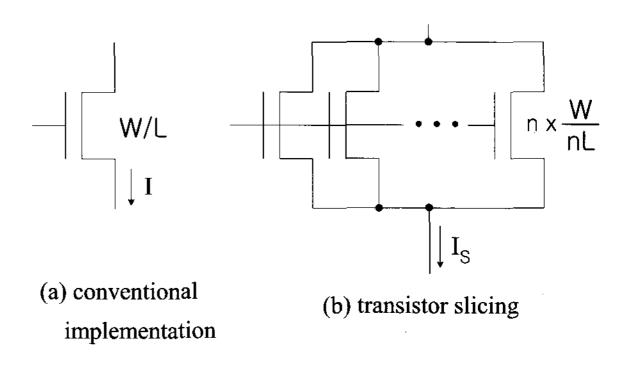


Fig. 4. Idea of transistor slicing: (a) conventional implementation and (b) transistor slicing.

Consider first that only the mobility of a TFT is a random variable. That is, we assume that we can accurately control the threshold voltage of a TFT. Then, by taking the standard deviation of Equations (1) and (2), we obtain:

$$\sigma(I) = \frac{1}{2} C_{ox} \frac{W}{I} (V_{GS} - V_{T0})^2 \cdot \sigma(\mu_0)$$
 (3)

$$\sigma(I_S) = \frac{1}{2}C_{ox}\frac{W}{L}(V_{GS} - V_{Ti})^2 \cdot \frac{1}{n}\sigma(\sum_{i=1}^{n}\mu_i)$$

$$= \frac{1}{2} C_{\text{ox}} \frac{W}{L} (V_{\text{GS}} - V_{\text{T0}})^2 \cdot \frac{\sigma(\mu_0)}{\sqrt{n}}$$
 (4)

where σ represents the standard deviation. From these two equations, we can see that the variance of I_s is smaller than that of I when n is greater than one. In fact, we get more variance reduction as we increase the number of TFT slices. This result shows that transistor slicing can be used as a method to reduce the non-uniformity in TFT mobility.

Next, consider that only the threshold voltage of a TFT is a random variable. Here, the mobility of a TFT is assumed to be a constant. Again, by taking the standard deviation of Equations (1) and (2), we have:

$$\sigma(I) = \frac{1}{2} C_{ox} \mu_0 \frac{W}{I} \cdot \sigma[(V_{GS} - V_{T0})^2]$$
 (5)

$$\sigma(I_S) = \frac{1}{2} C_{ox} \mu_0 \frac{W}{L} \cdot \sigma[\sum_{i=1}^{n} \frac{1}{n} (V_{GS} - V_{Ti})^2]$$
 (6)

Now if we make an additional assumption that V_{Ti} (i = 0, 1, ..., n) have normal distributions, we can make the sum-of-square terms in the right-hand-side of Equations (5) and (6) to have chi-square distributions by multiplying them with some constants. In other words, we can make $A \cdot \Sigma_i (V_{GS} - V_{Ti})^2 / n$ to have a chi-square distribution of degree n, where the value of A can be determined from the mean and variance of V_{Ti} [6]. Then, we can compare the variances of I and I_s, as we change the value of n, by referring to a statistical table. (In this study, the standard deviations of the mobility and the threshold voltage of a poly-silicon TFT are assumed to be 10 percent of their nominal values.) Figure 5 shows the results of comparison. The y-axis of the figure represents the relative reduction of the standard deviation of the drain current. The figure indicates that we can reduce the effects of the non-uniformity in TFT threshold voltage with transistor slicing. For example, with two TFT slices, the standard deviation of the drain current is reduced to about 70 % of that for the case where transistor slicing is not used.

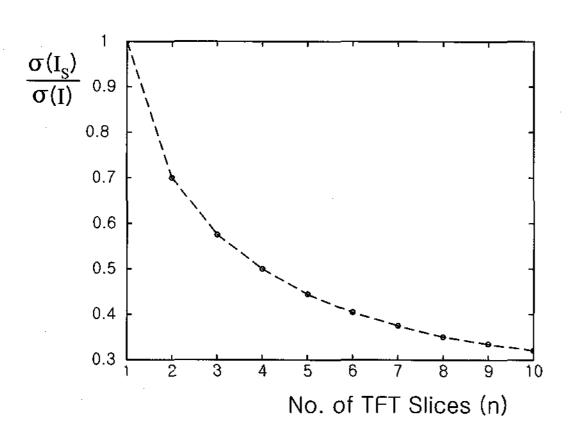


Fig. 5. Variance of drain current as a function of the number of TFT slices.

In real poly-silicon TFTs, both the mobility and threshold voltage are random variables. Again, by taking standard deviation of Equations (1) and (2), we can obtain:

$$\sigma(I) = \frac{1}{2} C_{ox} \frac{W}{L} \cdot \sigma[\mu_0 (V_{GS} - V_{T0})^2]$$
 (7)

$$\sigma(I_S) = \frac{1}{2} C_{ox} \frac{W}{L} \cdot \sigma[\sum_{i=1}^{n} \frac{1}{n} \mu_i (V_{GS} - V_{Ti})^2]$$
 (8)

Since an analytic evaluation is no longer possible, we use the Monte Carlo simulation method to evaluate Equations (7) and (8). That is, we evaluate the above equations using various samples of μ_i and V_{Ti} generated by drawing random numbers. The simulation gives a curve very similar to Figure 5, confirming that transistor slicing can be used to reduce the effects of random variations in TFT mobility and threshold voltage.

4. Current Buffer with Transistor Slicing

To evaluate the performance of transistor slicing, we use transistor slicing for the design of a current buffer for 14.1" XGA 6-bit Ploy-Si TFT-LCD. Figure 6 shows the current buffer structure with transistor slicing. Figure 7 illustrates the simulation environment that includes models for the pixel array as well as data and gate line parasitic resistances and capacitances.

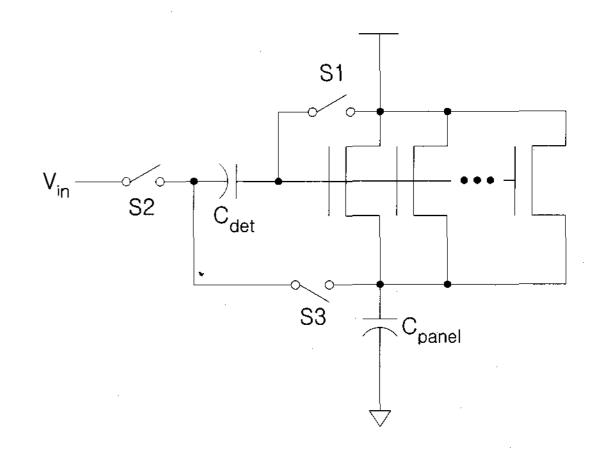


Fig. 6. Structure of V_T -compensating current buffer with transistor slicing.

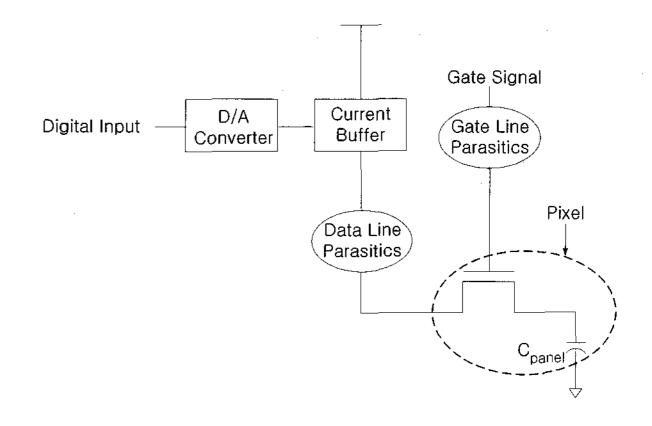


Fig. 7. Environment for dimulating friving securacy in Poly-Si TFT-LCD.

TABLE 1. Reduction of driving error with TFT slicing.

No. of TFT Slices	Overall Average Driving Error (%)	Standard Deviation of Driving Error (%)
1	100	100
2	83	65
3	67	55
4	67	55

We again perform Monte Carlo simulation using the HSPICE tool. A pixel is initially charged or discharged to the ground level. We, then, generate random samples of μ_i and V_{Ti} and evaluate the driving error when we drive the pixel to the gray scale of 0. After repeating this step many times, we calculate the mean and variance (as well as the distribution) of driving error. Then, we reset the simulation and characterize the driving error when we drive a pixel from the ground level to the gray scale of 1. If we keep doing this evaluation up to the gray scale of 63, we will get 64 values of mean driving error, one for each gray scale. Let's consider the mean and standard deviation of these 64 mean driving errors, which are referred to as the overall average driving error and the standard deviation of driving error, respectively.

Table 1 summarizes the simulation results. The first row of the table (i.e., the case of only one TFT slice) refers to the case where using transistor slicing is not used (Figure 3). The overall average driving error and the standard deviation of driving error for this case are used as references of comparison; all driving errors in the table are represented as percentages of these values. The remaining rows summarize the improvement in driving accuracy with transistor slicing (Figure 6). The second column of the table shows the reduction of overall average driving error, and the third column shows the reduction of standard deviation of driving error. The table clearly shows that transistor slicing can reduce the driving error caused by the non-uniformity in TFT mobility and threshold voltage. For example, when the number of TFT slices is three, the overall average driving error is reduced to 67 %, as compared with the case of not using transistor slicing; the standard deviation of driving error is also reduced to 55% with transistor slicing.

Table 1 also shows that the overall average driving error is not reduced further when the number of TFT slices is four or more. This phenomenon is not attributed to transistor slicing, but is attributed to the structure of the current buffer. That is, the driving error caused by the TFT non-uniformity decreases as the number of TFT slices increases, but the driving error caused by the capacitive coupling between the detection capacitor (C_{det}) and switches (S1, S2, and S3) does not change. In fact, the error caused by the capacitive coupling is a dominate cause for driving error when the number of TFT slices is four or more in the current buffer.

5. Conclusions

In this paper, we presented transistor slicing as a technique to reduce driving errors caused by the TFT non-uniformity in Poly-Si TFT-LCDs. In transistor slicing, we use multiple smaller TFTs to implement a large TFT. The paper analyzed the benefits of using transistor slicing and illustrated its effectiveness by applying it in a design of a current buffer for 14.1" XGA 6-bit Poly-Si TFT-LCD. The results clearly show that transistor slicing can reduce the effects of the TFT non-uniformity and improve the driving accuracy in Poly-Si TFT-LCDs. Transistor slicing does not add complexity to circuits design or fabrication.

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