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29GHz 국부 발진 신호용 MMIC 주파수 체배기의 설계 및 제작

(Design and fabrication of the MMIC frequency doubler for 29 GHz local oscillator application)

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요 약

밀리미터파 대역에서 안정적이고 경제적인 local oscillator (LO) 신호를 생성하기 위한 주파수 체배기를 설계 및 제작하였다. 주파수 체배기는 14.5 GHz를 입력받아 29 GHz를 생성하도록 설계되었으며, 측정 결과 14.5 GHz에서 S11이 -9.2 dB, 29 GHz에서 S22가 -18.6 dB 로 입력 측은 14.5 GHz에, 출력 측은 29 GHz에 매칭이 되었다. 변환손실의 경우 14.5 GHz에서 입력전력 6 dBm일 때 최소 값인 18.2 dB를 보였으며, 출력 단에서의 주파수 스펙트럼 특성은 14.5 GHz에서 15.2dBc의 값을 나타내었다. 또한 입력신호의 isolation특성은 10.5 GHz에서 18.5 GHz까지 주파수 범위에서 30 dB이상의 값을 보였다. 제작된 MMIC (Microwave monolithic integrated circuits) 주파수 체배기의 칩 사이즈는 1.5×2.2 mm^2 이다.

Abstract

We demonstrate the MMIC (monolithic microwave integrated circuit) frequency doublers generating stable and low-cost 29 GHz local oscillator signals from 14.5 GHz input signals. These devices were designed and fabricated by using the MMIC integration process of 0.1 ㎛ gate-length PHEMTs (pseudomorphic high electron mobility transistors) and passive components. The measurements showed S11 of -9.2 dB at 14.5 GHz, S22 of -18.6 dB at 29 GHz and a minimum conversion loss of 18.2 dB at 14.5 GHz with an input power of 6 dBm. Fundamental signal of 14.5 GHz were suppressed below 15.2 dBc compared to the second harmonic signal at the output port, and the isolation characteristics of fundamental signal between the input and the output port were maintained above 30 dB in the frequency range 10.5 GHz to 18.5 GHz. The chip size of the fabricated MMIC frequency doubler is 1.5×2.2 mm^2.

I. Introduction

Recently, the millimeter-wave communication systems, such as 38 GHz PCN (personal communication network) and 60 GHz wireless LAN (local area network), have been greatly focused because of the shortage in the frequency resource due to the rapid development of various telecommunication services and the requirement of high speed and mass data

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transmission capacity. For these millimeter-wave communication systems, the millimeter wave LO (local oscillator) signal is obviously necessary to convert RF (radio frequency) to IF (intermediate frequency). With an increase in frequency, it is very difficult to obtain a stable oscillation and to demonstrate the PLL (phase locked loop) circuits. To solve these problems, frequency multipliers are commonly used. These days, much effort is being made on fabricating the frequency doublers and triplers, which are adopted by 60 GHz wireless LAN, 76 GHz automotive radars and the signal sources for V/W band test instruments[1~3]. In this report, we also designed first one of frequency doubler to demonstrate LO of 60GHz wireless LAN by doubling 14.5GHz twice. The frequency multipliers utilize the non-linear characteristics of devices producing the harmonic signals according to the input frequency. The relation between the input and the output signals can be defined as shown in equation (1)

$$y(t) = a_1 x(t) + a_2\, x(t)^2 + a_3\, x(t)^3 \qquad (1)$$

, where $y(t)$, $x(t)$, a_i are the output signal, the input signal and the i-th order constant, respectively.

If a sinusoidal signal of $x(t) = A\cos(wt)$ is provided for an input wave form, the output spectrum of the fundamental and the harmonics[4] will be given by equation (2)

$$y(t) = \frac{a_2 A^2}{2} + \left(a_1 A + \frac{3a_3 A^3}{4}\right)\cos(wt) + \frac{a_2 A^2}{2}\cos(2wt) + \frac{a_3 A^3}{4}\cos(3wt) \qquad (2)$$

, where A, w and t are the amplitude of input signal, the angular frequency of signal and the elapsed time, respectively.

When we use the third term, $\frac{a_2 A^2}{2}\cos(2wt)$, for the multipliers, these are called the frequency doublers. Similarly, the frequency triplers use the forth term of $\frac{a_3 A^3}{4}\cos(3wt)$.

These frequency multipliers can be categorized into two types, such as the active and the passive multiplier[5,6]. The active multipliers normally show a higher conversion efficiency than the passive multipliers, such as in the cases of conversion gain and isolation characteristics.

Ⅱ. Design and Fabrication

First, we developed a MMIC library of active and passive device using our own integrated efforts of device process, modeling and characterization for 30~60 GHz applications. Based upon this library, we designed and fabricated the frequency doublers for this report.

For designing the MMICs, we used 0.1 ㎛ gate-length PHEMTs (pseudomorphic high electron mobility transistors) of 70㎛ x 2 (70 ㎛ gate width and 2 fingers) for the active devices. The SEM (scanning electron microscopy) planar view of a fabricated PHEMT is shown in figure 1. From these PHEMTs, we obtained the DC characteristics as follows; I_{dss} of 53.8㎃, transconductance (g_m) of 367.9 mS/㎜ and pinch-off voltage of -1.5 V. In figures 2 and 3, we illustrated DC current-voltage and transconductance charateristics of 70㎛x2 PHEMTs. Shown in figure 4 are the measured RF characteristics of fT (cut-off frequency) and fMAX (maximum frequency of oscillation) of the PHEMTs used for the library construction. Typical fT and fMAX of the PHEMTS were ~106 and ~160 GHz, respectively. The large-signal modeling for the fabricated PHEMTs were performed using the IC-CAP of EEHEMT1 model[7].

To produce more harmonic components, the gate bias point is set near the pinch-off voltage (V_{gs}=-1 V, V_{ds}=2 V). The input and the output ports were matched at 14.5 and 29 GHz, respectively.

In figure 5, we showed a schematic of the MMIC frequency doubler circuit used in this study. We produced the layouts using the ADS (Advanced Design System), and verified them by using the momentum simulation. The momentum simulation exhibited a

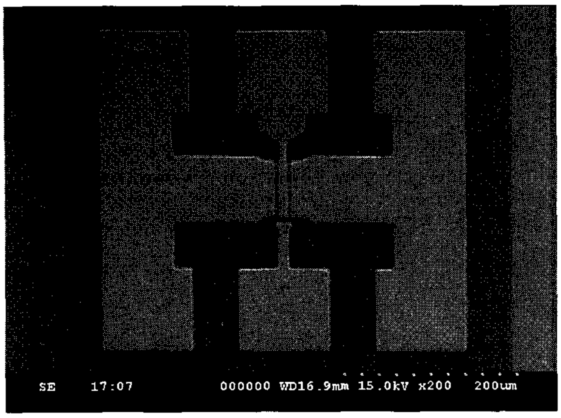


그림 1. 70×2 PHEMT의 SEM 사진
Fig. 1. SEM plan view of 70 ㎛×2 PHEMT (Lg=0.1 ㎛).

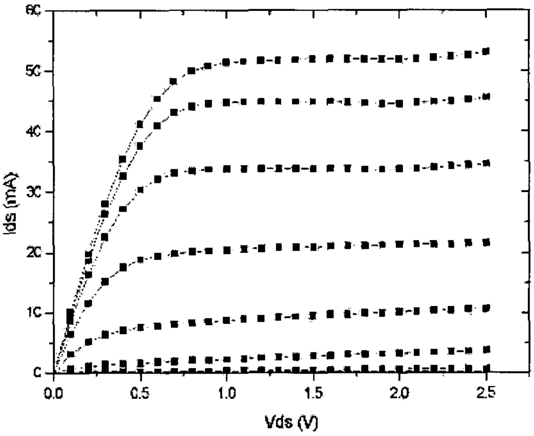


그림 2. 70 ㎛×2 PHEMT의 DC 전류-전압 특성
Fig. 2. DC current-voltage characteristics of 70 ㎛ ×2 PHEMT.

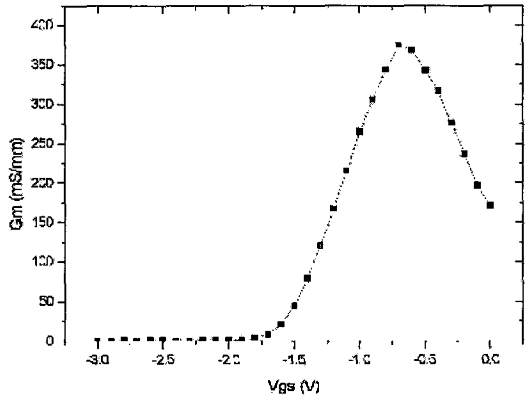


그림 3. 70㎛×2 PHEMT의 transconductance 특성
Fig. 3. transconductance of 70㎛×2 PHEMT.

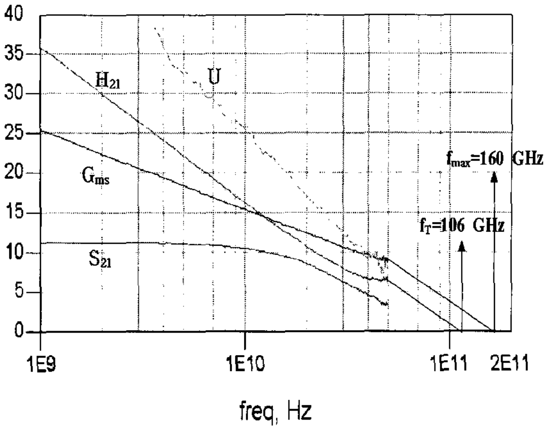


그림 4. 70㎛×2 소자의 RF특성 측정 결과
Fig. 4. Measured RF characteristics of 70㎛×2 PHEMT.

different matching condition with the schematic simulation. Therefore, the layout was modified iteratively until the momentum simulation results satisfy the matching state at 14.5 and 29 GHz. The final results of the momentum simulation are shown in figures 6 and 7. From the results of S-parameters simulation, S11 of -17.8 dB at 14.5 GHz and S22 of -11.7 dB at 29 GHz are obtained, respectively. When the input power is varied from -10 dBm to 10 dBm, a minimum conversion loss of 13.4 dB was obtained at a 4 dBm input power.

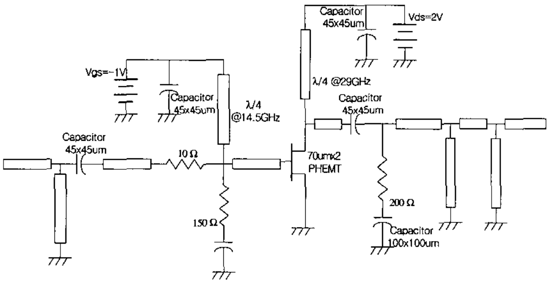


그림 5. 주파수 체배기의 회로도
Fig. 5. Schematic of the MMIC frequency doubler circuit.

The designed MIMIC frequency doublers were fabricated using our standard integration process[8,9] for the MMICs including the active and passive components. The fabricated chip size is 1.5x2.2 ㎟, and a plan-view micrograph of the fabricated doubler is shown in figure 8.

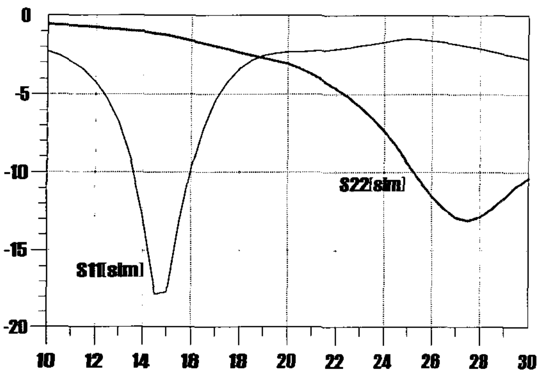


그림 6. S-parameter 시뮬레이션 결과
Fig. 6. Simulation results of S-parameter.

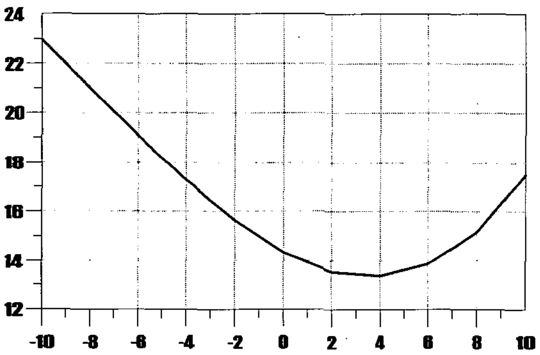


그림 7. 입력 전력에 따른 변환손실
Fig. 7. Conversion loss versus the input power.

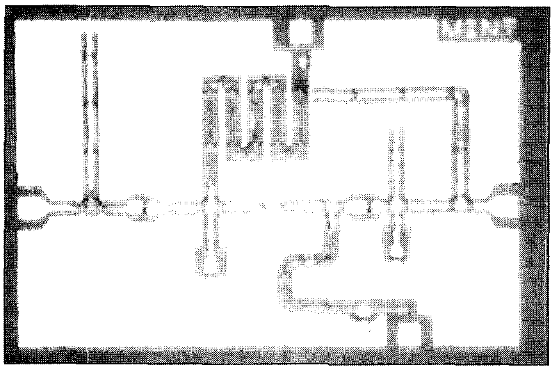


그림 8. 제작된 주파수 체배기의 사진
Fig. 8. Plan-view micrograph of the MMIC frequency doubler.

III. Measurements of RF characteristics

The input and output matching characteristics of the fabricated frequency doublers were measured by a on-wafer probing using the 8510C network analyzer and the MS2668C spectrum analyzer. First, we measured DC current-voltage characteristics of PHEMTs in the fabricated MMICs. From this, we obtained I_{dss} of 17 ㎃ and gm of 130 mS/mm. Compared to the PHEMT library described earlier, the drain current and transconductance were reduced by ~70 and ~65 %, respectively. It is believed that this was due to the process variation, such as gate recess etching time and Si3N4 passivation effect compared to the PHEMTs used in the library.

After this, the small signal characteristics were examined. From the measurement, we obtained S11 of -9.2 dB and S22 of -18.6 dB at 14.5 and 29 GHz, respectively. In overall, the S-parameter measurement results showed similar results with the simulation. However, the input matching peaks were shifted by ~3 GHz toward the high frequency. The difference between the measurement and the simulation result was due to the degradation in PHEMT performance of the fabricated MMICs, as discussed earlier. In figure 9, we illustrated the S-parameter spectra of the measurement and simulation results.

We also measured the conversion loss at various input powers and frequencies. For the measurements,

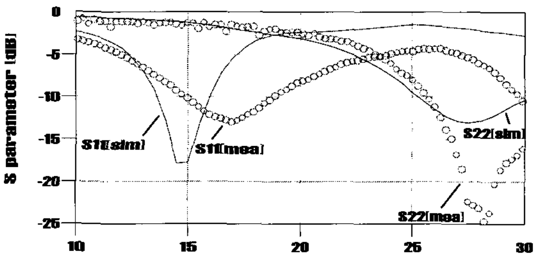


그림 9. 제작된 주파수 체배기의 S-parameter 측정결과
Fig. 9. S-parameter measurement and simulation spectra of the fabricated MMIC doubler.

14.5 GHz input signal was generated by an Agilent 83623B signal generator. The output signal was detected by an Anritsu MS2668C spectrum analyzer. In figure 10, we showed a measurement setup for measuring the conversion loss and the isolation characteristics of the fundamental signals between the input and the output port. By using this measurement setup, we measured the output power and isolation characteristics with the power of fundamental and second harmonic signal. The measurements were performed by fixing the input power at a 6 dBm and by varying input signal frequency.

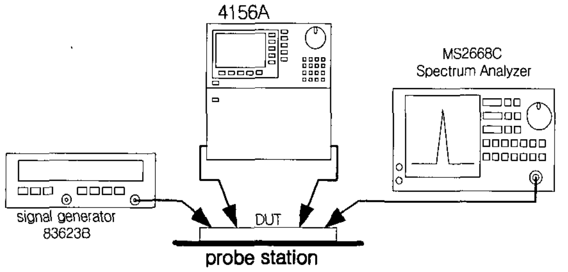
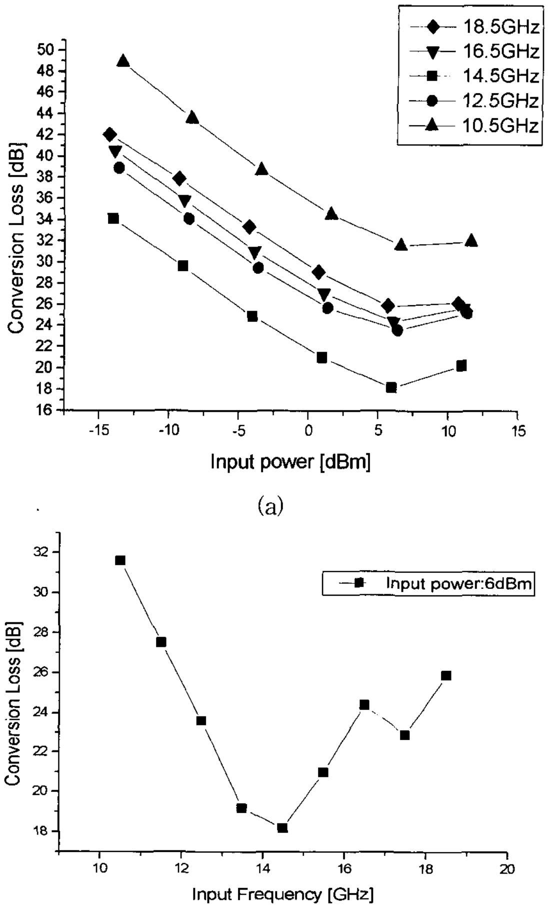


그림 10. 측정 장비 구성도

Fig. 10. A schematic of measurement system.

A minimum conversion loss of -18.2 dB was obtained under an input power of 6 dBm at 14.5 GHz. It is believed that, because the DC characteristics of PHEMTs in the MMIC was degraded than those of the library, the measured conversion loss was higher than expected in the simulation results. By using more reliable MMIC and PHEMT process, further investigation is under the work to demonstrate a comparable conversion loss with the simulation result. Shown in figures 11 (a) and (b) are the measured conversion loss versus the input frequency and the power, respectively.

The measurements also showed a maximum D/U (desired/undesired) ratio of 15.2 dBc at 14.5 GHz. The examined isolation of the fundamental signal was greater than 30 dB in the frequency range from 10.5 to 18.5 GHz. In figures 12 and 13, the measured output power spectra and isolation characteristics were presented, respectively.



(a)

(b)

그림 11. 입력전력(a)과 입력 주파수(b)에 따른 변환 손실

Fig. 11. Conversion loss versus (a) input power and (b) input frequency.

Finally, the phase noise of the frequency doublers was measured to examine the stability of the frequency-doubled signals. The measured phase noise of the input signal source was 86.7 dBc/Hz (300 ㎑ offset) at 14.5 GHz. When this input signal was provided for the doublers, the phase noise of the output signals was 83.4 dBc/Hz (300 ㎑ offset) at 29 GHz. As was measured, we observed no clear degradation in phase noise of the output signals. It is believed that this result was due to the fact that the phase noise of the signal source is not so sufficiently low. More accurate measurement is under the schedule by improving the phase noise performance of the signal generator.

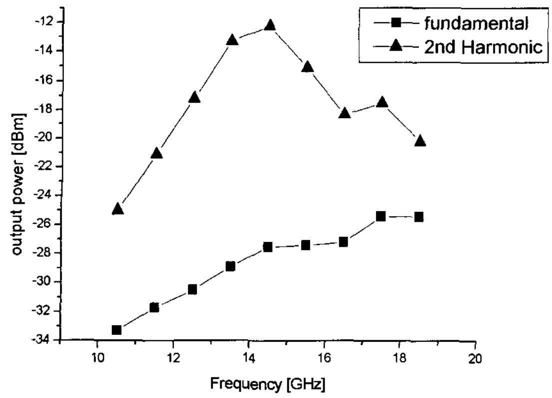


그림 12. 출력단의 주파수 스펙트럼

Fig. 12. Output power spectra of the fundamental and second harmonic signals.

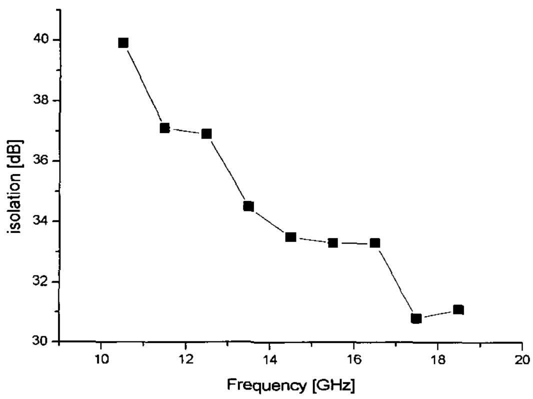


그림 13. 입력주파수에 따른 Isolation특성

Fig. 13. Isolation between input and output port versus frequency.

Ⅳ. Conclusions

We demonstrated the MMIC frequency doublers generating 29 GHz signals using the PHEMT-based technology. The fabricated devices showed the S11 of -9.2 dB and S22 of -18.6 dB at 14.5 and 29 GHz, respectively. The matching was shifted by ~3 GHz toward the high frequency region compared to the simulation result. The conversion loss was examined at various frequencies (from 10.5 to 18.5 GHz) and powers (from -10 dBm to 10 dBm). A minimum conversion loss of 18.2 dB was obtained under an input power of 6 dBm at 14.5 GHz. The measurement also showed a maximum D/U (desired/undesired) ratio of 15.2 dBc at 14.5 GHz. The examined isolation was greater than 30 dB, as measured from the fundamental signals in the frequency range from 10.5 to 18.5 GHz. It is believed that, because DC characteristics of PHEMTs in the MMIC was degraded than those of the library, the measured conversion loss was higher than expected in the simulation results.

References

[1] M. Funabashi, T. Inoue, K. Mauhshi, K. Hosoya, M. Kuzuhara, K. Kanekawa, Y. Kobayasi, “A 60GHz MMIC stabilized frequency source composed of a 30GHz DRO and A Doubler: IEEE MTT-S Intl. Microwave Symp. Digest , pp. 71-74, 1995.

[2] A. Werthof, H. Tischer, T. Grave, “High Gain PHEMT Frequency Doubler for 76GHz Automotive Radar”, IEEE MTT-S Intl. Microwave Symp. Digest vol. 1, pp.107-109, Pheonix, USA, May 2001.

[3] Matthew Morgan, Sander Weinreb, “A FULL WAVEGUIDE BAND MMIC TRIPLER FOR 75-110GHz”, IEEE MTT-S Intl. Microwave Symp. Digest, pp. 103-106, Pheonix, USA, May 2001.

[4] Behzad Razavi, “RF Microelectronics”, Prentice Hall, pp. 15, 1998.

[5] Yasushi Shizuki, Yumi Fuchida, Fumio Sasaki, Kazuhiro Arai, Shigeu Watanebe, “A K-band MMIC frequency doubler using resistive series feedback circuit”, IEICE Transactions on Electronics, V.E83-C No.5, pp. 759-766, May 2000.

[6] John Papapolymerou, Jack East, Linda P. B. Katehi, “W-band finite ground coplanar monolithic multipliers”, IEEE MTT, Vol.47 No.5, pp. 614-619, May 1999.

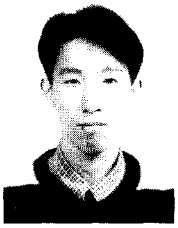
[7] IC-CAP User's Guide, Agilent.

[8] Seong-Dae Lee, Yeon-Sik Chae, Yong-Soon Yoon, Jin-Seub Yoon, Eung-Ho Rhee, Jin-Koo Rhee, “Studies on the MMIC Power Amplifier

using the AlGaAs/InGaAs /GaAs PHEMT", Journal of KITE vol. 38 SD. no. 1, pp. 30-36 Jan. 2001.

[9] Seong-Dae Lee, Sung-Chan Kim, Bok-Hyoung Lee, Woo-Suk Sul, Byeong-Ok Lim, Dan An, Yong-Soon Yoon, Sam-Dong Kim, Dong-Hoon Shin, Jin-Koo Rhee, "Design and Fabrication of the 0.1㎛ Γ-Shaped Gate PHEMT's for Millimeter-Waves", JKEES vol. 1, no. 1, pp. 73-78, May, 2001.

저자소개



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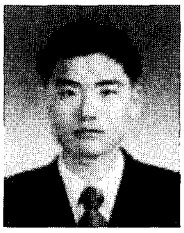

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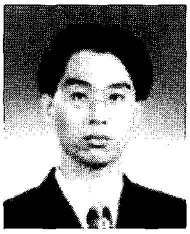

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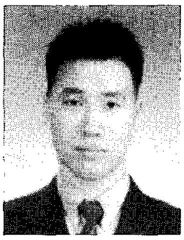

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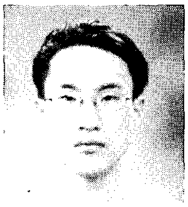

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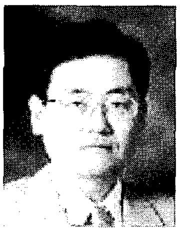

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