재수렴성 경로를 고려한 견실한 신호 전이 밀도 예측

김 동 호[†]·우 종 정[††]

요 약

전력 소모 예측에 필요한 신호 전이 밀도를 구하기 위하여, 세로 지연 모델에 대한 견실한 신호 전이 밀도 전파 방법이 제시된다. 세로 지연 모델을 위한 전력 예측은 전력 소모의 하한 경계값을 위한 적절한 기준이다. 입력 특성이 일반적으로 설계 단계에 알려져 있지 않기 때문에 광범위한 입력 특성에 대한 견실한 예측은 전력 소모에 대하여 매우 중요하다. 본 연구에서는 기존의 신호 전이 예측 방법에 대하여 입력 및 출력의 변이 특성을 분석하고 이러한 분석 결과에 근거하여 새로운 견실한 신호 전이 밀도 전파 방법을 제안한다. 실제 회로에 적용하기 위하여 전력 예측의 정확성에 크게 영향을 미치는 재수렴성 경로를 고려한 알고리즘을 제안 및 연구한다. 실험에 의하면 제안한 방법이 기존의 방법과 비교할 때 더욱 양호한 견실성 및 종래의 방식에 상응하는 정확성과 경과 시간을 보여준다.

Robust Signal Transition Density Estimation by Considering Reconvergent Path

Dongho Kim[†]·Jongjung Woo[††]

ABSTRACT

A robust signal transition density propagation method for a zero delay model is presented to obtain the signal transition density for estimating the power consumption. The power estimation for the zero delay model is a proper criteria for the lower boundary of power consumption. Since the input characteristics are generally unknown at design stage, robust estimation for wide range input characteristics is very important for the power consumption. In this paper, a conventional transition estimation method will be explored. And this exploration will be analyzed with the input/output signal transition behavior and used to propose the robust signal transition density propagation for the power estimation. In order to apply to practical circuits, the reconvergent path, which is crucial to affect the exactness of the power estimation, will be studied and an algorithm to take the reconvergent path into consideration will be presented. In experiment, the proposed methodology shows better robustness, comparable accuracy and elapsed time compared to the conventional methods.

키워드 : 전력 예측, 신호전이 밀도 전파, 재수렴성 경로, 회로분할

1. 서 론

With the advent of mobile computing, hot device and restricted battery life span, power estimation has been considered as one of the most urgent tasks to achieve low power consumption. Since the circuit reliability by the hot device is crucial obstacle to be tackled, the power estimation and the power analysis become more and more important aspect in VLSI design area. In CMOS circuits with negligible leakage current and short current, power is mainly dissipated during signal transition, which is caused by the charging and discharging of a load capacitance at each gate node.

Since the exact transition estimation of digital circuits is very difficult due to the unknown input behavior at design stage, the robustness of the transition density estimation for a wide range of input signals is very important to give a reliable power estimation result to the VLSI designer and to be used as a reference in logic synthesis [10]. There are two main streams in power estimation. These are the probabilistic approaches [1-4] and statistical approaches [5, 6]. It is known that even if the statistical approaches have good accuracy, they have large elapsed times to obtain the power estimation results. In contrast, the probabilistic approaches have a drawback for accuracy. Therefore the pursuing direction of the statistical approaches has focused on how to reduce the elapsed time and that of the probabilistic approaches are to improve accuracy of the

power estimation.

In this paper, the probabilistic approach will be dealt with and the statistical one [6] is implemented for comparison. And in order to apply on the real VLSI circuits, the consideration for reconvergent path will be explored and simple circuit partitioning algorithm will be proposed. In order to compute the signal probability on reconvergent paths, the suppressed exponent method [8] will be implemented.

2. ROBUST SIGNAL TRANSITION DENSITY PROPAGATION

As proposed in papers [1-4, 7], the power estimation method can be divided by two approaches. First one is to apply the operating frequency to each node's signal transition probability that is computed by propagating the probability of primary input signal through whole logic node to the primary output. Another one is to propagate the signal probability and the signal transition density simultaneously. If a temporal independence is assumed, the transition probability is expressed as follows,

$$P(y^{01}) = P(y^{10}) = P(y = 0)P(y = 1)$$
$$= (1 - P(y = 1))$$

where the P(y) for each 2-input gates is shown in table.

\<Table 1\> Signal probability computation for AND and OR gate.

	P (y = 0)	P (y = 1)
AND	$(1 - P_{x1} P_{x2})$	$P_{x1} P_{x2}$
OR	$(1 - P_{x1})(1 - P_{x2})$	$(1 - (1 - P_{x1})(1 - P_{x2}))$

And actual transition is twice of $P(y^{01})$ because the transition is only occurred during change of a state 0 to 1 and 1 to 0. After obtaining the signal transition probability, the estimated power consumption for each node can be computed by,

$$P(x_i) = \frac{F_c}{2} V_{dd}^2 P_t(x_i) C_i \qquad (1)$$

$$P_{total} = \sum_{x_i \in all-nodes} P(x_i) \qquad (2)$$

where F_c is the operating frequency and C_i is the total capacitance, which takes all fan-out load, at the output node and P_t is $2P(y^{01})$.

Since power estimation is obtained by multiplying the operating frequency with each node's transition probability, this power estimation method cannot consider the local transition density variation. In order to overcome this problem, transition density propagation method was proposed [1]. The transition density propagation is expressed by,

$$T(y) = \sum_{i=1}^{n} P(\frac{\partial y}{\partial x_i}) T(x_i) \qquad (3)$$

where $T(x)$ is the transition density which means the amount of transition in a given time interval. And $\partial y / \partial x$ is known as Boolean difference that is expressed by $\partial y / \partial x_i$ = $y |_{x_i = 1} \oplus y |_{x_i = 0}$. Since the probability of the Boolean difference means how much input change affects output signal change, equation (3) can be conceived that input signal transition density is propagated to output node by the probability of the Boolean difference.

However the paper [4] pointed out that there was some redundancy factor in equation (3) because the simultaneous signal transition effect was not taken into account. In their paper, they proposed a method to estimate signal transitions by introducing a normalized signal transition density. Even if the method, being introduced to overcome drawback of the conventional signal transition estimation method, reduces the simultaneous signal effect, using the normalized signal transition make the resulted value frail to signals with variable signal transition densities at a fixed signal probability.

There are two important aspects for exact power estimation, test vectors and power estimation model. In case of the test vector, the signal transition density, signal probability or signal transition probability or their combination have been used to estimate the signal transition density of each node and/or whole digital circuit. In papers [1, 4], the signal transition density and the signal probability were used by propagating two values through the whole circuit. It is obvious that the signal transition density and signal probability are independent each other; a signal with the specific signal probability has many different signal transition densities. It was said that the signal transition probability gives the maximum likelihood estimation of the signal transition density [7]. And the signal transition density can be governed by the signal probability and frequency as the equation (4).
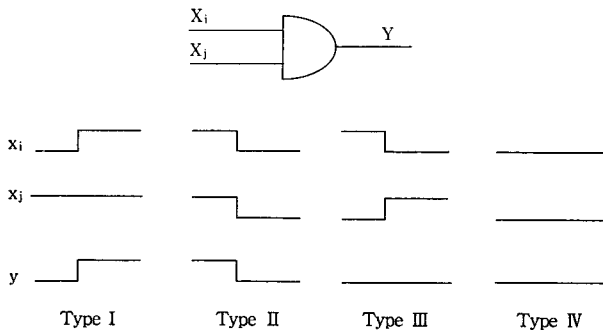
$$T(x) \le 2p(x)(1 - p(x)) * F_c \qquad (4)$$

where F_c is an operating frequency and p(x) is a probability of the signal x = 1.

Since primary input signals' characteristics are not determined in design stage, the power estimation method should be robust over whole range of signal probability and whole range of signal transition density at a certain signal probability.

As mentioned, the transition density propagation method [1] has some exactness problem because the simultaneous signal effects are not considered. In contrast to this, the Chou's method has bad robustness because the normalized transition density propagation method was used.

2.1 2-Input Signal Transition Density Propagation

(Figure 1) 4 types of signal transition density propagation

As shown in equation (3), density propagation equation can explain the density propagation behavior characteristic in gate level. From our observation, there is some redundancy factor in the process of transition density propagation. (Figure 1) shows the density propagation behavior of input and output signal for AND gate. In this figure, all input signals can be categorized as 4 types of group.

- Type I : all of the signal transition density should be propagated.
- Type II : Some of the signal transition density should be eliminated.
- Type III : All of input densities don't need to be propagated.
- Type IV : No signal transition density and no signal transition propagation.

Among 4 types, the propagation behavior of the type I and the type II has no simultaneous signal effect. Type III has been explained that there should be the additional consideration for redundancy [4]. From our observation, type II should be also taken into account for redundancy. One of relationships between input signal and output signal is shown in (figure 2). This figure shows that the output signal

transition, whose input signal transition is either 00 to 11 or 11 to 00, occurs once rather than twice, even if two input signal states change simultaneously; i.e., both signal transitions can not contribute to output signal transition separately.

From equation (3), the signal transition density propagation for 2-input AND gate can be expressed by,

$$
\begin{aligned}
T(y) &= P(x_2)\,T(x_1) + P(x_1)\,T(x_2) \\
&= (P(x_2^{01}) + P(x_2^{11}))\,T(x_1) + ((Px_1^{01}) \\
&\quad + P(x_1^{11}))\,T(x_2)
\end{aligned} \tag{5}
$$

If the term $T(x_i)$ is substituted by the term $2P(x_i)(1-P(x_i))F = 2P(x_i^{01})F$, the equation can be expressed by,

$$
\begin{aligned}
T(y) &= 2P(x_1^{01})\,P(x_2^{01})\,F + 2P(x_1^{01})\,P(x_2^{11})\,F \\
&\quad + 2P(x_1^{01})\,P(x_2^{01})\,F + 2P(x_1^{11})\,(P(x_2^{01})\,F
\end{aligned} \tag{6}
$$

Assuming that $P(x_i^{01})$ is $P(x_i^{10})$, the equation (6) can be derived by,

$$
\begin{aligned}
T(y) &= P(x_1^{01})\,P(x_2^{11})\,F + P(x_1^{11})\,P(x_2^{01})\,F \\
&\quad + P(x_1^{10})\,P(x_2^{11})\,F + P(x_1^{11})\,P(x_2^{10})\,F \\
&\quad + 2P(x_1^{01})\,P(x_2^{01})\,F + 2P(x_1^{10})\,P(x_2^{10})\,F
\end{aligned} \tag{7}
$$

input				output		
previous		current		previous	current	transition density
x_1	x_2	x_1	x_2	y	y	$D(y) = f(p(x_1),p(x_2))$
0	0	0	0	0	0	
		0	1	0	0	
		1	0	0	0	
		1	1	0	1	$p(x_1^{01})\,p(x_2^{01})$
0	1	0	0	0	0	
		0	1	0	0	
		1	0	0	0	
		1	1	0	1	$p(x_1^{01})\,p(x_2^{11})$
1	0	0	0	0	0	
		0	1	0	0	
		1	0	0	0	
		1	1	0	1	$p(x_1^{11})\,p(x_2^{01})$
1	1	0	0	1	0	$p(x_1^{10})\,p(x_2^{10})$
		0	1	1	0	$p(x_1^{10})\,p(x_2^{11})$
		1	0	1	0	$p(x_1^{11})\,p(x_2^{10})$
		1	1	1	1	

(Figure 2) Signal transition density propagation behavior
(2-input AND gate)

As shown in (figure 2) and the equation (7), the equation, being derived from the propagation equation by Najm, is exactly matched each other except for last two terms. And by comparing the (figure 2) and the equation (7), it is intuitively accepted that redundant terms are introduced into Najm's equation. Hence this redundant factor should be eliminated to minimize the simultaneous signal effect.

Lemma1.

When there are simultaneous signal effects in input signals, only one of them affects the process of the signal transition propagation.

Lemma 2.

Among the signals, being simultaneous signal effects, the smaller one is the dominant factor for the process of the signal transition propagation.

Theory 1.

If there is two signal transition, an equation, $\max \{P(x_2^{01})$ $T(x_1), P(x_1^{01})T(x_2)\}$, is the redundancy factor of a input signal transition to be propagated by the signal transition density propagation when the simultaneous signal transition is existed.

By considering Lemma 1, 2 and theory 1, the equation (7) can be expressed by,

$$
\begin{aligned}
RT(y) =\ & P(x_2)\,T(x_1) + P(x_1)\,T(x_2) \\
& - \max\{P(x_2^{01})\,T(x_1),\,P(x_2^{01})\,T(x_1)\} \qquad (8) \\
=\ & T(y) - \max\{p(x_2^{01})\,T(x_1),\,p(x_1^{01})\,T(x_2)\}
\end{aligned}
$$

2.2 n-Input Signal Transition Density Propagation

In the case of the n-input gates, there are much more complicated combination of simultaneous signal effects.

Before generalizing robust density propagation equation, several terminologies will be defined. If output signal y has $x_1, x_2, \cdots\cdots, x_n$ as primary inputs, several sets are defined as $S=\{1, 2, 3, \cdots\cdots, n\}$ and its subset $S_i = \{$all subsets of S and $n(\text{subset}) = i\}$. And a couple of algebraic lemmas should be defined.

Lemma 3. Empty set

If L = {0, 1},

then

$P(x_\phi^{ii})$ = 1 where i is an element of set L.

Lemma 4. Multiplication

If L = {0, 1},

then

$\prod P(x_{\{1,2,\cdots,m\}}^{ii}) = \prod\limits_{k=1}^{m} P(x_k^{ii})$ where i is an element of set L.

Lemma 5. Expansion

$\underset{i \in \{1,2,\cdots,m\}}{\beta} \{T(x_i)\} = \beta\{T(x_1), T(x_2), \cdots, T(x_m)\}$

where β can be displaced by max.

By considering Lemma 3, 4, and 5, the equation for n-input transition density propagation is as follows,

$$
\begin{aligned}
RT(y) =\ & \sum_{i=1}^{n} P(\frac{\partial y}{\partial X})\,T(y) \\
& - \sum_{i=2}^{n}\Bigg[\sum_{\forall j \in S_i}\prod_{j} P(x_j^{01}) \prod_{k \in (S_i - j,)} P(x_k^{ii}) \Big[\sum_{m=1}^{n} \qquad (9) \\
& T(x_m) - \sum_{m \in (S-j)} T(x_m) - \max_{m \subset j} \{T(x_m)\}\Big]\Bigg]
\end{aligned}
$$

where l can be '1' or '0' for AND or OR gate respectively.

3. Consideration FOR RECONVERGENT PATH

Even if it is assumed that all inputs of a given gate are independent each other, this can't be applied on real circuit due to its reconvergent paths. Hence the reconvergent paths should been taken into consideration to reduce the effect of the spatial correlation.
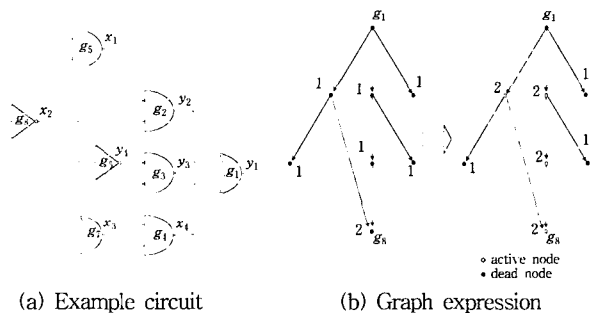
3.1 Circuit partitioning

Definition 1 Root vertex (node)

A vertex(r) is defined root vertex if a vertex(r) which is a member of a sub-graph(V) can reach every vertex $(v \in V)$ in the sub-graph; i.e. there is directed path from a root vertex to an arbitrary vertex in the sub-graph.

Definition 2 Reconvergent fan-out

A vertex is defined a reconvergent fan-out if more than two directed path exist from a root vertex(r) to a vertex $(v \in V)$ in the sub-grapth and any input to the root node of the directed path should not be shared.

o active node
• dead node

(a) Example circuit   (b) Graph expression

(Figure 3) Circuit partitioning

(Figure 3a) is a simple example circuit. In order to transform the circuit into a graph representation, each gate and connectivity corresponds to a vertex and an edge. The primary input and the gates are vertexes and the net, which is a connectivity between the gates, are represented by an edge. (Figure 3b) is a version of graph of the circuit of (figure

3a). From (figure 3a), the primary input for the gate output y_1 is $\{x_1, x_2, x_3, x_4\}$ and the reconvergent path is the net list from g_1 to g_8. In the probabilistic approach, the purpose of the circuit partitioning is to identify the primary inputs, which should be spatially independent each other, and the reconvergent path.

(Figure 3b) shows the transformed graph representation of the (figure 3a) and the resultant graph representation after applying the circuit partitioning algorithm. The active nodes of the (figure 3b) represent the reconvergent fan-out node and the nodes that are on the reconvergent path.

The pseudo-code for the circuit partitioning algorithm that detects the reconvergent path is presented in (figure 4). In the circuit partitioning algorithm, the function Search-Increase() is recursively called by decreasing the current depth to traverse every node from the root node within DEPTH. For the child nodes of the root node, a pathcount is assigned to identify each path. The pathcount is assigned only at the child nodes of the root node, which means that all paths from a child node, which is located under root node, has the same pathcount ((3) ~ (7)). If the search routine meet unvisited node, hit number of that node is increased to be referred as reconvergent fan-out. If the search routine meet visited node and the node was hit from the path other than current path, the hit number of the node is also increased ((8) ~ (11)). The function SearchIncrease() is recursively called for the child gates DEPTH away from the root gate. For the child node whose hit number is greater than 1, the routine will exit ((12) ~ (14)). After running this recursive function, any gate whose hit number is greater than 1 is considered as a reconvergent fan-out node. In this function, the reconvergent fan-out can be separated. Even if the reconvergent fan-out is separated, the function that can identify which nodes are members of the reconvergent path from the reconvergent fan-out to root node or which nodes can be primary inputs is needed. (Figure 4) and (Figure 5) show how the SeachUpdate procedure works. The procedure needs two pairs of temporal array. First array is used for storing every node information and hit number within the depth span from the root node. Second array pair is used to update the hit number and eliminate unwanted nodes. Other function is to sort the stored nodes with respect to the depth position, which can make the polynomial parameter being computed from the reconvergent fan-out to the root node. In the procedure of the hit number update, the hit number is propagated from the reconvergent fan-out node to the root node.

```
SearchIncrease (netlist, n_i, DEPTH)
(1)  increase c_depth by 1
(2)  foreach n_j ∈ child_i
(3)    if c_depth = DEPTH 1 then
(4)      increase pathcount
(5)    else
(6)      path_j = path_i
(7)    endif
(8)    if hitj = 0 or path_j ≠ path_i then
(9)      increase hit_j by 1
(10)     T_i ← n_j
(11)   endif
(12)   if c_depth < DEPTH and hit_j < 2 then
(13)     call SearchIncrease (n_j, DEPTH)
(14)   endif
(15) endfor
```

(Figure 4) Pseudo-code for the SearchIncrease procedure.

DEPTH : search depth.

n_i : gate i.

child$_i$: set of child gate of n_i (gates whose output is connected to the input of gate i).

hit$_i$: hit number of gate i. (initially, hit$_i$ = 0 for all i)

path$_i$: path number of gate i. (initially, path$_i$ = 0 for all i)

c_depth : current depth.

T_i : Tree of gates within the depth of DEPTH from the root gate i.

Pathcount : count for paths. Each fanin of the root gate i has a distinct path counter number.

```
Rec_i : set of nodes along the reconvergent paths to gate i.
SearchUpdate
       (1)  foreach nj ∈ T_i from bottom gate to the root gate
       (2)     if there exists n_k childj such that hit_k > 1 then
       (3)       Rec_i ← n_j
       (4)     end
       (5)  endfor
```

(Figure 5) Pseudo-code for the SearchUpdate procedure.

Property 1.

If any node is on the reconvergent path, the updated hit number is more than 1.

3.2 Parker-McCluskey Method Application

The Parker-McCluskey method [9] was introduced to generate a polynomial that represents the probability that the gate output is 1, for a gate in the circuits. In this computation, all propagated polynomial through the logic circuits are governed by definition 1.

Definition 3. Given Polynomial $F(x_1, \cdots, x_N)$, the function supexp(F) is defined as the polynomial resulting from replacing each $x_i^k \in F$ with x_i for all $k > 1$.

For example, if $F = x_1^2 + x_2 x_3$, supexp(F) is expressed as $x_1 + x_2 x_3$. In the case of applying the Parker-McCluskey method on probability computation, the probability of a polynomial $F(x_1, \cdots, x_N)$ can be expressed as $F(P(x_1), \cdots, P(x_N))$. In the subgraph, which is partitioned by the algorithm, the reconvergent fan-out is kept as variable until computation of the root node and other input is substituted with its signal probability. By using this, we can reduce the complexity of the polynomial that expresses the signal probability.
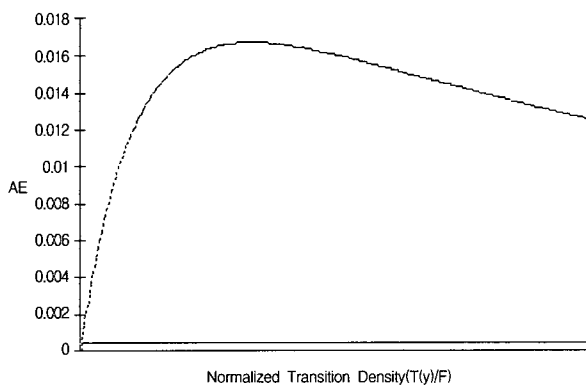
3.3 Update The Signal Transition Density

As shown in previous part, the signal probability is obtained by taking the reconvergent path into consideration. In this paper, the signal probability and the signal transition density is propagated through the whole circuit node from the primary input to the primary output node. Hence the signal transition density at the node, which has reconvergent paths under cone influence area, should be updated by the updated signal probability. In this paper, the signal transition density can be updated by equation (10).

$$RT_{new}(y) = RT_{old(y)} \frac{P_{new}(y^{01})}{P_{old}(y^{01})} \qquad (10)$$

where RT_{old} and P_{old} is obtained without considering the reconvergent path and P_{new} is computed by the exponent suppressed method to take reconvergent path into account.

4. SIMULATION AND RESULT

The proposed transition density propagation uses signal probability and the signal transition density to compute the signal transition density in CMOS circuits. Accurate and

(Figure 6) Absolute error comparison for a fixed signal probability (2-input AND gate)

robust computation of the signal transition density is very crucial role in power estimation because this is not only for measuring the exact density propagation but also for being used in low power logic synthesis as an objective function.

However, it is known that exact power estimation is NP-hard [1]. In practice, the input characteristics can't be determined when power estimation is computed. In our observation, the performance of power estimation should be evaluated by how much accurate power estimation is obtained for a certain gate type and for various signals' probability and wide range of signal transition densities for a certain signal probability. Hence our experiments considered this aspect by varying the input signal probability as forced data of primary input and by varying the input signal transition density for a certain signal probability. In this experiments, the ISCAS-85 combinational benchmark circuits were used. We guess that the good robustness and accuracy for this kind of experiments can guarantee the good performance for real logic circuits. In this experiments, the proposed signal transition density estimation method, Chou's method [4] and the time-parallel simulation approach [7] are implemented by C language. The simulation approach used the random signal as primary input signals of benchmark circuits whose probability and signal transition density is variable. First the experiments applied to 2-input gate to show the robustness. In this experiments, input signal probability is fixed to 0.5 while the normalized signal transition density is varied from 0.5, maximum value, to 0.125. And the resulted absolute errors between the proposed method and others were compared. (Figure 6) shows that while proposed method is more accurate after the normalized signal density (= 0.49), the resulted error of ATDP (dash line) is more accurate only in the range of 0.5 and 0.49.

<Table 2> shows the absolute error of Chou's method (ATDP) and the proposed method (RTDP) on the basis of the timeparallel switching activity estimation. In this experiment, values in the second row are the signal probability and the signal transition density is fixed at 0.5(signal transition density/FREQ). <Table 2> shows that both methods have similar accuracies for estimating the transition density. In contrast to this result, <table 3> shows that the proposed method has better accuracy and more stable result comparing to the Chou's method. In case of elapsed time, the Chou's method is a little better but the proposed method is comparable.

〈Table 2〉 Absolute error comparison at fixed signal transition density (SP : Signal probability)

SP	RDTP			ADTP			Elapsed Time
	0.50	0.25	0.75	0.50	0.25	0.75	
cla8	0.00260	0.00364	0.05116	0.00199	0.00340	0.05055	0.86598
c432	0.04382	0.08462	0.04213	0.04354	0.08480	0.04329	0.85281
c499	0.00325	0.00255	0.00110	0.00277	0.00289	0.00287	0.94881
c1355	0.01643	0.01997	0.01521	0.01614	0.02013	0.01621	0.79336
c1908	0.01674	0.01770	0.00710	0.01591	0.01788	0.00717	0.87809
c2670	0.00939	0.02100	0.09542	0.01059	0.02236	0.09396	0.90054
c3540	0.01075	0.00655	0.00571	0.00828	0.00564	0.00685	0.88002
c6288	0.06232	0.02981	0.03490	0.07391	0.04280	0.03741	0.83142
c7552	0.01516	0.02826	0.00977	0.01403	0.02997	0.00865	0.92343
Average	0.02005	0.02379	0.02917	0.02080	0.02554	0.02966	

〈Table 3〉 Absolute error comparison at fixed signal probability (NTD : Normalized Transition Density)

NTD	RTDP			ATDP		
	0.45	0.4	0.35	0.45	0.4	0.35
cla8	0.00305	0.00335	0.00238	0.05945	0.12458	0.19544
c432	0.04364	0.04318	0.04578	0.00457	0.04064	0.09004
c499	0.00470	0.00405	0.00356	0.06368	0.14703	0.25099
c1355	0.01737	0.01702	0.01644	0.02166	0.06636	0.11841
c1908	0.01520	0.00785	0.01498	0.02117	0.06224	0.10876
c2670	0.00943	0.00890	0.00960	0.05201	0.09771	0.15089
c3540	0.01021	0.01107	0.01233	0.04065	0.09632	0.18753
c6288	0.06694	0.06649	0.06713	0.15116	0.24208	0.35447
c7552	0.01524	0.01508	0.01549	0.03414	0.08808	0.14805
Average	0.02064	0.01967	0.02085	0.04983	0.10723	0.17829

<Table 4> showed that the depth length could affect the estimation accuracy. In case of the relationship between depth length and the estimation accuracy, even if the depth length is not exactly proportional to the estimation accuracy, the longer length can improve the estimation accuracy.

〈Table 4〉 Absolute error comparison for variable search depth (SP=0.5 & NSTD=0.5).

Length	3	4	10
cla8	0.00770	0.01178	0.00921
c432	0.00654	0.00755	0.04378
c499	0.00325	0.00250	0.00143
c1355	0.00141	0.00113	0.00238
c1908	0.00280	0.00441	0.01344
c2670	0.01070	0.00827	0.00233
c3540	0.06918	0.06575	0.03132
c6288	0.05273	0.05273	0.02327
c7552	0.01227	0.01112	0.00572
Average	0.01851	0.01836	0.01476

5. CONCLUSION

In this paper, we explored the relationship between the transition density propagation equation, being derived from Najm's, and the behavior of the signal transition density propagation for 2-input gate. The redundancy factor that was obtained by analyzing 2-input gate was applied to n-input gate. By using this exploration, the robust signal transition density propagation methodology was proposed. And the circuit partitioning algorithm was proposed to take reconvergent paths into account. In experiment, we showed that the proposed methodology has more robustness and comparable accuracy not only for the 2-input gate but also for ISCAS-85 benchmark circuits. In addition, we showed that the search depth is closely related to the estimation accuracy. However its application is restricted because the proposed method is focused on the zero delay models. Hence we should explore the method that can apply to real delay model in the future.

6. REFERENCES

[1] F. Najm, "Transition density : a new measure of activity in digital circuits," *IEEE Transaction on Computer Aided Design*, pp.224-228, November 1993.

[2] A. Ghosh, S. Devadas, K. Keutzer, and J. White, "Estimation of average switching activity in combinational and sequence circuits," *ACM/IEEE Design Automation Conf*, pp.253-259, 1992.

[3] J. Monteiro, S. Devadas, B. Lin, C-Y. Tsui, M. Pedram, and A. Despain, "Exact and approximate methods of switching activity estimation in sequential circuits," *Intl. Workshop on Low Power Design*, Napa Valley, 1994.

[4] T. Chou, K. Roy, and S. Prasad, "Estimation of circuit activity considering signal correlations and simultaneous Switching," *IEEE/ACM International Conference on Computer Aided Design*, Page(s) : 300-303, 1994.

[5] R. Burch, F. Najm, P. Yang, and T. Trick, "McPOWER : a Monte Carlo approach to power estimation, "*IEEE/ACM International Conference on Computer-Aided Design*, pp. 90-97, 1992.

[6] K. Kapp, M. Buhlder, D. Dallmann, and U. G. Baitinger, "TESA : Timeparallel Estimation of Switching Activity under a Real Delay Model," *IEEE International Conference on Electronics, Circuits and Systems*, pp.233-236, 1998.

[7] Q. Wu, M. Pedram, and X. Wu, "A Note on the Relationship Between Signal Probability and Switching," *Proceedings of the ASP-DAC '97 Asia and South Pacific*, pp.117-120, 1997.

[8] J. Costa, J. Monteiro, and S. Devada, "Switching activity estimation using limited depth reconvergent path analysis," *International Symposium on Low Power Electronics and Design*, pp.184-189, 1997.

[9] K. Parker and E. McCluskey, "Probabilistic Treatment of General Combinational Networks," *IEEE Transactions on Electronics Computers*, C-24, pp.668-670, 1975.

[10] R. Panda and F. Najm, "Technology-dependent Transformation For Low Power Synthesis," *ACM/IEEE Design Automation Conference*, pp.650-655, 1997.

김 동 호

e-mail : donghkim@ece.utexas.edu
1990년 경북대학교 전자공학과 학사.
1992년 경북대학교 전자공학과 석사.
1992년~1997년 LG전자 주임연구원.
1997년~2001년 Univ. of Texas at Austin
　　　　　 전기 컴퓨터 공학과 박사.
1998년~1999년 AMD Software Test Engineer.
2001년~현재 Intel Senior Engineer
관심분야 : PowerEstimation, Low Power Synthesis 및Computer
　　　　　 Arithmetic

우 종 정

e-mail : jwoo@cs.sungshin.ac.kr
1982년 경북대학교 전자공학과 학사
1982년~1988년 산업연구원 책임연구원.
1988년~1993년 Univ. of Texas at Austin
　　　　　 전기 컴퓨터 공학과 석사 및 박사
1998년~1999년 Univ. of Texas at Austin
　　　　　 전기컴퓨터공학과 Visiting Scholar
1993년~현재 성신여자대학교 교수.
관심분야 : 병렬처리, 컴퓨터구조, 멀티미디어시스템, 전자상거
　　　　　 래, CAD