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# 고속 DRAM 모듈 설계에 대한 전원평면의 임피던스 계산

# (Impedance Calculation of Power Distribution Networks for High-Speed DRAM Module Design)

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요 약

본 논문에서는 DRAM 모듈의 전원 평면에 대한 효과적인 설계 방법을 제시하였고 그 방법은 다음과 같이 세 단계로 구성되어 있다.

1) PEEC 등가회로를 이용한 2D 전송선 구조로 전원평면의 모델링 및 해석.

2) 측정값 비교를 통한 해석 결과 검증.

3) 전원 평면의 물리적 파라미터를 이용한 설계 가이드 제시.

제시한 내용을 바탕으로 하여 DRAM 모듈에서 전원 및 접지평면 성능을 안정화를 이루기 위한 효과적인 De-coupling 커패시터의 용량과 개 수를 결정하는 방법을 기술하였다. 이 설계 방법론은 스트립 구조 및 de-coupling 커패시터를 갖는 DRAM 모듈에서 효과적으로 사용할 수 있다.

**Abstract**

A systematic design approach for power distribution network (PDN) is presented aiming at applications to DRAM module designs. Three main stages are comprised in this design approach: modeling and simulation of a PDN based on a two-dimensional transmission line structure employing a partial element equivalent circuit (PEEC); verification of the simulation results through comparison to measured values; and design space scanning with PDN parameters. Impedance characteristics for de-coupling capacitors are analyzed to devise an effective way to stabilize power and ground plane performance within a target level of disturbances. Self-impedance and transfer-impedance are studied in terms of distance between circuit features and the size of de-coupling capacitors. A simple equation has been derived to find the de-coupling capacitance values yielding impedance lower than design target, and thereby reducing the overall computation time. The effectiveness of the design methodology has been demonstrated using a DRAM module with discrete de-coupling capacitors and a strip structure.

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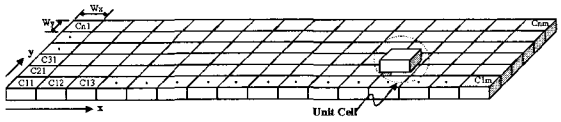
## I. Introduction

Noise in power distribution nets (PDN) sets the performance limit of digital systems as their speed increases with decreasing supply voltage and signal

swing. One of the major design concerns is to secure good power supply characteristics with lower simultaneous switching noise (SSN) [1]. It is required to have a precise modeling of PDN and evaluation of physical behavior using prototypes. The most important elements are the impedance of power/ground planes of multi-layer printed circuit boards and de-coupling capacitors in the design of PDN for high-speed digital systems. Difficult problems such as resonance in PDN become extremely difficult to solve without practical approaches dealing with PDN impedance and de-coupling capacitors [2].

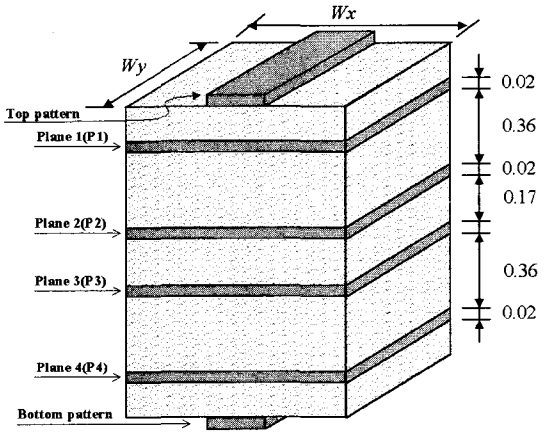
Some methods have been proposed to handle resonance problems in PDN [3-5]: de-coupling capacitor in PDN; control of thickness of conductors and PCB materials such as FR-4; compensation of loss in dielectrics and conductors. These methods, however, are mainly focused on the design of multi-chip modules, general printed circuit board structure and standard packages. Due to the strict standardization of DRAM modules, the application of these approaches to DRAM module PDN designs demands additional modification and fine tuning to get optimal design parameters such as layer assignment, location and size of de-coupling capacitors.

This paper presents an efficient design methodology of PDN for DRAM modules operating up to 500MHz. Three main stages are comprised in this design approach. It begins with modeling and simulation of a PDN based on a two-dimensional transmission line structure employing a partial element equivalent circuit (PEEC) [6,7]. The second stage is verification of the model through comparing the simulation results to measured values; and finally it performs scanning of design space with a simple equation finding viable capacitance values lower yielding impedance lower than a target level. Three models are studied in the first stage: RLCG model of a unit power plane cell with R and G components having frequency dependency; W-element unit cell model of HSPICE; and finally power plane unit cell model without frequency dependency in R and G components.




(a) segmentation of a power plane

(a) 전원평면 셀 분할




(b) PCB layers of a unit cell

(b) 단위 셀의 PCB 층 구조

그림 1. 전원평면의 단위 셀 구성: (a) 전원평면 셀 분할; (b) 단위 셀의 PCB 층 구조

Fig. 1. Cell network of power plane: (a) segmentation of a power plane; (b) PCB layers of a unit cell.

In the second stage, evaluation boards have been fabricated to verify the simulation results. The third stage of this design methodology is to verify the model through comparing the simulation results to study addresses the application and analysis of the performance of this model in a practical DRAM module. All the possible location and size of de-coupling capacitors are evaluated in terms of power plane impedance changes and thereby the noise elements in the planes. A simple equation has been derived speeding up calculation of PDN impedance. A PDN for DRAM modules is used as a running example. The Section 2 of this paper presents a modeling and measurements based on

PEEC methods. The Section 3 describes the effect of de-coupling capacitors in PDN in terms of impedance. Experimental results of impedance characteristics of PDN in a DRAM module are also demonstrated, and finally Section 4 draws a conclusion.

## Ⅱ. Analysis of Power/Ground Planes

We now turn to the modeling problem of power and ground planes. A power plane is divided into n(m unit cells, each of which is represented by an equivalent circuit. Computation results based on this model are compared to measured values from an evaluation board.

### 1. Unit Cell Model

A unit cell of PDN is an element of an $n \times m$ array of a power or ground plane. Figure 1a shows the structure of a two-dimensional array of unit cells. It has n cells in the $x$ direction and $m$ cells in the $y$ direction, respectively. The layer assignment of entire cells is illustrated in Figure 1b, where the layers $P_1$ and $P_3$ are for $V_{DD}$ or $V_{REF}$, and the layers $P_2$ and $P_4$ are ground planes, respectively. The $V_{DD}$ plane ($P_1$) and ground plane ($P_2$) form a micro-strip structure, and $P_3$ and its surrounding ground planes provide with a strip plane structure. The size of unit cells determines overall computation time and precision of the model estimation. Here the unit cell size is determined based on the effective electrical length of signals using the following equation:

$$Unit\ cell\ size = \frac{1}{N} \bullet \frac{v_0 t_r}{0.35\sqrt{\varepsilon_r}} \ [m] \tag{1}$$

Here $\varepsilon_r$ is the dielectric constant of FR-4, $v_0$ is the speed of light in vacuum, $t_r$ is the pulse rise time, and N is a number. Generally, N is greater than 10. In this paper, in order to obtain more accurate simulation results, N is set as 50.

The values of equivalent circuits of a unit cell shown in Figure 1b are derived using the following equations. Capacitance between two parallel plates is given as follows:

$$C = \frac{\varepsilon_0 \varepsilon_r w}{d} \ [F/m] \tag{2}$$

Here $w$ represents the width of a unit cell, $d$ is the distance between two parallel plates. The velocity of a wave traveling between the plates can be described in two ways: a function of the speed of light and the dielectric constant of FR-4, and an LC delay function of the equation (4).

$$v = \frac{v_0}{\sqrt{\varepsilon_r}} \ [m/sec] \tag{3}$$

$$v = \frac{1}{\sqrt{LC}} \ [m/sec] \tag{4}$$

Here $v_0$ is the speed of light in vacuum. From the equations (3) and (4), parallel plate inductance can be obtained as follows.

$$L = \frac{\varepsilon_r}{{v_0}^2 C} \ [H/m] \tag{5}$$

The values of C and L between layers $P_1$ and $P_2$ can be calculated. Let $C_1$ and $C_2$ be capacitance of layers $P_2$ and $P_3$ and that of layers $P_3$ and $P_4$, respectively. Then the capacitance associated with $P_3$ is capacitance $C_{P3} = C_1 // C_2$. Inductance can be obtained in the same fashion. Suppose $L_1$ be the inductance between $P_2$ and $P_3$, and $L_2$ be the inductance between layers $P_3$ and $P_4$, then inductance associated with $P_3$, $L_{P3} = L_1 // L_2$. Resistance component $R_{DC}$ that does not depend on frequency changes can be represented as follows.

$$R_{DC} = 2\frac{\rho}{wt} \tag{6}$$

Resistance components depending on frequency changes are mainly due to skin effect.

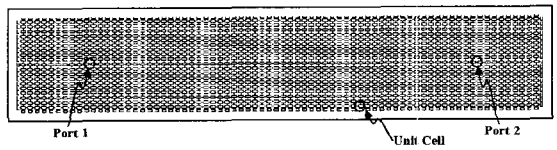
$$f_s = \frac{\rho}{\pi \mu (t/2)^2} \tag{7}$$

$$R(f) = R_{DC}\left(\frac{f}{f_s}\right)^{1/2} \tag{8}$$

Here $\rho$, $\mu$, w and t are the resistivity, magnetic permeability, width and thickness of a conductor, respectively. $f$ and $f_s$ are the operating frequency and skin effect frequency. Dielectric loss can be represented in terms of operating frequency and capacitance.

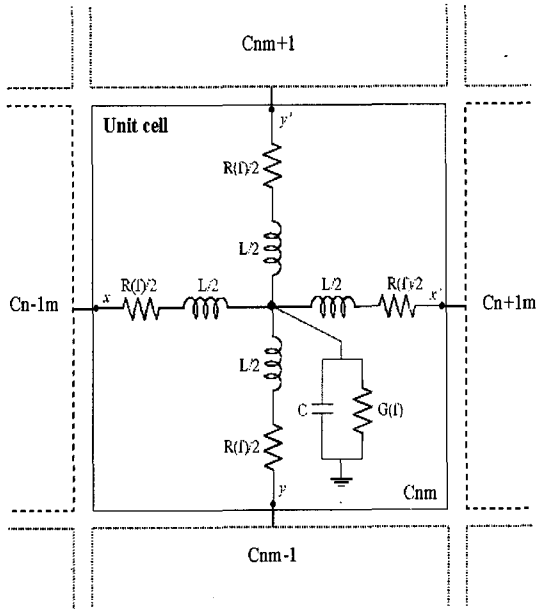
$$G_f = 2\pi f C \tan\delta \tag{9}$$

Here $\delta$ is the loss tangent of the conductor; and its typical value measured is 0.02.




(a) a partial element equivalent circuit(PEEC) model

(a) PEEC 모델




(b) an equivalent circuit of a unit cell

(b) 단위 셀의 등가회로

그림 2. 전원평면의 등가회로 모델: (a) PEEC 모델; (b) 단위 셀의 등가회로

Fig. 2. An equivalent circuit model of power plane: (a) PEEC model; (b) an equivalent circuit of a unit cell.

2. Power Plane Model

A PEEC SPICE simulation circuit model has been constructed to evaluate the power and ground plane performance based on three transmission line models, and the computed results have been compared to measured values. The three models comprise a W-element unit cell model, a frequency independent RLCG model and an frequency dependent RLCG model. The W-element model of HSPICE reflects the loss in transmission lines, demands RLCG parameter values, and construct SPICE nets based on lengths designated by W-elements. RLCG models, on the other hand, employ T-model in their equivalent circuit and take unit cell parameters directly as their inputs. An RLCG T-model has been employed in this study and frequency dependency has been reflected on R(f) and G(f) inputs.

A power plane has been modeled employing 75×20 unit cells, which are interconnected to form a single net for circuit simulation purposes as shown in Figure 2a. At the periphery of a plane, big resistors have been connected for SPICE analysis purposes, which represent resistance between two adjacent planes. An RLCG T-model either of micro-strip or of strip structure is illustrated in Figure 2b. Input and output ports are located at the same places as the measurement probe contact points. Via structures for probing pads are modeled using an RLC $\pi$ modelconnected to the SPICE net. The location and number of capacitors are determined to trace

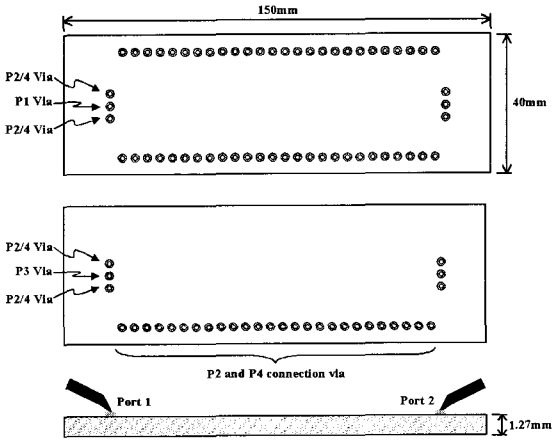



그림 3. 평가 보드 구조

Fig. 3. Evaluation board design for power planes.

impedance characteristics changes of a power plane effectively as all their possible values are tried.

3. Comparison of Simulation and Measurements

Two types of printed circuit boards have been designed and fabricated for evaluation purposes: one for micro-strip and the other for strip structure. Their lateral dimension is 150×40mm and thickness is 1.27mm as shown in Figure 3. A layer assignment of micro-strip structure is shown in Figure 3a, where layers $P_2$ and $P_4$ are ground planes. To observe return current, probing pads and via connections are implemented: some boards carry via holes connected only to $P_2$, and some have via holes connected to both $P_2$ and $P_4$. Figure 3b shows an evaluation board group having strip structure: where the power plane $P_3$ is placed between two ground planes $P_2$ and $P_4$. Internal via connections are used to connect $P_2$ and $P_4$.

Measurement of frequency characteristics of the evaluation boards has been conducted using a vector network analyzer (VNA) HP8720 whose termination impedance is 50Ω. Two-port measurement has been carried out on the frequency range between 50MHz and 3GHz. The central probing pads have via connections connected either to micro-strip or to strip planes and pads at the periphery have via connections connected to ground planes of $P_2/P_4$.

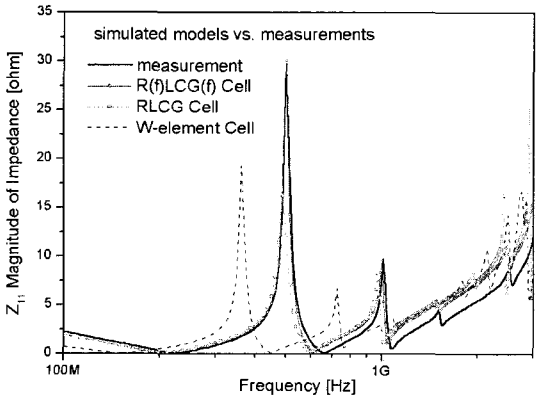
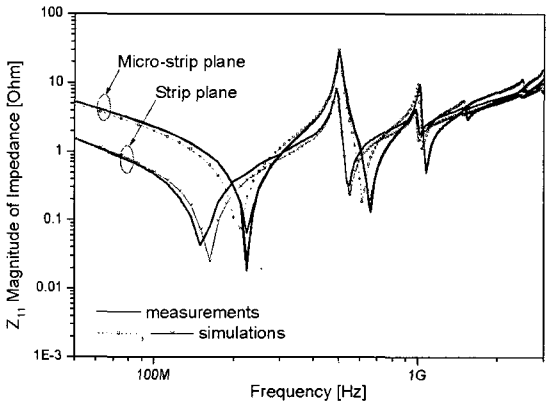
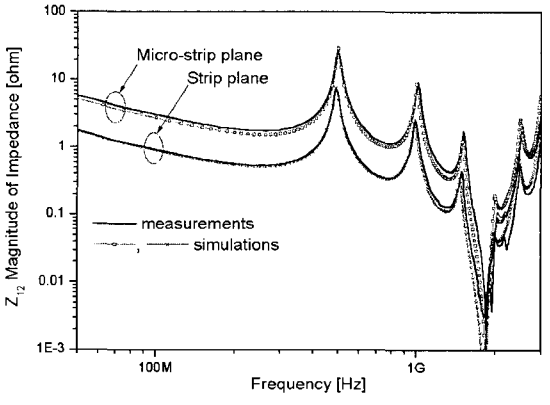



그림 4. 측정 및 해석 결과 비교
Fig. 4. Comparison of simulation results and measurements.

Simulation results are compared to the measurement values from evaluation boards as shown in Figure 4, where three types of unit cell circuits are employed in the PEEC power plane model estimation. The W-element unit cell structure yields frequency characteristics substantially differ from measurements in impedance and resonance frequency in the lower frequency range. The element size of the mesh is believed to make these differences. The frequency independent RLCG circuit yields some differences in magnitude of impedance and resonance frequency, which depends on the frequency characteristics of R and G in high frequency ranges.




(a) self-impedance ($Z_{11}$)




(b) transfer-impedance ($Z_{12}$)

그림 5. 마이크로 스트립과 스트립 평면 특성 비교:
(a) self-impedance ($Z_{11}$)
(b) transfer- impedance($Z_{12}$).

Fig. 5. Comparison of micro-strip and strip plane performance: (a) self-impedance ($Z_{11}$); (b) transfer-impedance($Z_{12}$).

The frequency dependent RLCG circuit, denoted R(f)LCG(f) in Figure 4, yields the most realistic results both in impedance and resonance. Minor differences between measurements and simulation results reflect some inaccurate estimation of current crowding due to skin effect in higher frequency range. Further discussions in this paper are based the frequency dependent RLCG model for PEEC SPICE nets focusing on impedance analysis.

## Ⅲ. De-Coupling Capacitors of DRAM Modules

Introduction of de-coupling capacitors changes frequency characteristics of PDN substantially. Optimal size and position of de-coupling capacitors yield stable PDN designs.

### 3. Impedance and De-coupling Capacitors

Layer assignment of power and ground planes determines impedance characteristics. Figures 5a and 5b show the simulation and measurement results both for micro-strip and strip structures. Both self-impedance [$Z_{11}$] and transfer-impedance [$Z_{12}$] are compared. The layer $P_1$ of micro-strip structure shown in Figure 1b is the $V_{DD}$ plane, and $P_2$ and P4 are ground planes. $P_3$ is for $V_{REF}$, which yields a strip structure with the adjacent ground planes of $P_2$ and $P_4$.

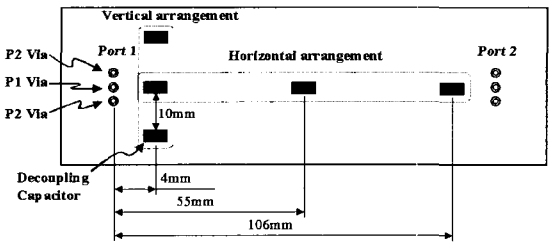
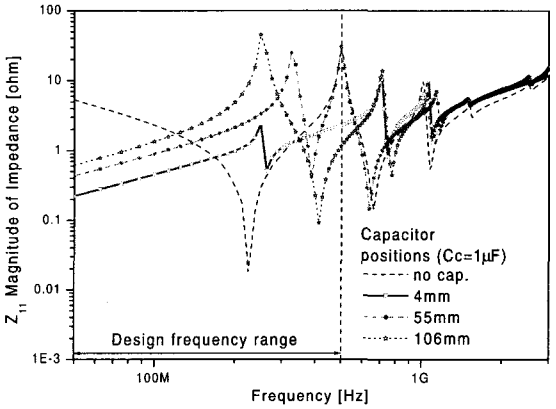
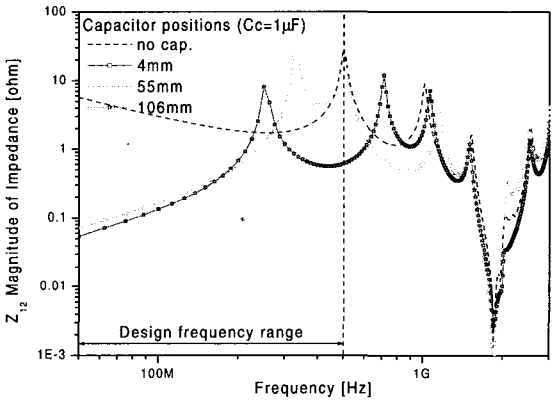



그림 6. 평가 보드에서 커패시터 위치
Fig. 6. Capacitor locations in an evaluation board.

It has found that the strip structure yields lower impedance than a micro-strip counter part both in the operating range and in peak values. The strip structure is better for the sensitive voltage level of $V_{REF}$. More accurate results have been obtained for transfer-impedance [$Z_{12}$] than self-impedance [$Z_{11}$] due to lower dependency on unit cells. Self-impedance [$Z_{11}$] reflects some influence from evanescent wave mode, whereas transfer-impedance [$Z_{12}$] is relatively free from this mode. It has been also found that the number of via connections and their location do not give significant differences both in measurement and simulation results.




(a) self-impedance ($Z_{11}$)




(b) transfer-impedance ($Z_{12}$)

그림 7. 커패시터 위치에 따른 임피던스 특성:
(a) self-impedance ($Z_{11}$)
(b) transfer-impedance ($Z_{12}$)

Fig. 7. Impedance characteristics due to capacitor positions: (a) self-impedance ($Z_{11}$); (b) transfer-impedance ($Z_{12}$).

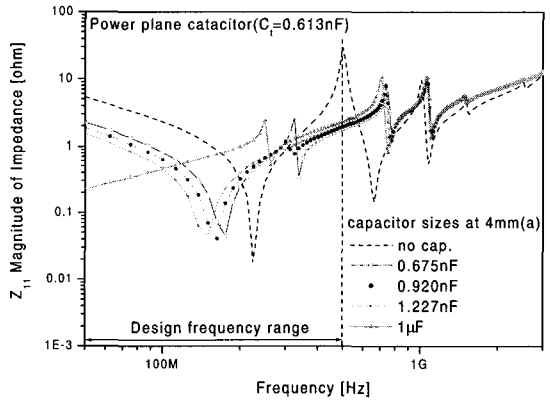
The location of de-coupling capacitor makes significant differences in power plane impedance. To

estimate these differences in self-impedance [$Z_{11}$] and transfer-impedance [$Z_{12}$], several capacitor locations are studied as shown in Figure 6. The distances from probing port 1 to the capacitors are 4mm, 55mm and 106mm in horizontal capacitor arrangements; and vertical assignments allows 10mm separation. This separation reflects the physical dimension of DRAM chips implemented on a module and the minimum distance between them.

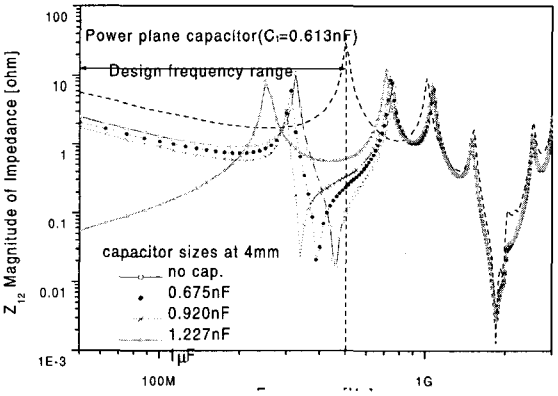
Figure 7 shows some simulation results with respect to the three locations of de-coupling capacitors. It is found that the location of de-coupling capacitors makes significant differences in self-impedance [$Z_{11}$] and transfer-impedance [$Z_{12}$] when the sizes of the capacitors are the same. De-coupling capacitors are to be placed as close to power/ground pins of DRAM chips as possible. Figure 7a self-impedance [$Z_{11}$] can be lowered substantially by placing capacitors closer to current sources. Figure 7b shows transfer-impedance [$Z_{12}$], where a symmetric capacitor configuration yields the same capacitance.

We now turn to the size problem of de-coupling capacitors. Four different capacitance values are studied based on the inherent capacitance of printed circuit board (Ct=0.613nF): 110% of Ct (0.675nF), 150% (0.920nF), 200% (1.227nF) and 1uF. These capacitors are placed at vertical locations separated 10mm as show in Figure 6. Figure 8a shows that larger capacitors are helpful in lowering power plane impedance unless the power and ground planes experience resonance. Transfer-impedance [$Z_{12}$] shown in Figure 8b indicates that a larger capacitor may bring in an unwanted impedance hike in some frequency ranges, and thereby bigger noise in PDN. Here impedance increases 250MHz with 1uF capacitance whereas cases with lower capacitance of 110-200% of Ct yield the lowest value at 300MHz. Vertical deployments of capacitors yield better performance than horizontal counterparts.

Figure 9a shows self-impedance [$Z_{11}$], where capacitors in vertical locations near the current source affect input impedance. These capacitors yield resistive loads up to a resonance frequency. These characteristics allow PDN to become a low pass filter. Transfer-impedance [$Z_{12}$] of Figure 9b is relatively lower for horizontal deployments up to 500MHz; cases with vertical deployments experience resonance at lower frequency regions. It seems that the optimization can be successfully accomplished considering both self-impedance [$Z_{11}$] and transfer-impedance [$Z_{12}$]. It is desirable to place de-coupling capacitors between a current source and DRAM chips. In DRAM modules having a limited PCB space, self-impedance [$Z_{11}$] and transfer-impedance [$Z_{12}$] can be improved by placing de-coupling




(a) self-impedance ($Z_{11}$)

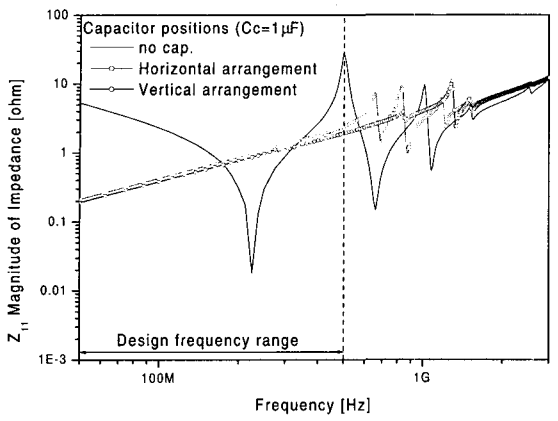



(b) transfer-impedance ($Z_{12}$)

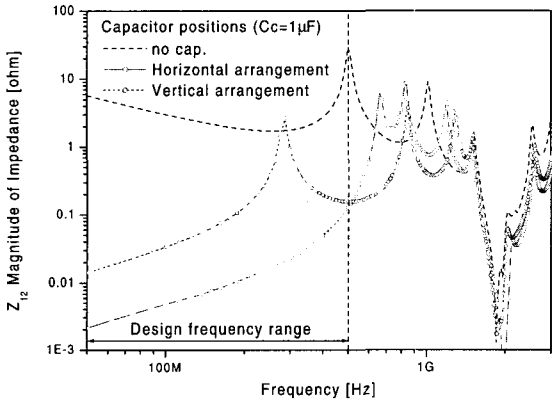
그림 8. 커피시터 용량에 따른 임피던스 특성
(a) self-impedance ($Z_{11}$)
(b) transfer- impedance ($Z_{12}$)

Fig. 8. Impedance characteristics due to capacitance values: (a) self-impedance ($Z_{11}$); (b) transfer-impedance ($Z_{12}$).

capacitors in vertical positions close to DRAM chips.




(a) self-impedance ($Z_{11}$)




(b) transfer-impedance ($Z_{12}$)

그림 9. 커패시터 위치에 따른 임피던스 특성
(a) self-impedance.
(b) transfer-impedance ($Z_{12}$)

Fig. 9. Impedance characteristics due to capacitor positions: (a) self-impedance. (b) transfer-impedance ($Z_{12}$).

2. Simple Impedance Calculation

Some design parameters should be considered in designing PDN for digital circuits such as layer assignment, thickness copper layer, thickness of dielectrics, types of capacitors. Due to excessive computation time of PEEC model simulation, a simple circuit model is preferred to figure out the approximate values of each parameter configuration, and thereby to reduce computation time. It is to find viable de-coupling capacitor size and location in DRAM module PDN based on the discussion and observation in the previous sections.

In deriving the simple equation a lumped model is employed to represent PDN capacitor size and locations. This equation may yield a viable capacitance value via rough estimation of the impedance value; a further precise estimation should follow with PEEC model taking the capacitor values. The equivalent impedance between ports and capacitors are represented as follows:

$$Z_P = R_{eff} + j\omega L_{eff} + \frac{1}{j\omega C_{DE-C}} \tag{10}$$

Here, $R_{eff}$ is the sum of ESR of the capacitors and $R_{PCB}$ of PCB, and $L_{eff}$ is the sum of ESL of capacitor leads and $L_{PCB}$, respectively. $C_{DE-C}$ is de-coupling capacitance and $\omega = 2\pi f$.

Resistance and inductance between ports and capacitor locations, the capacitor locations are connected to ground. SPICE simulation yields real and imaginary parts of impedance as follows:

$$Z_{PCB} = R_{PCB} + j\omega L_{PCB} \tag{11}$$

$$L_{PCB} = \frac{Z_{PCB}(Imaginary\ part)}{2\pi f} \tag{12}$$

Effective resistance and inductance of PCB, $R_{PCB}$ and $L_{PCB}$, are obtained from a lumped mode with a de-coupling capacitor, and equivalent impedance of Equation (10) can be written as follows.

$$Z_P = R_{ESL} + R_{PCB} + j\omega(L_{ESL} + L_{PCB}) + \frac{1}{j\omega C_{DE_c}} \tag{13}$$

The magnitude of impedance of a power plane is as follows:

$$|Z_P| = \sqrt{R^2 + \frac{(\omega^2 LC - 1)^2}{\omega^2 C^2}} \tag{14}$$

The above equation is the main formula simplifying the calculation of impedance without simulation of PDN planes. The resultant PDN impedance values from different capacitance and inductance are compared to a target value determined by the following equation [5]:

$$Z_{target} = \frac{(V)supply) \times (5\%, ripple)}{current} \quad (15)$$

Only the ones lower than the target value can be used to select de-coupling capacitor of a PDN. As an example, the target impedance can be estimated with the following values: a case with supply voltage of 3.3volts and current of 0.152A yields 1.09ohm.

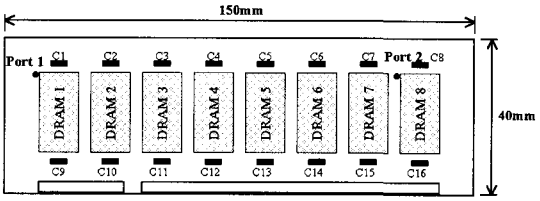



그림 10. DRAM 칩과 커피시터 위치
Fig. 10. Layout of DRAM chips and de-coupling capacitors.

3. De-coupling Capacitance of DRAM Modules

We now turn to the problem finding de-coupling capacitance yielding impedance lower than the target impedance. To keep the impedance under the target value, capacitance should be carefully evaluated. Larger capacitance may suffer higher ESR and ESL, and thereby the high frequency characteristics may degrade sharply. For the high frequency region, multiple capacitors are used to overcome the ESR and ESL problem of a single capacitor.

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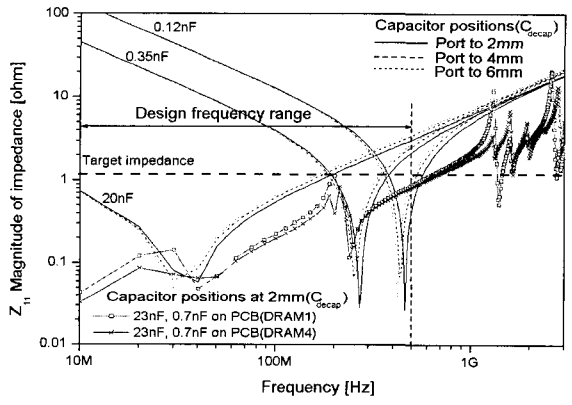
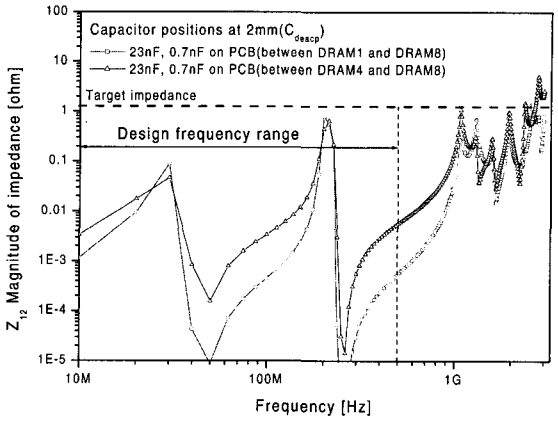



(a) self-impedance ($Z_{11}$)




(b) transfer-impedance ($Z_{12}$)

그림 11. DRAM 모듈에서 임피던스 특성 :
(a) self-impedance ($Z_{11}$)
(b) transfer- impedance ($Z_{12}$)

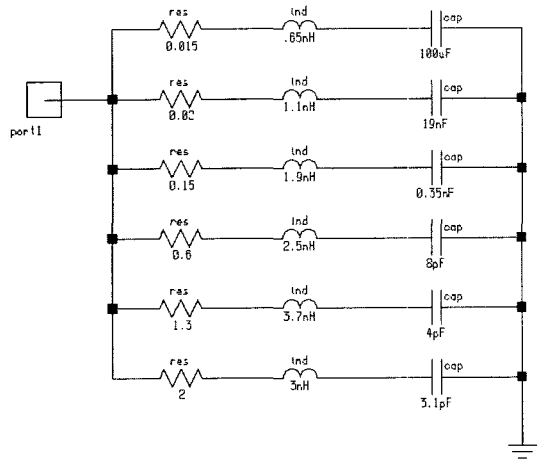
Fig. 11. Impedance characteristics in a DRAM module: (a) self-impedance ($Z_{11}$); (b) transfer-impedance ($Z_{12}$)

The search of appropriate de-coupling capacitance values can be pursued in two ways: through an algebraic optimization based on precise model equations reflecting characteristic impedance of power planes; and through a series of exhaustive search via computer simulation. The algebraic approach, however, is impractical due to the difficulties in derivation of comprehensive equations yielding PDN impedance. Parameters depend on too many variables such as thickness of layers, parasitic element values related capacitors employed, PCB size, and etc.

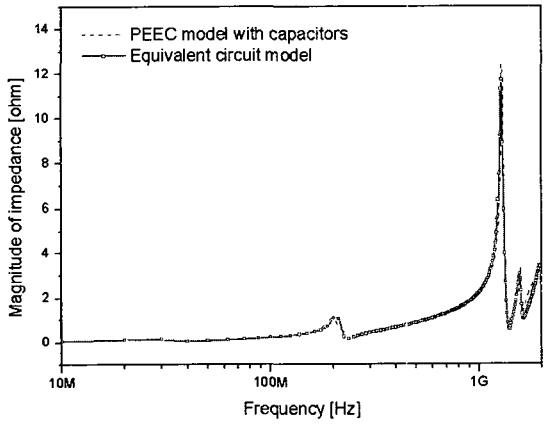
The approach employed here is basically through the computer simulation employing a simple equation yielding rough estimations, where parameter spaces of distance and capacitance are systematically spanned. Figure 10 shows a DRAM module accommodating 8 chips on a micro-strip power plane. Since the module is inserted into its motherboard during normal operation, an equivalent capacitance of 100uF is introduced at the lower part of a PDN SPICE net. De-coupling capacitors are implemented at the top and bottom sides of each DRAM chip.

Self-impedance [$Z_{11}$] of DRAM 1 and DRAM 4 is shown in Figure 11a: two groups of curves represent

cases with one de-coupling capacitor and a case with two capacitors. It shows cases with single capacitor yield lower self-impedance at the low frequency range but higher impedance at the high frequency region. To control this high impedance an additional capacitor has been introduced. Figure 11b shows transfer impedance of the case with two capacitors yield impedance lower than the target value.




(a) equivalent circuit of power plane




(b) comparison of impedance by the PEEC model and the equivalent circuit

그림 12. PEEC 모델과 등가회로의 임피던스 비교

Fig. 12. Comparison of impedance of equivalent circuit and PEEC model: (a) equivalent circuits of power plane; (b) comparison of impedance by the PEEC model and equivalent circuit.

The design space scanning results are verified through comparison to the computation outputs using the PEEC model. Figure 12 shows the comparison of the two computations: one from the simple equation employing lumped parameters and the other from the simulation using the PEEC based on distributed circuit structure. Even though the differences are negligible in most cases, it is necessary to confirm the impedance level: the level should be lower than the target in the design operating frequency range

Figure 13 shows a time-domain response of PDN noise. Modules with de-coupling capacitors suffer lower noise: 3 orders of magnitude smaller than the one without capacitors. This estimation is based on the following operating conditions: the input current source of PDN is DRAM 1, which generates a current stream of five pulses, each magnitude of 1A, rise time 0.1nsec, pulse width 0.9nsec and period of 2nsec. The victim device is DRAM 8 suffering power/ground plane fluctuation. The case with de-coupling capacitors suffers far smaller disturbances than the one without capacitors. It is mainly due to de-coupling capacitors resulting in lower transfer-impedance.

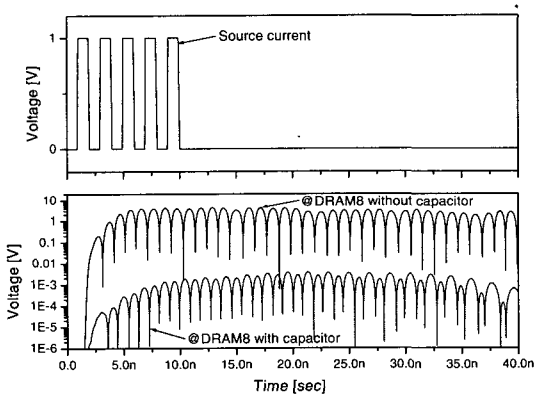



그림 13. DRAM 모듈 시간 응답

Fig. 13. Transient PDN behavior of a DRAM module.

## Ⅳ. Conclusion

Presented is a systematic design approach for power distribution network aiming at applications to

DRAM module designs. Three main stages are comprised in this design approach: PDN modeling and simulation based on partial element equivalent circuit; verification of the simulation results; and design space scanning for viable capacitance values. Power and ground planes have been modeled and simulated using frequency-dependent RLCG circuit structure, and the computed outputs are compared to the measured values. Behavior of the model has turned out to be fairly close to the actual measurements, which becomes the basis of further studies on power and ground plane performance.

Impedance characteristics with a de-coupling capacitor are analyzed to devise an effective way to stabilize power and ground plane performance within a target level of disturbances. Self-impedance [$Z_{11}$] and transfer-impedance [$Z_{12}$] are examined in terms of distance between circuit features and the size of de-coupling capacitors. A simple equation has been derived to find the de-coupling capacitance values yielding impedance lower than design target, and thereby reducing the overall computation time. Since the equation is based on lumped model, it is necessary to use the rigorous PEEC model to get more precise values.

The effectiveness of the design methodology has been demonstrated using a DRAM module with discrete de-coupling capacitors and a strip structure. The target operating frequency of 500MHz has been successfully pursued with two de-coupling capacitors of 23nF and 0.7nF, which are mounted in parallel. During the time consuming search processes utilize the simple equation based on a model, and thereby reducing the computation time. The simple equation is repeatedly used to evaluate the PDN structure without significant design time overhead. After the search, precise results are obtained through some simulation runs based on the PEEC model. The overall computation time can be saved significantly.

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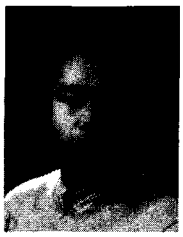
## 저 자 소 개



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