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# High-Frequency Forward Transformer Linked PWM DC-DC Power Converter with Zero Voltage Switching and Zero Current Switching Bridge Legs

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## ABSTRACT

A novel zero-voltage and zero-current switching PWM DC-DC converter with lowered conduction losses is presented in this paper. A new double two-switch forward high frequency transformer type soft-switching converter topology is developed to minimize circulating currents occurs during freewheeling period. This converter has advantages as less number of the components, simple control principle under constant operation frequency, free of transformer imbalance effect. The principle of operation is illustrated with steady-state analysis. Moreover, the effectiveness of the proposed converter topology is verified by implementation of a 500W-100kHz breadboard using IGBTs.

**Keywords:** Double two-switch forward PWM circuit topology, High frequency transformer link, ZVZCS soft switching, Idle and circulating currents, Tapped induct type smoothing filter

## 1. Introduction

A variety of high performance transformer linked DC-DC power converter topologies have been proposed for increasing power density and efficiency. In high power applications, soft-switching phase-shifted PWM (PS-PWM) full-bridge converters have much attention because of their low switching losses, constant frequency operation and simple control[1]-[4]. In most of PS-PWM full-bridge converters, however, a large circulating current flows through the transformer and primary side circuit during a freewheeling interval[5]. Fig. 1 shows the conventional ZVS PS-PWM full-bridge converter.

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High frequency transformer voltage and current waveforms of this converter are illustrated in Fig. 2. During freewheeling period caused by varying duty cycle as phase-shift PWM control strategy, a circulating current flows through power semiconductor devices and high frequency transformer. Due to the circulating current, conduction losses of the switching devices and transformer are still high compared with those of hard-switching PWM converters. In recent years, several soft-switching PS-PWM full-bridge converters, which can reduce the circulating current, have been developed[5]-[9].

The converter presented in the reference [6] employs saturable reactors and a tapped inductor as an output low-pass filter. The tapped inductor acts as a passive clamp element, so that the rectified output voltage is clamped in positive polarity during the freewheeling interval.

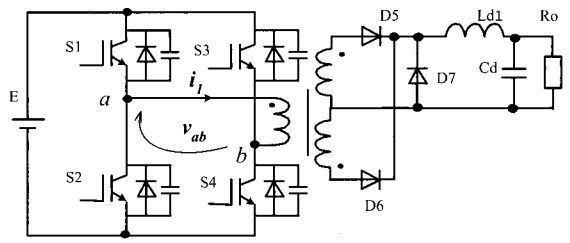


Fig. 1. A conventional full-bridge ZVS phase-shifted PWM converter.

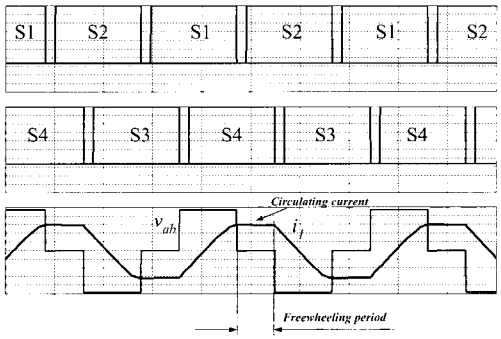


Fig. 2. Voltage and current waveforms of the conventional ZVS converter.

Therefore, the rectifier diodes are biased in reverse, and the output inductor current flows through the secondary freewheeling diode during the freewheeling interval. As a result, the circulating current through the transformer and primary side circuit becomes zero. The saturable reactors however need highly square B-H magnetization curve, what causes cost increasing. The converter presented in the reference [7] makes use of an active clamp circuit in the secondary side circuit to clamp the rectified output voltage in positive polarity during the freewheeling interval. Therefore, the circulating current can be reduced during the freewheeling interval. The converter needs the active switch and its drive circuit, however, what makes circuit complex. In addition, a high peak current corresponding to output current flows through the auxiliary active switch, which operates under hard-switching. The converter presented in the reference [8] uses an auxiliary winding of the transformer, auxiliary rectifier diodes, and output capacitor (hold capacitor) to keep the rectified output voltage in positive polarity in the freewheeling interval. There is no additional active switch, but the passive auxiliary circuit is sufficiently complex. The converter presented in [9] employs auxiliary diodes and capacitors in the secondary side circuit as an energy-recovery snubber. The auxiliary capacitors are charged up through the rectifier during the powering interval, and keep the rectified output voltage in positive polarity in the freewheeling interval. Although the auxiliary circuit is comparatively simple, there is another problem, namely, high voltage stresses appear across the rectifier diodes and the auxiliary circuit. Converters topologies operate under ZVS for leading leg, and ZCS for lagging leg have been presented[7]-[9]. Due to ZCS operation, the parasitic inductance in primary DC bus causes a high voltage overshoot or current ringing on the switches when each switch in the lagging leg is turned on because the parasitic capacitance of the switch charges through the parasitic inductance and DC voltage source. Therefore, there is need to minimize parasitic inductance in the DC bus.

Taking into account all mentioned above disadvantage of the early-presented high frequency transformer linked converter topologies in this paper new double (interleaved) two-switch forward PWM DC-DC converter is presented. As well as full-bridge converter topology, interleaved two-switch forward converter topology has been often used for high power applications[10][11]. The two forward circuits operate 180 degrees out of phase each other. As well known, the peak voltage stress on each switch is clamped to DC voltage source $E_0$ and current stresses are also comparable to those of full-bridge converter. Forward configuration has a disadvantage such that the flux swing of the transformer operates in one direction, so that the transformer core size is to be enlarged as compared with that of full-bridge configuration. In high frequency operation however thermal stress due to power losses of the magnetic core limits the operating flux swing, therefore the disadvantage is eliminated. Moreover, there is no need to use any flux balancing methods such as blocking capacitor in case of the full-bridge configuration.

This paper proposes a new interleaved two-switch forward converter topology operating under ZVS and ZCS with minimized idling and circulating current with no additional auxiliary circuits. The operation principle is illustrated together with steady-state circuit analysis.

Moreover, a 500W, 100kHz prototype is implemented to verify effectiveness of the proposed converter.

## 2. Principle of Operation

Fig. 3 shows a basic circuit of the proposed converter. One of the forward conversion stages consists of switches $S_1$, $S_4$, transformer $T_2$, diodes $D_2$, $D_4$, and rectifier diode $D_6$. The other one consists of switches $S_2$, $S_3$, transformer $T_1$, diodes $D_1$, $D_3$, and rectifier diode $D_5$. $L_{S1}$ and $L_{S2}$ are small leakage inductance of $T_1$ and $T_2$, respectively. In addition, a tapped inductor is used as output low-pass filter. In order to prevent parasitic ringing and negative undershoots across $S_3$ and $S_4$, caused by parasitic capacitance of $S_3$ and $S_4$, antiparallel diodes $D_8$ and $D_9$ are used.

Fig. 4 illustrates switching sequences and theoretical waveforms of the converter in continuous conduction mode. Switch $S_4$ ($S_3$) is turned off after $S_1$ ($S_2$) is turned off with a short delay time $t_6$. Moreover, $S_1$ and $S_2$ are driven complementary with a short blanking interval $t_d$. The output voltage can be regulated by varying a controllable interval $t_\alpha$ as PWM with a constant switching frequency.

Fig. 5 shows the topological equivalent circuits for a half-cycle of operation in continuous conduction mode. The principle of operation in steady-state condition is described with the following assumptions.

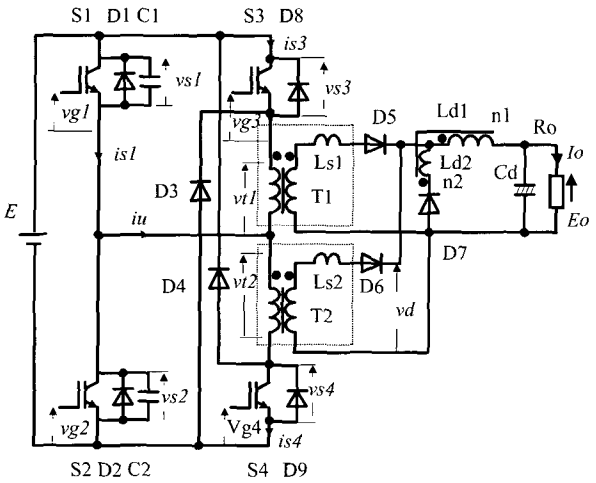


Fig. 3. Basic circuit of the proposed soft-switching DC-DC converter.

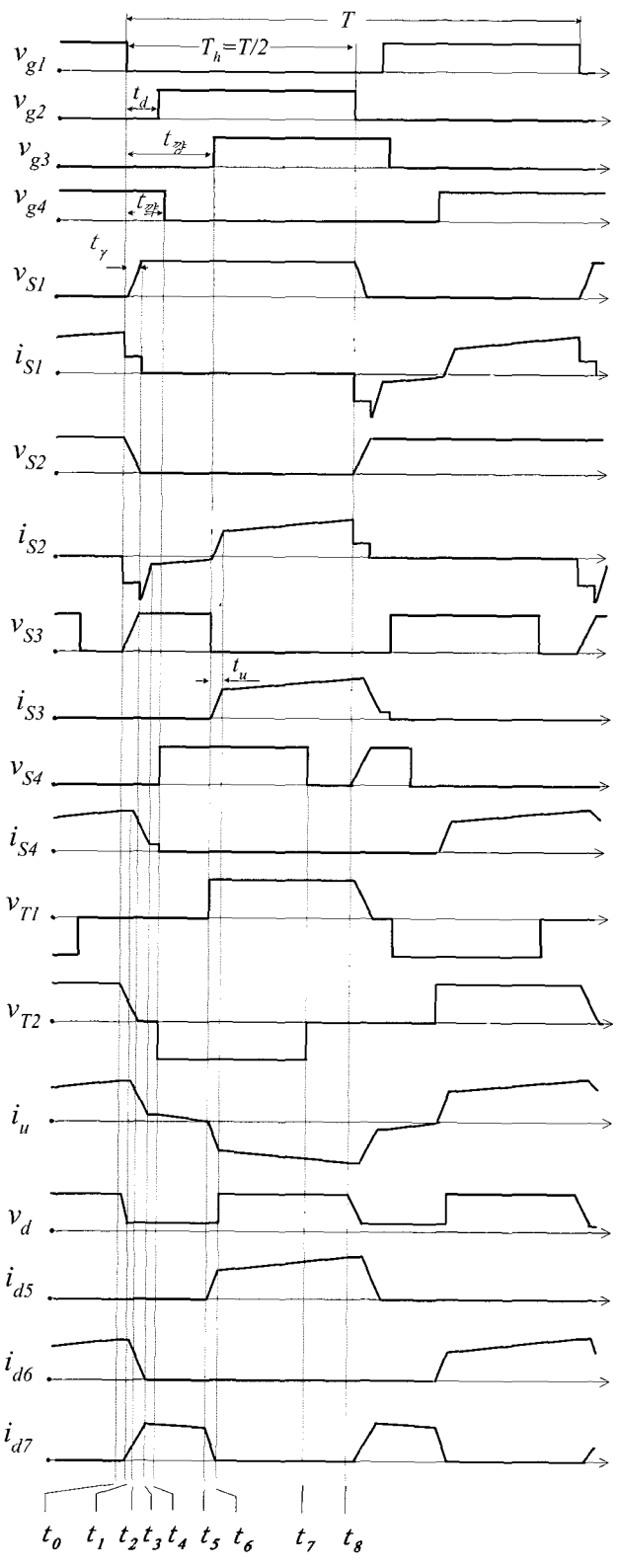


Fig. 4. Theoretical waveforms of the proposed converter in continuous conduction mode.

- All the switches and components are ideal.
- Transformers $T_1$ and $T_2$ are identical, so that each magnetizing inductance and leakage inductance are represented as $L_{p1}$ =$L_{p2}$ =$L_p$, $L_{S1}$ =$L_{S2}$ =$L_S$ respectively.
- Capacitors $C_1$ and $C_2$ are identical, $C_1$ =$C_2$ =C.
- Inductance $L_{d1}$ and $L_{d2}$ are tightly coupled with each other and its coupling coefficient k =1.

Before time $t_0$, switches $S_1$, $S_4$ and rectifier diode $D_6$ are conducting.

**(a) Interval 1($t_0$, t1):** At time $t_0$, $S_1$ is turned off under ZVS by the aid of lossless snubber capacitors $C_1$ and $C_2$. Since inductance $L_p$ and $L_{d1}$ are large, magnetizing current ip2 and rectifier current $i_{d6}$ are assumed to be a constant during this interval. Capacitor voltage $v_{c1}$, increases as

$$v_{C1} = \frac{i_{p2}(t_0) + \{i_{d6}(t_0)/N_T\}}{2C}(t - t_0) \tag{1}$$

where, $N_T$, ($N_T$=$N_p$/$N_S$ ) is the turns ratio of the transformer. Then, rectified voltage $v_d$ decreases as

$$v_d = (E - v_{C1})/N_T \tag{2}$$

Freewheeling diode $D_7$ starts to conduct when $v_d$ reaches $N_L E_0$, where $N_L$ is the turns ratio of the tapped inductor defined as $N_L$=$n_2$/($n_1$+$n_2$); $n_1$, $n_2$ are the number of turns of $L_{.d1}$ and $L_{d2}$ respectively. At the end of this interval, $i_{p2}$, $i_{d6}$ and $v_{c1}$ are given by

$$\begin{aligned} i_{p2}(t_1) &= i_{p2}(t_0) \\ i_{d6}(t_1) &= i_{d6}(t_0) \\ v_{C1}(t_1) &= E - N_T N_L E_0 \end{aligned} \tag{3}$$

**(b) Interval 2($t_1$, $t_2$):** The output current starts flow through $D_7$, $L_{d2}$ and $L_{d1}$. Therefore, the output current reflected to primary side decreases. $v_{c1}$ and $i_{d6}$ are estimated by

$$\begin{aligned} 2C\frac{dv_{C1}}{dt} &= \frac{1}{N_T} i_{d6} + i_{p2}(t_1) \\ L_S\frac{di_{d6}}{dt} &= \frac{1}{N_T}(E - v_{C1}) - N_L E_0 \end{aligned} \tag{4}$$

Capacitor voltage $v_{c1}$ and rectifier current $i_{d6}$ are derived from (4) under the second-order approximation as

$$v_{C1} \approx v_{C1}(t_1) + \frac{i_{p2}(t_1) + \{i_{d6}(t_1)/N_T\}}{2C}(t - t_1) \tag{5}$$

$$i_{d6} \approx i_{d6}(t_1) + \frac{N_T i_{p2}(t_1) + i_{d6}(t_1)}{4N_T^2 L_S C}(t - t_1)^2 \tag{6}$$

This interval ends either when voltage $v_{c1}$ rises to E, after what $D_2$ starts to conduct (this stage is defined as mode A), or when $i_{d6}$ reaches zero and $D_6$ turns off (this stage is defined as mode B), whichever occurs first. In most cases, since capacitance C is small, $v_{c1}$ reaches E before id6 becomes zero. The boundary condition for this mode (mode A) can be given from (5) and (6) as

$$C(N_T N_L E_0)^2 < L_S i_{d6}(t_1)\{N_T i_{p2}(t_1) + i_{d6}(t_1)\} \tag{7}$$

**(c) Interval 3($t_2$, $t_3$):** For the case of mode A, as shown in Fig.5, diode $D_2$ Starts $t_0$ conduct and $i_{d6}$ continues to decrease as

$$i_{d6} = i_{d6}(t_2) - \frac{N_L E_0}{L_S}(t - t_2) \tag{8}$$

This interval ends when $i_{d6}$ reaches zero.

For mode B (this equivalent circuit is not indicated in Fig. 5), rectifier $D_6$ is turned off first. The capacitor voltage $v_{c1}$ increases as

$$v_{C1} = v_{C1}(t_2) - \frac{i_{p2}(t_2)}{2C}(t - t_2) \tag{9}$$

This interval ends when $v_{c1}$ becomes E.

**(d) Interval 4($t_3$, $t_4$):** Whole output current flows through $D_7$, $L_2$ and $L_{d1}$. The output current reflected to the primary side becomes zero. Only a small magnetizing current of the transformer $T_2$ circulates through $S_4$ and $D_2$. This interval ends when switch $S_4$ is turned off and $i_{p2}$ is

$$i_{p2}(t_4) \approx i_{p2}(t_0) \tag{10}$$

**(e) Interval 5($t_4$, $t_5$):** At time $t_5$, switch $S_4$ is turned off with ZCS. Magnetizing current $i_{p2}$ flows through $D_2$ and $D_4$ to DC voltage source E as a reset action of transformer $T_2$. Then $i_{p2}$ decreases as

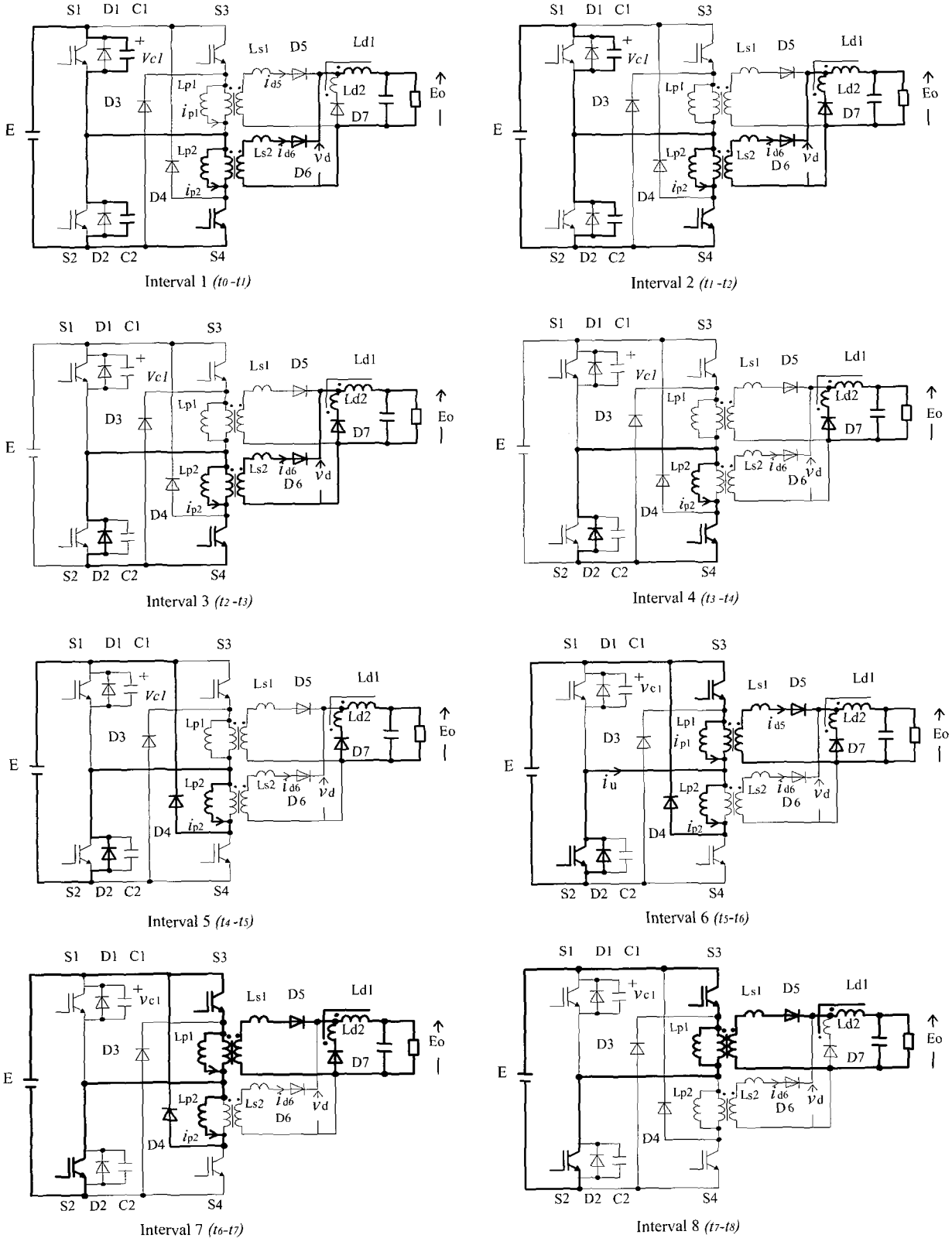


Fig. 5. Equivalent circuits in a half cycle of operation.

$$i_{p2} = i_{p2}(t_4) - \frac{E}{L_p}(t - t_4) \tag{11}$$

**(f) Interval 6($t_5$, $t_6$):** At time $t_5$, depending on duty ratio of the converter, $S_3$ is turned on under ZCS because leakage inductance $L_{S1}$ softens $di_{S3}/dt$ at turn-on of $S_3$. Switch $S_2$ is also turned on with ZVS and ZCS when current $i_u$ becomes $i_u < 0$. The output current reflected to primary side of the transformer flows through $S_2$ and $S_3$. Magnetizing current $i_{p1}$ and rectifier current $i_{d5}$ begins flowing through $S_2$ and $S_3$, and $D_5$, respectively. They are given by

$$i_{p1} = \frac{E}{L_p}(t - t_5) \tag{12}$$

$$i_{d5} = \frac{E - N_T N_L E_0}{N_T L_S}(t - t_5) \tag{13}$$

On the other hand, current $i_{L2}$ through $L_2$ decreases. This interval ends when $i_{L2}$ reaches zero.

**(g) Interval 7($t_6$, $t_7$):** Diode $D_7$ turns off. Whole output current mows through $D_5$ and $L_1$. Magnetizing current $i_{p2}$ continues to decrease with a constant slope - $E/L_p$.

**(h) Interval 8($t_7$, $t_8$):** When the magnetizing current $i_{p2}$ becomes zero ($t=t_7$), diode $D_4$ turns off. The energy is being delivered through $S_3$, $S_2$, $T_1$, and $D_5$. The half cycle of operation ends at time $t_8$.

The operation of the next half-cycle is symmetrical with mentioned above half-cycle. As described above $S_1$ and $S_2$ are turned on and turned off with ZVS, while $S_3$ and $S_4$ operate with ZCS at turn-on and turn-off. The idling and circulating currents in both primary and secondary side are substantially low with no additional auxiliary circuits.

## 3. Steady-State Characteristics

The current stress on the switches and the output voltage in continuous conduction mode are analytically evaluated in this section. Fig. 6 shows relevant waveforms of rectifier voltage $v_d$ and inductor current $i_{L1}$.

Peak current stress $I_{sp}$ for $S_1$-$S_4$ are given by

$$i_{sp} = i_{p2}(t_1) + \frac{i_{d6}(t_1)}{N_T} \tag{14}$$

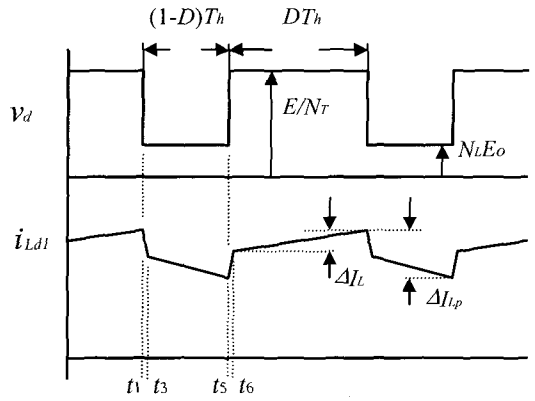


Fig. 6. Relevant waveforms of rectified voltage $v_d$ and inductor current $i_{Ld1}$.

And $i_{p2}(t_1)$ is obtained as

$$i_{p2}(t_1) = \frac{DET_h}{L_S} \tag{15}$$

where, $T_h$ ($T_h = T / 2$) is the half-switching interval of the converter, and D is the duty ratio of the converter represented by $D=(T_h - t_\alpha)/T_h$ (see Fig. 4). Due to delay time $t_\delta$, the maximum duty ratio is limited by

$$D_{\max} = \frac{T_h - t_\delta}{T_h} \tag{16}$$

Current $i_{d6}(t_1)$ is derived as follows. Since inductance $L_S$ is substantially low, current commutation intervals, from $t_1$ to $t_3$ and from $t_5$ to $t_6$, are negligible small. Therefore, current $i_{L1}$ through $L_{d1}$ can be represented as

$$\begin{aligned} n_1 i_{L1}(t_1) &= (n_1 + n_2) i_{L1}(t_3) \\ (n_1 + n_2) i_{L1}(t_5) &= n_1 i_{L1}(t_6) \end{aligned} \tag{17}$$

Then $i_{d6}(t_1)$ and peak to peak current ripple $\Delta I_{LP}$ of $L_{d1}$, shown in Fig. 6, are derived as

$$i_{d6}(t_1) = i_{L1}(t_1) = \frac{I_0}{1 - (1 - D)N_L} + \frac{\Delta I_L}{2} \tag{18}$$

$$\Delta I_{Lp} = \frac{N_L I_0}{1 - (1 - D)N_L} + (1 - \frac{N_L}{2})\Delta I_L \tag{19}$$

where, Io is the output current expressed by

$$I_0 = \frac{1}{T_h}\int_0^{Th} i_{L1}(t)dt, \tag{20}$$

and $$\Delta I_L = \frac{(1-D)(1-N_L)E_0T_h}{L_{d1}} \tag{21}$$

Therefore, $I_{sp}$ is given by

$$I_{sp} = \frac{DET_h}{L_p} + \frac{I_0}{N_T\{1-(1-D)N_L\}} + \frac{\Delta I_L}{2N_L} \tag{22}$$

The output voltage is derived as follows.
During a half cycle period, rectified voltage $v_d$ is expressed as

$$\begin{aligned} v_d &= N_L E_0 \quad for \quad t_1 < t \le t_6 \\ v_d &= \frac{E}{N_T} \quad for \quad t_6 < t \le t_8 \end{aligned} \tag{23}$$

From (23), output voltage $E_0$ is estimated by

$$E_0 = \frac{1}{T_h}\int_0^{Th} v_d(t)dt = \frac{DE}{N_T\{1-(1-D)N_L\}} + \frac{L_S I_0 DE}{T_h\{1-(1-D)N_L\}^2} \tag{24}$$

When $L_s$ is small enough, $E_0$ is given as

$$E_0 \cong \frac{DE}{N_T\{1-(1-D)N_L\}} \tag{25}$$

As can be seen from (22) and (24), when turns ratio $N_L$ is small as $N_L << 1$, both current stress $I_{Sp}$ and output voltage characteristic are close to those of conventional hard switching interleaved two switch forward converters.

## 4. Experimental Results

To verify the operating principle and steady state characteristics, the experiments were carried out with a 500W($E_0$ = 50V, $I_0$ = 10A) 100kHz breadboard using IGBTs. The circuit parameters are presented in Table1.

The magnetizing inductance and leakage inductance of the transformer were utilized for $L_{p1}$, $L_{p2}$ and $L_{S1}$, $L_{S2}$, respectively. Delay time $t_\delta$ limits maximum duty ratio as mentioned in (16).

Table 1. Design specifications of the converter.

| | | |
|---|---|---|
| IGBT | $S_1$-$S_4$ | IRG4PC40W, $V_{ces}$ =600V, $I_c$ =20A ($T_c$ =100°C), Coes =140pF (at $V_{cc}$ =30V) |
| Diode | $D_1$-$D_4$ | SF8L60, $V_{PRM}$ =600V, $I_F$ =8A |
| Rectifier Diode | $D_5$-$D_7$ | ESAC93M-03, $V_{PRM}$ =300V, $I_F$ =12A |
| Antiparallel diode | $D_8$-$D_9$ | SF8L60, $V_{RRM}$ =600V, $I_F$ =8A |
| Lossless snubber capacitor | $C_1$, C2 | 820Pf (Including $C_{oes}$, of $S_1$, S2) |
| High Frequency Transformer | $T_1$, T2 | $N_p$ =23Turns $N_s$ =7Turns $N_T$ =3.3 |
| Magnetizing inductance of the transformer | $L_{p1}$, $L_{p2}$ | 2.5mH |
| Leakage inductance (referred to secondary side) | $L_{S1}$, $L_{S2}$ | 0.35μH |
| Tapped inductor | $L_{d1}$, $L_{d2}$ | $L_{d1}$ =35μH, $L_{d2}$ =1.1 μH, $N_L$ =0.14 |
| Output capacitor | $C_d$ | 540 μΦ |

Therefore $t_\delta$ is chose as 0.7μs to obtain maximum duty ratio over 0.8. Blanking time $t_d$ should be set to a value smaller than $t_\delta$ to maintain ZVS operation for $S_1$ and $S_2$, so $t_d$ was chosen as 0.5μs.

Fig. 7 illustrate experimental voltage and current waveforms under full and light load.

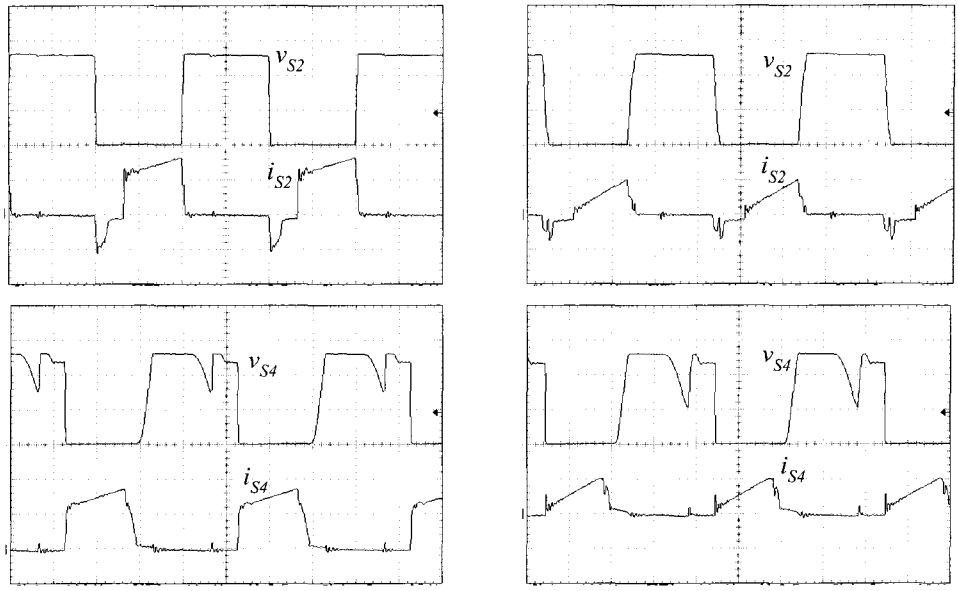


Fig. 7. Experimental waveforms of the converter; (a) E= 260V, $E_0$= 50V, Io=10A ($v_{s2}$: 100V/div., $i_{s2}$: 2A/div., $v_{s4}$: 100V/div., $i_{s4}$: 2A/div., time scale: 2.5μs/div.), (b) E= 260V, $E_0$= 50V, $I_0$= 2A ($v_{s2}$: 100V/div., $i_{s2}$: 1A/div., $v_{s4}$: 100V/div., $i_{s4}$: 1A/div., time scale: 2.5 μs /div.)

In both cases, it can be seen that switches $S_1$ and S2 operate with ZVS, and switches $S_3$ and $S_4$ operate under ZCS at turn-on and turn-off.

In Fig. 7 voltage $v_{s4}$ has a glitch. This does not match with the theoretical analysis shown in Fig. 4. In actual converters, switching devices have parasitic output capacitances ($C_{oes}$). Therefore, after transformer $T_2$ is reset (interval 8 in Fig. 5), output capacitance of $S_4$ starts discharging through $L_{p2}$ and $S_2$, and then $v_{s4}$ decreases with resonant mode. When $S_2$ is turned off, the output capacitance of $S_4$ recharges through $S_3$, $T_1$ (and $L_{s1}$) and $T_2$ (and $L_{s2}$), therefore $v_{s4}$ rises up to E. For this time, diode $D_6$ may be conducting. The recharged current through the output capacitance of $S_4$ has been observed as only a little value in $i_{s4}$ as shown in Fig. 7. If the parasitic capacitance completes discharging before $S_2$ is turned off, diode $D_9$ will starts conducting. Since the parasitic capacitances have been neglected in the theoretical waveforms shown in Fig. 4, $v_{S4}$ instantaneously falls down to zero when $T_2$ finishes resetting.

Fig. 8 shows the calculated and measured output voltage versus output current characteristics, taking the duty ratio as a parameter. As can be seen, the output voltage reduction caused by the presence of the leakage inductance $L_S$ is substantially low.

Fig. 9 shows the measured efficiency as a function of output current with a constant output voltage of 50V. The efficiency was 93.5% under full-load. When switch $S_3$ or $S_4$ turns on, its parasitic output capacitance is shorted, so turn-on losses in $S_3$ and $S_4$ exist. The turn-on loss is approximately calculated as $C_{oes}E^2f_s/2$=0.47W each in the experimental circuit.

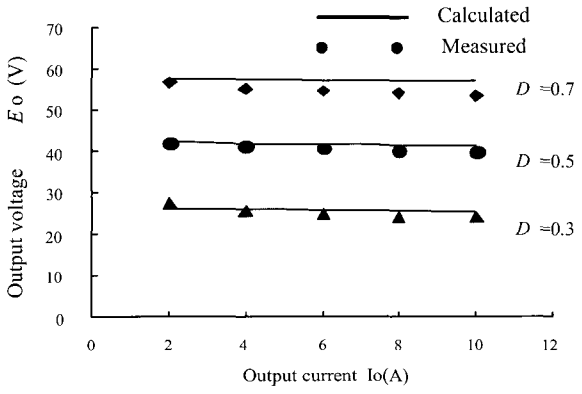


Fig. 8. Output voltage as a function of output current.

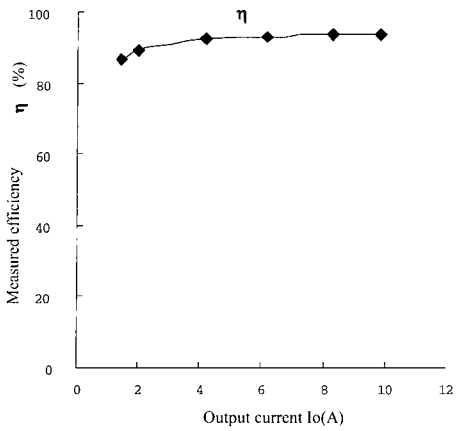


Fig. 9. Measured efficiency vs. output current under $E_0$= 50V.

## 5. Conclusions

The new double two switch forward soft-switching PWM DC-DC converter has been presented in this paper. The problem of the conduction losses occur due to circulating currents during freewheeling period has been solved due to make use of the unique circuit configuration with tapped inductor smoothing filter. High efficiency stable operation ability of the proposed converter has been verified by the experimental results.

Following features of the proposed converter has been revealed:

- Soft-switching operation in a wide range of load variation and PWM regulation.
- Free of complexity.
- Free of flux imbalance for the transformers.

The proposed soft-switching DC-DC power converter has enough ability to be used as high performance switch-mode power supply for high power applications.

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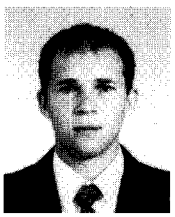

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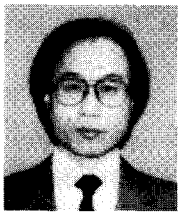

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