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A New PWM DC/DC Converter with Isolated Dual Output Using Single Power Stage

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ABSTRACT

This paper presents a new PWM DC/DC converter with dual output power using single power stage, which has the isolation characteristics between each dual output. The proposed converter topology consists of two switches (S_B and S_F) and only single secondary winding. Therefore, the proposed converter has better advantages of not only low cost and small size but also high power density because of using minimum components and devices compared with conventional methods which use multi winding transformers or several converters. The operating principle of the proposed converter topology, which includes the conventional auxiliary ZVT (Zero-Voltage-Transition) circuit to implement soft switching of the main switch, is illustrated in detail and the validity of the proposed converter is verified through several simulated and experimental results.

Keywords: Dual output power, Single power stage, Single secondary winding, Zero-Voltage-Transition (ZVT)

1. Introduction

Recently, with the remarkable progress of the power semiconductor devices and the control scheme, it is possible to achieve high power density in the low power conversion systems. In particular, in the Micro Air Vehicle (MAV) systems, these power conversion systems require more than one precisely regulated DC supply voltage since one is supplied to control circuit, like DSP, and other ones are supplied to the loads, like motor and accessory.

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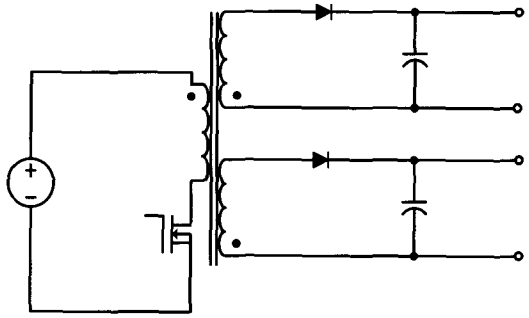
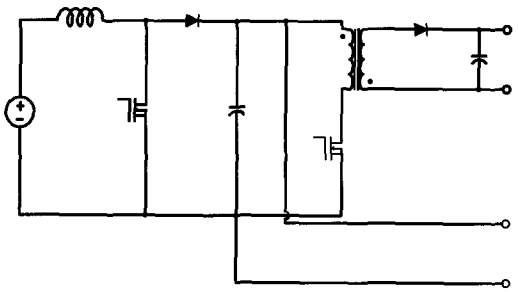
In general, Batteries are mainly used as the main input power source for these applications and must supply two different DC output voltages. Therefore, the isolation between control power and loads in these systems is positively necessary[1]-[3]. Also, these converter systems should be operated by high switching frequency to achieve the high power density of the power conversion system. However, the increase of the switching frequency makes the switching losses and noises. So, the various resonant converters have been used to reduce the switching loss such that the system efficiency is increased[4]-[6]. Until now there have been many works to achieve high power density of the power conversion system by the simplification and high efficiency of the system.

Fig. 1 shows the typical circuits to obtain the isolated dual output power for these objects such as



(a) Flyback converter with multi-winding



(b) Boost and Flyback converter

Fig. 1. Typical circuits to obtain the isolated dual output power.

the simplification and high efficiency. However, the circuits, shown in the Fig. 1(a) and (b), have several drawbacks as followings:

- Increase of the size because they have two power stages and two secondary windings.
- Difficulties of the design of multi transformer and the voltage control of two outputs.
- Low efficiency because of two times power conversion.

To solve these problems, a new PWM DC/DC converter with dual output power using single power stage is presented in this paper, which has isolation characteristics between each two outputs. The proposed converter topology consists of two switches (S_B and S_F) and only single secondary winding to obtain precisely regulated dual output voltage. Therefore, the proposed converter has advantages such as low cost, small size, high efficiency and high power density because of using minimum components and devices. The operating principles of the proposed converter topology, including the conventional ZVT (Zero-Voltage-Transition) circuit for soft switching of the main switch because the proposed converter system is operated at high switching frequency, are illustrated in detail. To verify the validity of the proposed converter system, simulation and experiment are performed.

2. The Proposed PWM DC/DC Converter with Dual Output

2.1 Circuit Description

Fig. 2 shows the proposed PWM DC/DC converter in this paper.

Basically, as shown in Fig. 2, the proposed converter has the structure of the conventional Boost converter which is lower one and the conventional Flyback converter which is upper one. The proposed converter circuit consists of two switches (S_B & S_F), a transformer with single secondary winding, two diodes (D_B & D_F) and two output filter capacitors (C_{OB} & C_{OF}). Between two switches (S_B & S_F), the switch S_F is used as a controllable switch to regulate output voltage of the upper converter accurately. Also the switch S_F achieves the ZVS turn-on by assistance of diode D_F.

At the proposed converter, a lower converter acts as Boost converter, and an upper converter acts as Flyback converter during one switching period respectively. Also, the operation of the proposed converter is decided by conditions of converter system such as input and output voltage and turns-ratio of the transformer.

Eq. (1) and (2) mean conditions of the input and output voltage of the proposed converter system and Fig. 3 shows the current and voltage of the magnetizing inductor during one switching cycle to represent the operation procedures of the proposed converter following Eq. (1) and (2) respectively.

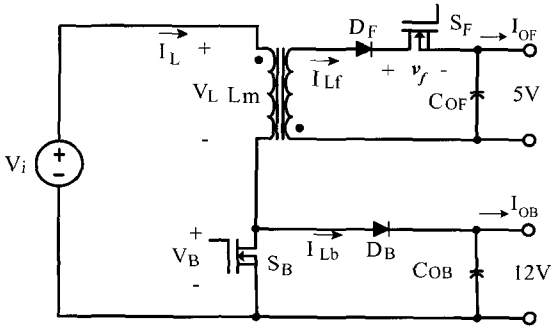


Fig. 2. The proposed PWM DC/DC converter circuit.

$$V_{OB} > nV_{OF} + V_i \quad (1)$$

$$V_{OB} = nV_{OF} + V_i \quad (2)$$

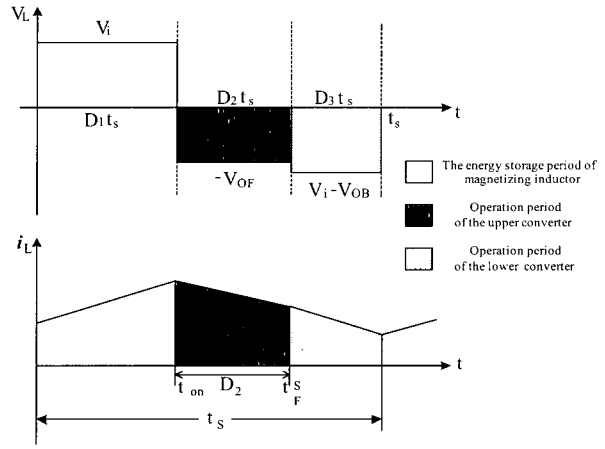
where, V_i: input voltage,

V_{OB}: output voltage of the lower converter

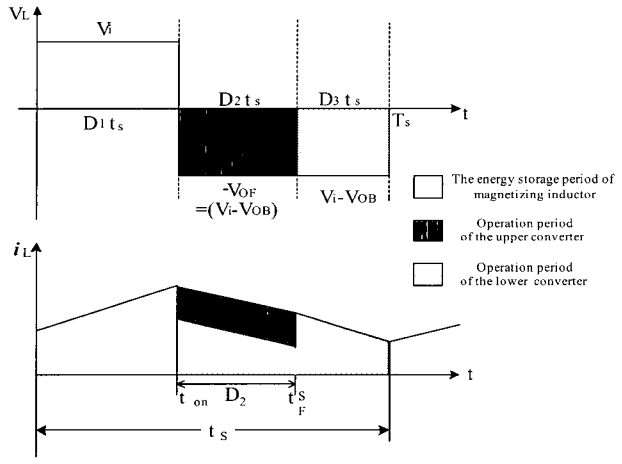
V_{OF}: output voltage of the upper converter,

n: turns-ratio of the transformer (N_1:N_2)

The essential reason having the operation sequences of the proposed converter as above mentioned is that the diode (D_B) of the lower converter is controlled by the magnitude of the voltage across the switch S_B after the switch S_B is turned off. Fig. 3(a) represents that the upper converter is operated first and then the lower converter is operated because the voltage across the switch S_B is less than the output voltage of the lower converter after the switch S_B is turned off. On the other hand, Fig. 3(b) shows that the upper and lower converter is operated at the same time because the diode D_B is simultaneously conducted after the switch S_B is turned off.



(a) Lower converter operation after upper converter one



(b) The simultaneous operation of upper and lower converter.

Fig. 3. The voltage and current of the magnetizing inductor during one switching cycle.

2.2 The steady-state analysis of the proposed converter

To obtain steady-state characteristics of the proposed converter, it is explained under following assumptions:

(1) All components and switches are ideal.

(2) The magnetizing inductance of the core is sufficiently large to be considered as a continuous current source.

(3) The output filter capacitances of C_{OB} and C_{OF} are so sufficiently large that the output voltage can be considered to be constant.

(4) The turns-ratio of the transformer is 1:1.

The steady-state analysis of the proposed converter is explained through Eq. (1) and (2) in detail and the analyzing procedures are the same as followings.

The output characteristics of the proposed converter are acquired through the following processes:

2.2.1 When V_{OB} is greater than V_{OF}+ V_i

Step 1. In case of an inductor operation under a steady-state condition, the average inductor voltage (averaged over one switching period) must be zero.

$$V_i D_1 = V_{OF} D_2 + (V_{OB} - V_i) D_3 \quad (3)$$

where, D_1: Duty ratio of the main switch, S_B.

D_2: Duty ratio of the switch of the upper converter, S_F.

D_3: Duty ratio of the diode of the lower converter, D_B.

Step 2. Sum of the switch duty ratios can be expressed as Eq. (4) during one switching period.

$$D_1 + D_2 + D_3 = 1 \quad (4)$$

Step 3. The stored energy in the magnetizing inductor of the transformer is delivered to the upper and lower converter through the switch S_F and the diode D_B by

turning on the switch S_B respectively. The delivered energy from the magnetizing inductor is equal to the average output power energy of the upper and lower converter respectively. Therefore, this can be represented by Eq. (5).

$$\frac{V_{OF} i_{Lf} D_2 T_S}{V_{OB} i_{Lb} D_3 T_S} = \frac{V_{OF} I_{OF} T_S}{V_{OB} I_{OB} T_S} \tag{5}$$

where, i_{Lf}: the current of switch S_F,

I_{OF}: the output current of the upper converter.

i_{Lb}: the current of diode D_B,

I_{OB}: the output current of the lower converter.

By using assumption (2), $i_{Lf} \cong i_{Lb} \cong i_L$

$$\frac{D_2}{D_3} = \frac{I_{OF}}{I_{OB}} = \gamma_P \tag{6}$$

where, γ_P : Power ratio of upper and lower converter.

By using Eq. (3) through Eq. (5), we can acquire the duty-ratios as followings respectively

$$D_1 = \frac{V_{OF}\gamma_P + V_{OB} - V_i}{\gamma_P(V_i + V_{OF}) + V_{OB}} \tag{7}$$

$$D_2 = \frac{\gamma_P V_i}{\gamma_P(V_i + V_{OF}) + V_{OB}} \tag{8}$$

$$D_3 = \frac{V_i}{\gamma_P(V_i + V_{OF}) + V_{OB}} \tag{9}$$

In Eq. (5), $I_{OF} = \frac{V_{OF}}{R_f}, I_{OB} = \frac{V_{OB}}{R_b}$ then, we can calculate Eq. (10).

$$\frac{V_{OB}}{V_{OF}} = \frac{R_b}{R_f \gamma_P} \tag{10}$$

Substituting Eq. (10) into Eq. (3) yields each voltage transfer ratio of the lower and upper converter as followings respectively:

$$V_{OF} = \frac{V_i(D_1 + D_3)}{D_2 + \frac{R_b D_3^2}{R_f D_2}} \tag{11}$$

$$V_{OB} = \frac{V_i(D_1 + D_3)}{D_3 + \frac{R_f D_2^2}{R_b D_3}} \tag{12}$$

2.2.2 When V_{OB} is equal to V_{OF}+ V_i

Step 1. In case of an inductor operation under a steady-state condition, the average inductor voltage (averaged over one switching period) must be zero. Thus, this is illustrated as

$$V_i D_1 = (V_{OB} - V_i)(1 - D_1) \tag{13}$$

Step 2. The stored energy in the magnetizing inductor of the transformer is simultaneously delivered to the lower and upper converter after the switch S_B is turned off. The ratio of the stored energy in the magnetizing inductor is the same as the ratio of consumed energy in their respective loads. Thus, it can be represented by Eq. (14).

$$\frac{V_{OF} i_{Lf1} D_2 T_S}{V_{OB}(i_{Lb1} D_2 + i_{Lb} D_3) T_S} = \frac{V_{OF} I_{OF} T_S}{V_{OB} I_{OB} T_S} \tag{14}$$

where, i_{Lf1}: the current of switch S_F during D_2,

i_{Lb1}: the current of diode D_B during D_2,

i_{Lb}: the current of diode D_B during D_3

Therefore, by assumption (2), Eq. (14) can be calculated as Eq. (15).

$$\frac{i_{Lf1} D_2}{i_{Lb1} D_2 + i_{Lb} D_3} = \frac{I_{OF}}{I_{OB}} = \gamma_{p1} \tag{15}$$

where, γ_{p1}: the power-ratio of the upper and lower converter.

Step 3. The magnetizing inductor current, i_L, in Fig. 3(b) is the sum of i_{Lf1} and i_{Lb1}.

$$i_L = i_{Lf1} + i_{Lb1} \tag{16}$$

From Eq. (15), (16), the current of each converter can be obtained as Eq. (17), Eq. (18).

$$i_{Lf1} = \frac{\gamma_{p1}(1 + \frac{D3}{D2})}{1 + \gamma_{p1}} i_L \tag{17}$$

$$i_{Lb1} = \frac{(1-\gamma_{p1}\frac{D3}{D2})}{1+\gamma_{p1}} i_L \tag{18}$$

From Eq. (15), we can obtain the relation between D_2 and D_3 as Eq. (19).

$$D_3 = \frac{(i_{Lf1} - \gamma_{p1} i_{Lb1})}{\gamma_{p1} i_L} D_2 \tag{19}$$

From Eq. (4), (13), (19), Duty equations are obtained as follows

$$D_1 = \frac{V_{OB} - V_i}{V_{OB}} \tag{20}$$

$$D_2 = \frac{\gamma_{p1} i_L}{i_{Lf1} + \gamma_{p1}(i_L - i_{Lb1})} \frac{V_i}{V_{OB}} \tag{21}$$

$$D_3 = \frac{i_{Lf1} - \gamma_{p1} i_{Lb1}}{i_{Lf1} + \gamma_{p1}(i_L - i_{Lb1})} \frac{V_i}{V_{OB}} \tag{22}$$

Therefore, the voltage transfer-ratio of the upper and lower converter can be obtained as following Eq. (23) and (24).

$$V_F = \frac{D_2 i_{Lf1}}{(D_2 + D_3) i_L - D_2 i_{Lf1}} \frac{R_F}{R_B} \frac{1}{1-D_1} V_d \tag{23}$$

$$V_B = \frac{1}{1-D_1} V_d \tag{24}$$

Until now, the steady-state analysis of the proposed converter was accomplished by two different conditions acorrding to the Eq. (1) and Eq. (2), above mentioned. From now on, we will only consider the case, Eq. (1) since operation principles of two cases, Eq (1) and (2), are almost equal.

3. Operation Principles of the New Converter

In power conversion system, power density and circuit performance of pulse-width-modulation (PWM) converter are generally improved by increase the switching frequency. Increasing of the switching frequency, however, makes switching losses, noises and severe di/dt and dv/dt, which produce electromagnetic interface (EMI) on the power semiconductor devices during the turn-on and turn-off transient state[4]-[6]. To operate the proposed converter at high frequency, therefore, the conventional ZVT auxiliary circuit, which is to accomplish ZVS of the main switch S_B, is added on the proposed converter as shown in Fig. 4.

The circuit has only one transformer with one secondary winding, a single power switch, S_B, and the auxiliary circuit that is composed of an auxiliary switch, S_{Ba}, a resonant inductor, L_r, and an auxiliary diode, D_{Ba}. The proposed converter has eight operating modes within one switching cycle. Fig. 5 shows the theoretical waveforms and Fig. 6 shows the eight topological operation stages of the proposed converter to be good agreement with the main waveforms shown in Fig. 5.

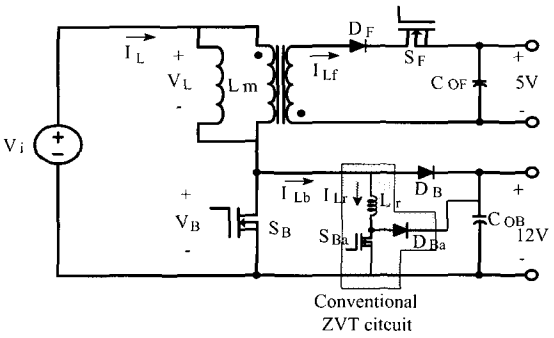


Fig. 4. Overall configuration of proposed converter added on the auxiliary circuit.

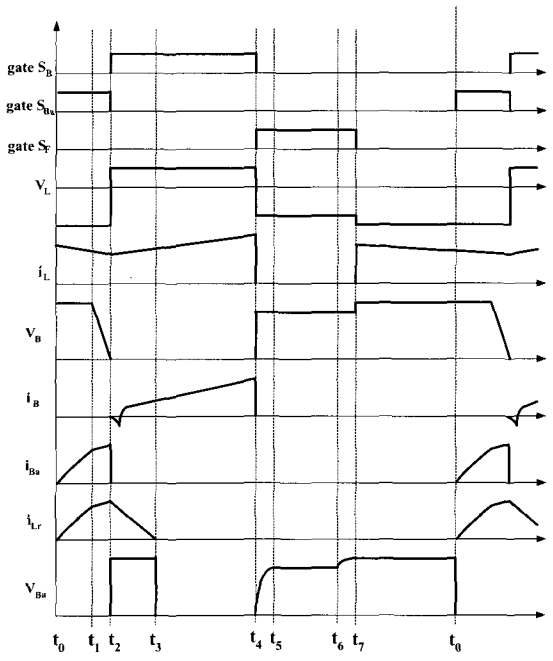


Fig. 5. The theoretical waveforms.

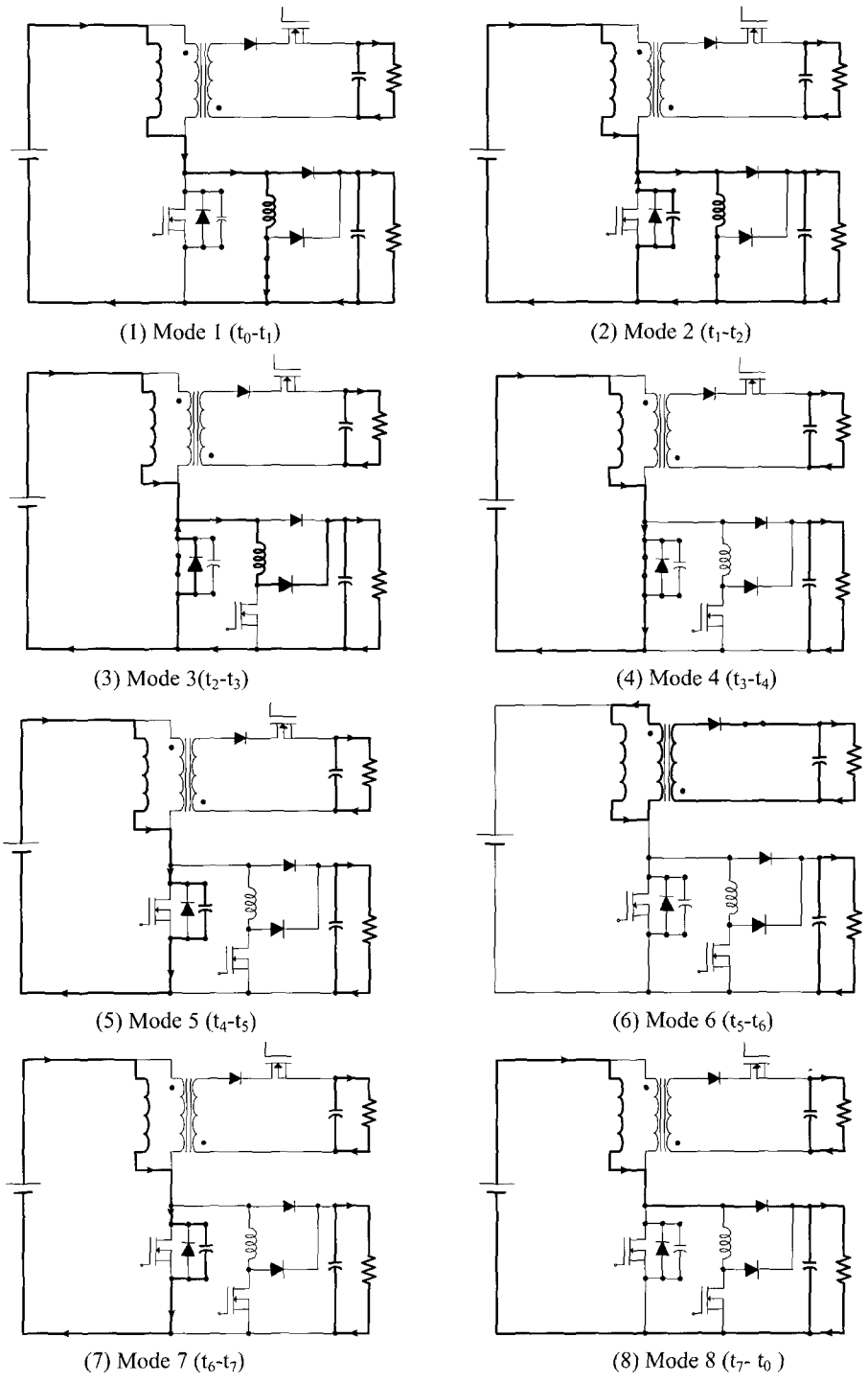


Fig. 6. Eight topological operation stages of the proposed converter.

(1) Mode 1 (t_0-t_1):

Prior to t_0, the main switch (S_B) and the auxiliary switch (S_{Ba}) of the lower converter and the switch (S_F) of upper converter are all off-state and primary current of the transformer is conducting through the diode (D_B) of the lower converter. At t_0, the auxiliary switch (S_{Ba}) is turned on and the current of the resonant inductor linearly ramps up until it reaches primary current of the transformer at t_1.

At this time, S_{Ba} is turned off with soft-switching. The resonant inductor current in this mode is

$$i_{Lr}(t) = \frac{V_{OB}}{L_r} t \tag{25}$$

(2) Mode 2 (t_1-t_2):

The auxiliary inductor current continues to increase due to the resonance between resonant inductor (L_r) and parasitic capacitor (C_r) of the main switch. C_r is discharged until the resonance brings its voltage to zero at t_2, where the anti-parallel internal diode of the main switch starts to conduct. The resonant current, i_{Lr}, and main switch voltage, V_B, are expressed as Eq. (26) and (27) respectively.

$$i_{Lr}(t) = \frac{V_{OB}\sin\omega_o t}{Z_o} + \frac{V_{OB}}{L_r} t \tag{26}$$

$$V_B(t) = V_{OB}\cos\omega_o t \tag{27}$$

where, $\omega_o = \frac{1}{\sqrt{L_r C_r}}$, $Z_o = \sqrt{\frac{L_r}{C_r}}$,

C_r: the lossless snubber capacitance including parasitic capacitance of the main switch.

(3) Mode 3 (t_2-t_3):

At t_2, the internal diode of the main switch is turn-on. The turn-on signal of the main switch must be applied to achieve ZVS while its internal diode is conducting. In this mode, the auxiliary switch is turned off and its voltage is clamped to the output voltage of the lower converter by the auxiliary diode. The stored energy of the resonant inductor is transferred to the output of the lower converter. The resonant current in this mode is

$$i_{Lr}(t) = I_{Lr}^{\max} - \frac{V_{OB}}{L_r} t \tag{28}$$

(4) Mode 4 (t_3-t_4):

The operation of the proposed converter at this stage is identical to that of the conventional Boost or Flyback converter. That is to say, the magnetizing inductor of the transformer acts as inductor of conventional Boost or Flyback converter and its current is represented by

$$i_L(t) = \frac{V_i}{L_m} t \tag{29}$$

where, L_m: the magnetizing inductance of the transformer.

(5) Mode 5 (t_4-t_5):

At t_4, the main switch (S_B) is turned off and the switch (S_{FD}) of the upper converter is turned on under zero voltage condition through the diode (D_F). The parasitic capacitor voltage (V_B) of the main switch is linearly charged by i_L to $V_{OF} + V_i$. The magnetizing inductor current (i_L) of the transformer and the voltage (V_B) of the main switch are as follows:

$$i_L(t) = \frac{V_i}{Z_1}\sin\omega_1 t + I_{L0}\cos\omega_1 t \tag{30}$$

$$V_B(t) = V_i\left(1 + \frac{\omega_1 D_1}{f_s}\sin\omega_1 t - \cos\omega_1 t\right) \tag{31}$$

where, $\omega_1 = \frac{1}{\sqrt{L_m C_r}}$, $Z_1 = \sqrt{\frac{L_m}{C_r}}$,

I_{L0} : Initial current of the magnetizing inductor.

(6) Mode 6 (t_5-t_6):

During this mode, the switch (S_F) of upper converter is only turned on. That is to say, the operation of the proposed converter is identical to that of the conventional Flyback converter during this interval. The output voltage of lower converter of the proposed circuit is higher than the applied voltage of the main switch and therefore the diode (D_B) of lower converter is not turned on. The current through the switch (S_F) of the upper converter and the voltage (V_B) of the main switch are explained as followings:

$$i_{Lf}(t) = I_{Lf} - \frac{V_{OF}}{L_m} t \tag{32}$$

$$V_B(t) = V_i + V_{OF} \tag{33}$$

where, $I_{Lf} = \sqrt{\left(\frac{V_i D_1}{L_m f_s}\right)^2 - \frac{C_r}{L_m}(V_i + V_{OF})^2}$,

I_{Lf}: the secondary peak current of the transformer.

(7) Mode 7(t_6-t_7):

The switch (S_F) of upper converter is turned off and the

voltage (V_B) of the main switch ramps up until it reaches the output voltage of the lower converter at t_6. At this time, the voltage (V_B) of the main switch is shown by

$$V_B(t) = V_{OB}\sin\omega_1 t - (V_i + V_{OF}) \quad (34)$$

(8) Mode 8(t_7-t_0):

During this mode, the stored energy of the magnetizing inductor of the transformer is delivered to the output side of the lower converter through the diode of the lower one. Namely, the proposed converter is identical to the conventional Boost converter. The current of the magnetizing inductor of the transformer can be explained by

$$i_L(t) = I_L - \frac{V_{OB}}{L_m}t \quad (35)$$

Here, the one cycle operation of the proposed converter is finished and then the proposed converter continues to repeat mode 1 to mode 8.

4. The Control Method of the Proposed Converter

Fig. 7 shows the total control block diagram of the proposed converter with dual output power.

As shown in Fig. 7, the control algorithm of the proposed dual output converter is mainly accomplished by lower converter system. Therefore, to execute precise control of each output, control loops consist of two different feedback loops as shown in Fig. 7. Between them, the upper part controls the upper converter and the lower part controls lower one. The voltage control of the upper converter is obtained by basing on the function between the error of the output voltage and the associated duty cycle calculated from lower converter. To acquire faster transient response and finer regulation of the proposed converter system, the control of the lower converter is achieved by using the peak current mode control scheme (PCM), which is attained by comparing the magnetizing current with the reference current, I^*, which is output of the voltage controller. Therefore, two outputs of the proposed converter are precisely regulated in case that input voltage or loads are perturbed.

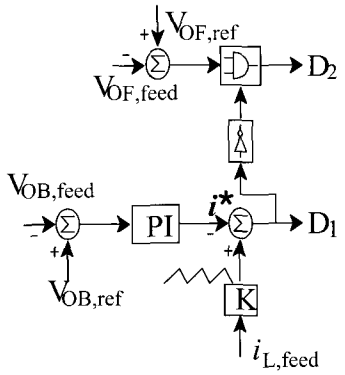


Fig. 7. The overall system block diagram.

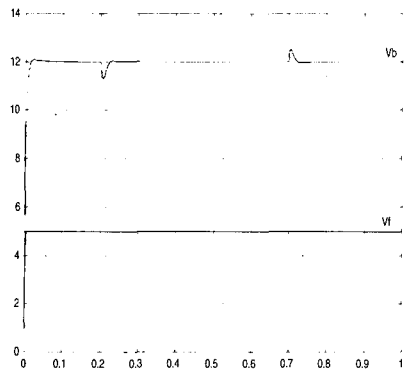
5. Simulated and Experimental Results

In order to verify the property of the proposed converter explained in section III, simulation and experiment were performed under the same conditions. Also, considering the difficulties at the realization of this circuit and the safe operation, system parameters are chosen as follows; input voltage, V_i, is varied from 3.5V to 7V, total output power, P_o=15W, including the upper (3W) and lower (12W) converter power respectively, and output voltage of upper and lower converter is 5V and 12V respectively; Switching frequency f_s =300kHz, turns ratio $n = n_1/n_2 = 0.7$, the lossless snubber capacitance $C_r = 1.2nF$ including parasitic capacitor of the switch, resonant inductance $L_r = 1uH$, output filter capacitance of the upper and lower converter $C_{oF} = 50uF$ and $C_{oB} = 50uF$ respectively, load resistance of upper and lower $R_f = 8\Omega$ and $R_b = 12\Omega$ in case of full load condition respectively.

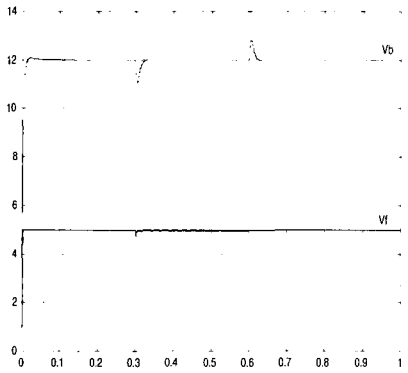
Also, to verify the validity of the proposed converter when the upper and lower converters are operated at the same time as shown in Fig. 3(b) by the condition Eq. (2) after the switch S_B is turned off, simulation and experiment were executed above the same system conditions and parameters except for output voltage of the lower converter, 10V.

5.1 Verification through the Simulated Results

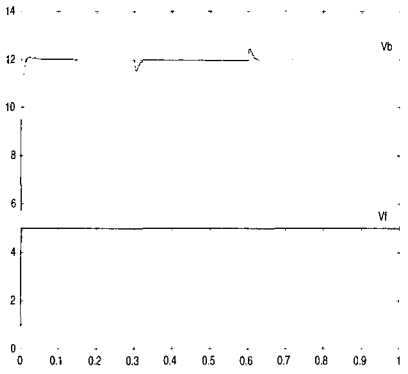
Fig. 8 and Fig. 9 show the simulated results of the proposed converter with two isolated outputs respectively.



(a) At the variation of the input voltage

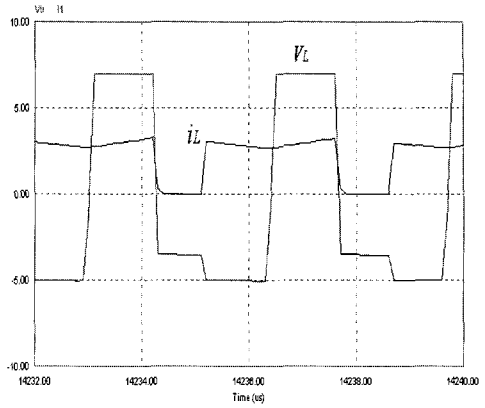


(b) In case of the load change of the upper converter

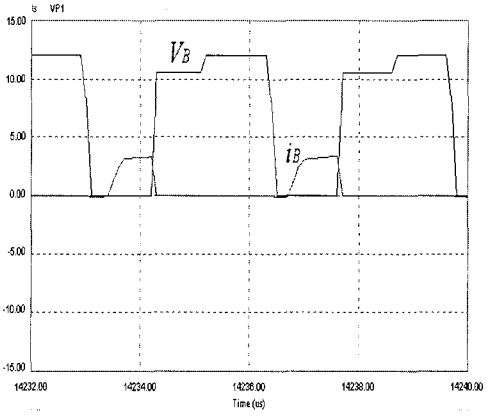


(c) In case of the load change of the lower converter

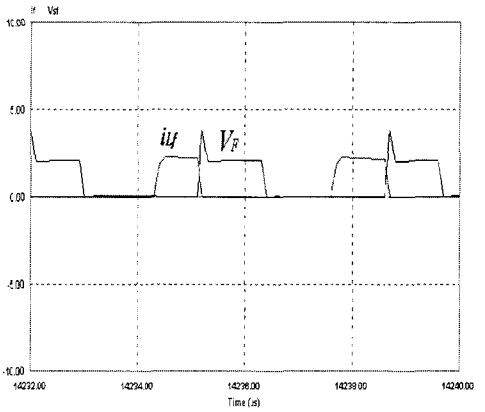
Fig. 8. The output characteristics of the proposed converter.



(a) Voltage and current of the primary side of the transformer



(b) Voltage and current of the switch S_B



(c) Voltage and current of the switch S_F

Fig. 9. Voltage and current of the switches (S_B & S_F) and the primary side of the transformer.

Fig. 8(a) shows the output voltage of the upper and lower converter of the proposed converter in case that its input voltage is varied from 6V to 3.5V at t=0.2ms and from 3.5V to 5V at t=0.7ms respectively.

From this result, it is shown that all output voltages of upper and lower converter of the proposed converter are exactly regulated. It is the primary merit of the proposed converter because the proposed converter is constituted to the only single power stage. Changing load of the proposed dual output converter, Fig. 8(b) and (c) show its

output voltage respectively. Fig. 8(b) varies the load of upper converter at t=0.3ms and at t=0.6ms 10% to 100%, 100% to 10% respectively, and Fig. 8(c) varies the load of the lower one at t=0.3ms and at t=0.6ms like the upper converter respectively. From Fig. 8(b) and (c), we show that the two outputs of the proposed converter are precisely regulated in which loads are changed. As known by the results so far achieved, it can be known that the proposed converter is able to regulate the isolated dual output voltage using the only single secondary winding.

Fig. 9 shows voltage and current of the proposed converter respectively. Fig. 9(a) shows the voltage and current waveforms of the primary side of the transformer. From this result of Fig. 9(a), this means that lower converter of the proposed system is operated after upper converter is operated first. Fig. 9(b) shows the voltage and current of the switch, S_B. From Fig. 9(b), it is shown that the switch, S_B, is turned on under zero-voltage switching condition acquired by operating the auxiliary circuit, conventional ZVT circuit. Fig. 9(c) shows the voltage and current of the switch, S_F. Here, the switch S_F, which is added to regulate the output voltage of the upper converter precisely, is turned on under condition of zero voltage by the diode, D_F. From these results of Fig. 9, we know that the operation of the proposed converter is divided into two steps. Also, Fig. 8 and Fig. 9 show that the simulated results are good agreement with theoretical analysis.

Fig. 10 shows the simulated result when the upper and lower converters are operated at the same time as shown in Fig. 3(b) by the condition Eq. (2).

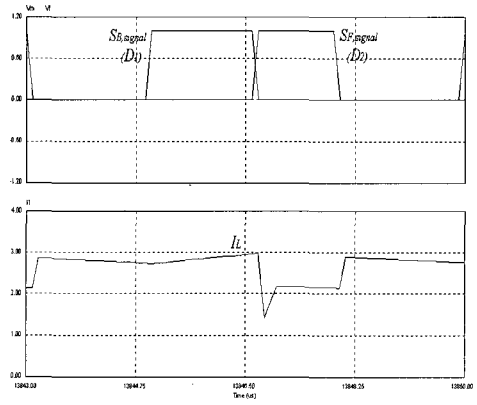


Fig. 10. The executed simulation result when the upper and lower converters are operated at the same time as shown in Fig. 3(b) by the condition Eq. (2).

Fig. 10 shows switching signals of the switches, S_B and S_F, and the current waveform of the primary side of the transformer. As a result, as the explained the proposed converter in section II, we can know that the upper and lower converters are operated at the same time after the switch (S_B) is turned off, because the primary current of the transformer, i_L, flows continuously. Therefore, Fig. 10 shows that the simulated results are good accordance with theoretical analysis.

5.2 Verification through the experimental Results

A circuit had been built and measurements were taken from the prototype in order to demonstrate the simulated results and verify the validity of the analysis and the circuit operation.

To implement experiment, the following devices are used as followings:

- Switch (S_B, S_F, S_{Ba}): FDS4410,
  Diode (D_B, D_F, D_{Ba}): FE6D
- Transformer: Ferrite Core PC409727Z

The power stage diagram is depicted in Fig. 11. Clamping circuit has been used in order to reduce the effect of the leakage inductance of the transformer on the power devices.

Fig. 12, 13 and 14 show the output characteristics of the proposed converter for the variation of input voltage and load conditions.

Fig. 12 shows output characteristics in case of the variation of the input voltage. Fig. 12(a) and (b) show that

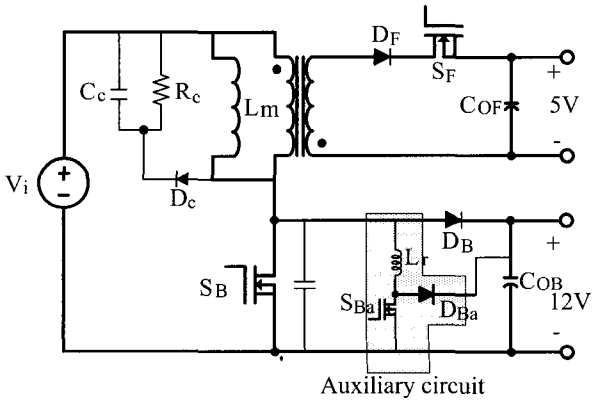
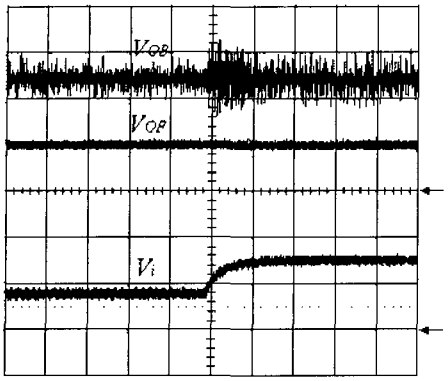
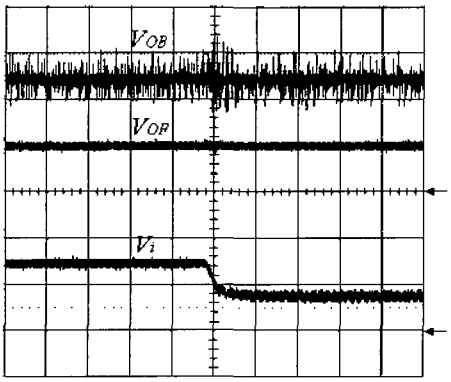


Fig. 11. Power stage diagram of the proposed converter.

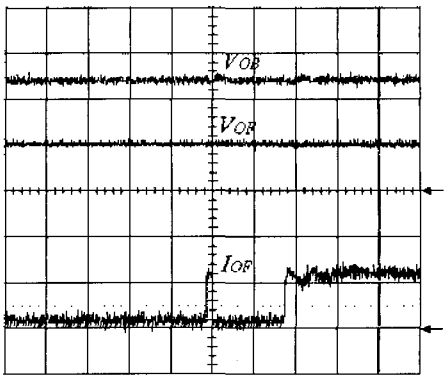


(a) V_{OB}, V_{OF}, V_i (5V/div., time: 50ms/div.)

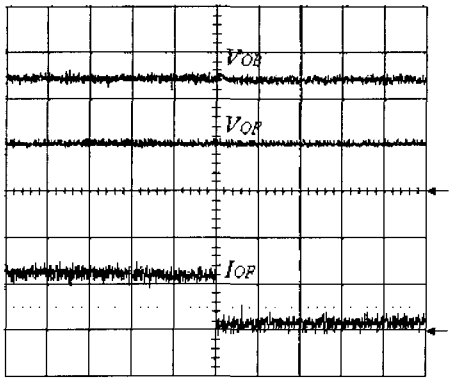


(b) V_{OB}, V_{OF}, V_i (5V/div., time: 50ms/div.)

Fig. 12. In case of the variation of the input voltage.



(a) V_{OB}, V_{OF}, I_{OF} (5V/div., 0.5A/div., time: 0.2ms/div.)



(b) V_{OB}, V_{OF}, I_{OF} (5V/div., 0.5A/div., time: 0.2ms/div.)

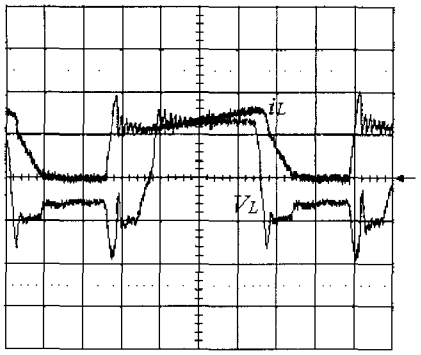
Fig. 13. In case of the load variation of the upper converter.

input voltage is varied from about 3.7V to 7 and from 7 to 3.7 respectively. From this result, it is shown that all output voltages of upper and lower converter of the proposed converter are exactly regulated by the control scheme explained in section IV although input voltage is varied.

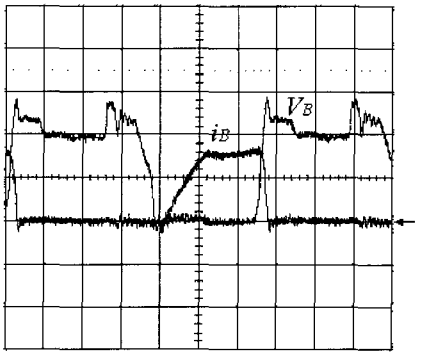
Fig. 13 and Fig. 14 show output characteristics in case that the load variation of upper and lower converter occurs respectively. Fig. 13 (a) and (b) show the changed load conditions of upper converter from 10% to 100% and from 100% to 10% respectively, and Fig. 14(a) and (b) show the changed load conditions of the lower one from 10% to 100% and from 100% to 10% respectively. From Fig. 13 and 14, they can be shown that the two outputs of the proposed converter are precisely regulated in which loads are changed. In view of the results so far achieved, it can be known that the proposed converter can regulate the isolated dual output voltage using the only single secondary winding.

In case that input voltage is 7V, the key voltage and current waveforms of the proposed converter are shown in Fig. 15(a)-(c). Fig. 15(a) shows the voltage and current of the primary winding. Fig. 15(b) and (c) present the voltage and current of the switch S_B and S_F respectively. From in Fig. 15(b) and (c), it can be found that the two switches S_B and S_F are turned on under zero voltage. Consequently, all experimental results are good accordance with the simulated results.

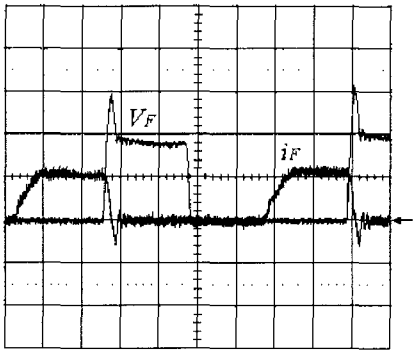
The experimentally measured efficiency curve of the proposed converter with isolated dual output using single power stage is shown in Fig. 16. The measured efficiency versus the input voltage is shown in Fig. 16(a). The efficiency slightly increases as input voltage is increased because the average input current decreases with increasing input voltage in constant output power operation and conduction loss becomes smaller. Fig. 16(b) shows the measured efficiency of the proposed converter versus total output power in case that input voltage is 7V



(a) i_L, V_L (5V/div., 2A/div., time: 0.5us/div.)



(b) V_B, i_B (5V/div., 2A/div., time: 0.5us/div.)

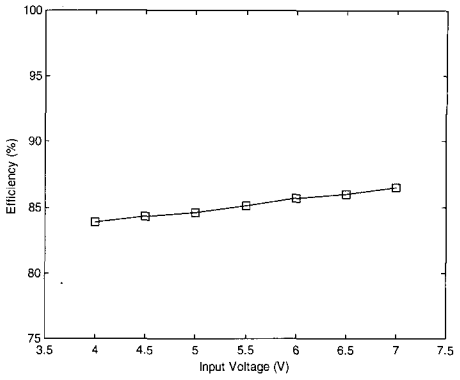


(c) V_F, i_F (5V/div., 2A/div., time: 0.5us/div.)

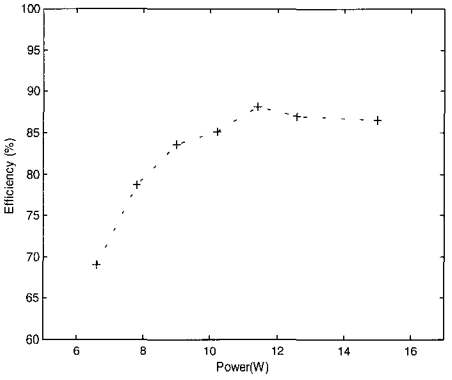
Fig. 15. The key voltage and current waveforms of the proposed converter.

and the load of the lower converter is only varied from 100%(12W) to 30%(3.6W). The measured efficiency of the proposed converter was about 86.5% at full load.

Fig. 17 shows the experimental result when the proposed converter is operated as Fig. 3(b) by the condition Eq. (2). Fig. 17 shows switching signals of the switches, S_B and S_F, and the current waveform of the primary side of the transformer.

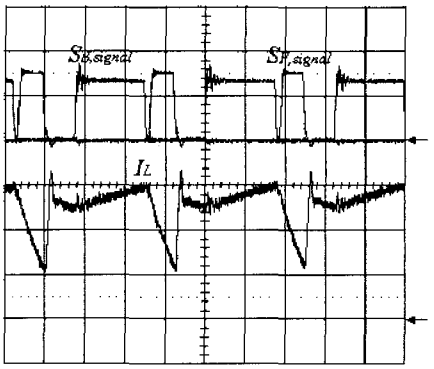


(a) Input voltage



(b) The output power

Fig. 16. Experimentally measured efficiency.



(5V/div., 2A/div., time: 1us/div.)

Fig. 17. The experimental result by the condition of the Eq. (2).

Therefore, as the explained in section II, it can be shown that the upper and lower converters are operated at the same time after the switch (S_B) is turned off. Consequently, Fig. 17 shows that it is good accordance with the simulated results.

6. Conclusion

A new PWM DC/DC converter with mutually isolated two outputs using single power stage is presented in this paper. The output characteristics and operation principle of the proposed converter are explained in detail. The validity of the proposed converter was verified through the simulated and experimental results.

The main features of proposed converter topology are:

- Simplification of the overall system because it is composed of the single power stage
- Small size and lightweight of the converter system due to higher operating switching frequency
- High power density of the proposed converter system
- Soft switching of all switching devices.

Therefore, the proposed converter can be applied to a field acquiring low power and high power density.

Acknowledgements

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