論文2002-39SD-12-5

# Grounded-Plate PMOS 게이트 강유전체 메모리 셀을 이용한 새로운 FRAM 설계기술에 관한 연구

# (A Feasibility Study on Novel FRAM Design Technique using Grounded-Plate PMOS-Gate Cell)

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요 약

본 논문에서는 grounded-plate PMOS 게이트 (GPPG) 강유전체 메모리 셀을 이용한 새로운 FRAM 설계기술을 제안하였다. GPPG 셀은 PMOS와 강유전체 커패시터로 구성되며 셀 plate 는 ground 에 접지된다. 제안된 FRAM 에서는 비트라인이 $V_{DD}$ 로 precharge 되고, negative 전압 워드라인 기법이 사용되며, negative 펄스 restore 동작을 이용한다. GPPG 셀을 이용한 FRAM 구조는 셀 plate 구동기를 사용하지 않으므로 메모리 셀 efficiency를 극대화 할 수 있는 장점이 있다. 또한 기존의 common-plate 셀과는 달리 제안된 FRAM 구조는 데이터의 읽기 및 쓰기 동작 시 강유전체 커패시터에 $V_{DD}$의 충분한 전압이 가해지므로 저 전압 동작에 제한이 없다. 아울러 제안된 FRAM 구조는 필요한 8 비트 데이터만 선택하는 column-path 회로를 사용하므로 메모리 array 전력소모를 최소화 할 수 있다. 끝으로 0.5-um, triple-well/1-polycide/2-metal 공정을 이용한 4-Mb FRAM 설계를 통해 GPPG 셀 FRAM architecture 실현 가능성을 확인하였다.

**Abstract**

In this paper, a new FRAM design technique utilizing grounded-plate PMOS-gate (GPPG) ferroelectric cell is proposed. A GPPG cell consists of a PMOS access transistor and a ferroelectric data storage capacitor. Its plate is grounded. The proposed architecture employs three novel methods for cell operation: 1) $V_{DD}$-precharged bitline, 2) negative-voltage wordline technique and 3) negative-pulse restore. Because this configuration doesn't need the plate control circuitry, it can greatly increase the memory cell efficiency. In addition, differently from other reported common-plate cells, this scheme can supply a sufficient voltage of $V_{DD}$ to the ferroelectric capacitor during detecting and storing the polarization on the cell. Thus, there is no restriction on low voltage operation. Furthermore, by employing a compact column-path circuitry which activates only needed 8-bit data, this architecture can minimize the current consumption of the memory array. A 4-Mb FRAM circuit has been designed with 0.5-um, triple-well/1-polycide/2-metal technology, and the possibility of the realization of GPPG cell architecture has been confirmed.

**Keyword** : Memory, ferroelectrics, FRAM, nonvolatile, GPPG ferroelectric cell

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接受日字:2002年2月25日, 수정완료일:2002年11月5日

## I. Introduction

As modern portable electronic systems such as

cellular phone, personal digital assistant and mobile computer become popular, there is an increasing demand for nonvolatile memories featuring high speed and low power consumption. The ferroelectric random access memory (FRAM) has a great potential to create such a memory because of its low voltage operation, fast read/write time and high read/write endurance. High reliability and small die size are a crucial requirement for the new generation of FRAM's.

The FRAM design requires a decision regarding how to operate the cell capacitor plate. Up to now, two kinds of cell-plate schemes for the FRAM have been reported: 1) decoded pulse-driven plate scheme [1~5] and 2) common half-$V_{DD}$ plate scheme.[6,7] The pulsed cell-plate scheme drives a heavy capacitive load of the cell plateline. This large on-pitch plate driver results in lots of circuit overhead for plate control, so that it causes relatively low cell array efficiency. On the other hand, the half-$V_{DD}$ cell-plate scheme is not suitable for low voltage operation because it cannot apply a sufficient voltage to the ferroelectric capacitor.

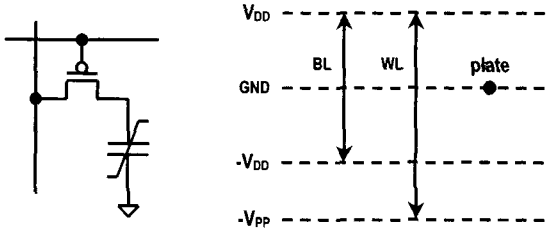



그림 1. 제안된 GPPG 강유전체 메모리 셀. 워드라인, 비트라인, 커패시터 plate 의 바이어스 영역을 표시하였음

Fig. 1. Proposed GPPG ferroelectric cell. Each bias range of wordline (WL), bitline (BL) and capacitor plate is indicated.

To overcome the above problems, a new ferroelectric memory design technique utilizing grounded-plate PMOS-gate (GPPG) ferroelectric cell is proposed. The configuration of proposed GPPG cell is shown in <Fig. 1>. The memory cell consists of a PMOS access transistor and a ferroelectric data storage capacitor. A unique feature of the proposed GPPG cell is that it doesn't require the plate decoding. The plates are tied to ground to be able to keep different polarity of voltage across the capacitors. Instead, the voltage bias of $V_{DD}$ to $-V_{DD}$ across the capacitors is supplied through the bitline (BL). The wordline (WL) voltage is switched from $V_{DD}$ to $-V_{PP}$ to select the cell. The voltage level of $-V_{PP}$ reaches sufficiently negatively below $-V_{DD}$ to make the cell transistor turn on even if the bitlines are biased to $-V_{DD}$, so that the ferroelectric capacitor is written fully to saturation. The needed negative voltages, $-V_{DD}$ and $-V_{PP}$, can be readily generated by a conventional negative charge pump circuit. As a result, it offers two natural benefits. The first is that this configuration realizes no circuit overhead for plate control. The second is that this scheme can supply a sufficient voltage of $V_{DD}$ to the ferroelectric capacitor during detecting and storing the polarization on the cell.

A 2.5-V, 4-Mb FRAM circuit using 0.5-um design rule has been designed in this paper, and the possibility of the realization of GPPG cell architecture has been confirmed. In Section II, the basic read/write operation of the GPPG cell is described. In Section III, technology about the memory cell and the peripheral transistors using triple-well structure is discussed. In Section IV, the detailed circuit design using GPPG ferroelectric cell is presented. In Section V, the performance of 4-Mb FRAM is estimated. Finally, the conclusion is given in Section VI.

## II. Read and Write Operation

<Fig. 2> shows the proposed GPPG cell array, and <Fig. 3> illustrates its read and write operation. There are three operational differences between the GPPG cell and the conventional FRAM cell: 1) $V_{DD}$-precharged bitline, 2) negative-voltage wordline access and 3) negative-pulse restore.

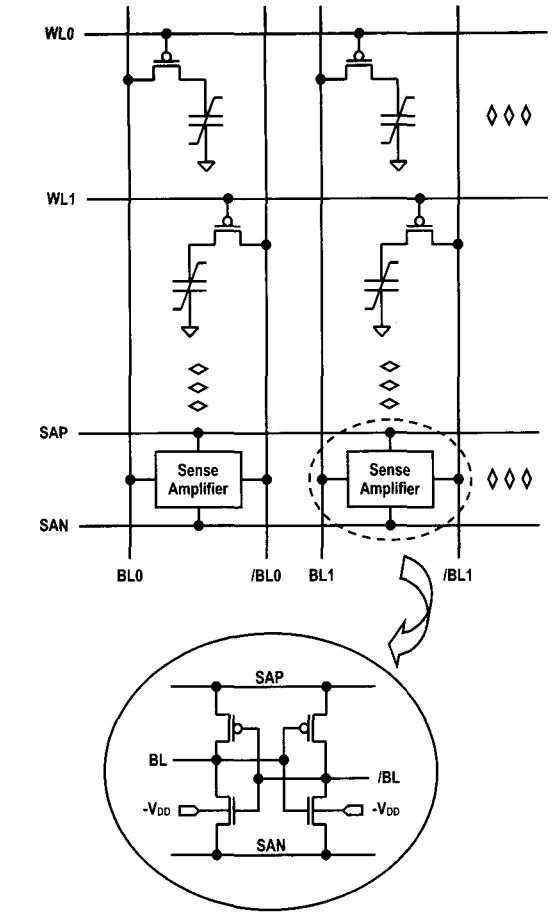
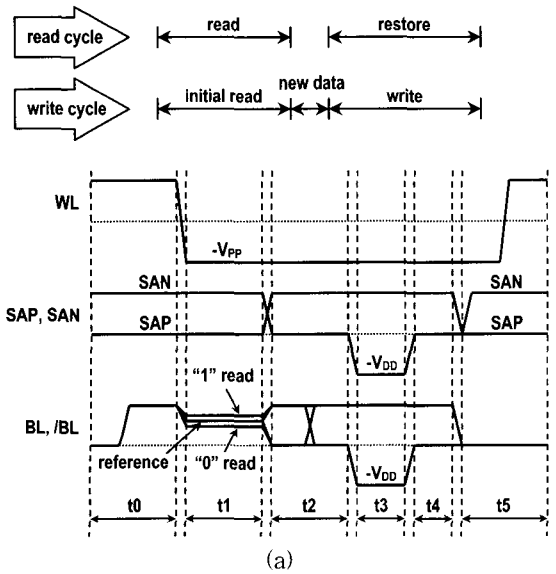
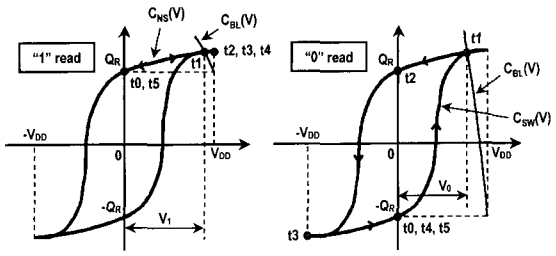



그림 2. GPPG FRAM 셀의 array 형태
Fig. 2. Basic GPPG FRAM cell array.




(a)




(b)

그림 3. 읽기 및 쓰기 동작: (a) 타이밍, (b) 읽기동작 중 메모리 셀의 분극상태
Fig. 3. Read/write operation: (a) timing, (b) polarization state of memory cell during read cycle. ($Q_R$: remnant charge).

In read operation, first, the bitline pairs are precharged to $V_{DD}$ and then floated. The cell access transistor is PMOS, which means that all of the non-selected wordlines are connected to $V_{DD}$. To read out a stored value in a GPPG cell, the wordline is switched from $V_{DD}$ to $-V_{PP}$. Charges transfer from bitlines to ferroelectric capacitors, producing a data voltage on bitlines. Referring to <Fig. 3(b)> which shows the polarization state of each time duration of t0-t5, the bitline voltage $V_1$ for the 1 state cell is

$$V_1 = \frac{C_{BL}(V = V_{DD}) \cdot V_{DD}}{C_{BL}(V = V_1) + C_{NS}(V = V_1)} \quad (1)$$

where $C_{BL}$ and $C_{NS}$ are bitline capacitance and non-switching cell capacitance, respectively. For the 0 state cell, the resulting bitline voltage $V_0$ is a function of the charge switched within the ferroelectric material, that is,

$$V_0 = \frac{C_{BL}(V = V_{DD}) \cdot V_{DD}}{C_{BL}(V = V_0) + C_{SW}(V = V_0)} \quad (2)$$

where $C_{SW}$ is the switching cell capacitance. At the same time, a reference voltage needed for sensing the bitline voltages is generated in the currently non-selected bitlines. It is a mid-level voltage between data "1" and data "0". (Detailed scheme of reference circuit is presented in Section IV.) Then, a sense amplifier (SAP and SAN) connected to the bitline pair amplifies the differential voltage between bitlines. The bitlines corresponding to cells with data

1 are driven to the full $V_{DD}$ level and the bitlines corresponding to the cells with data 0 are driven to ground. After sensing the data, SAN is brought to $-V_{DD}$ level for the restore operation. It will bring the data "0" bitlines to $-V_{DD}$ level. As a result, $-V_{DD}$ bias voltage is kept across the capacitors of the data "0" cell. Then, SAN is switched again to ground. After this negative pulse restore, the sense amplifiers are disabled and the bitlines are brought to ground. Finally, the wordline is pulled up to $V_{DD}$.

To write a value into the GPPG cell, the internal timing is similar to that of the read operation. After the sense amplifiers have determined the initial state of the accessed memory cells, a write request allows changing data state on the selected bitlines when the column gate is enabled. It is done by a write driver during t2 in <Fig. 3(a)>. With the bitlines held in their new state, SAN is brought to $-V_{DD}$ level. Then, the new data state is stored into the ferroelectric capacitors: that is, the "0" data is written into the cell with $-V_{DD}$ bitline and the "1" data is written into the cell with $V_{DD}$ bitline.

## Ⅲ. Process Technology

In this section, process technology to realize the proposed FRAM architecture is discussed. <Fig. 4> shows the cross section of the memory cell and peripheral transistors. In this process design, a 0.5-um ferroelectric storage cell integrated CMOS process with triple-well, 1-polycide, 2-metal has been adopted. The separated-body NMOS transistors are made in pocket p-well (pp-well). The voltage level of $-V_{PP}$ is chosen as -1.8 times of $V_{DD}$, that is, $-V_{PP} = -1.8V_{DD}$. The maximum voltage applied to the transistors is $2.8V_{DD}$. Therefore, if $V_{DD}$ is below 3.3 V, no high voltage transistors are needed since the conventional 5-V CMOS transistors have the breakdown voltages above 10 V.

As shown in the figure, the memory cell has the planar-stacked capacitor structure with ferroelectric thin film. The bitline is wired under the storage

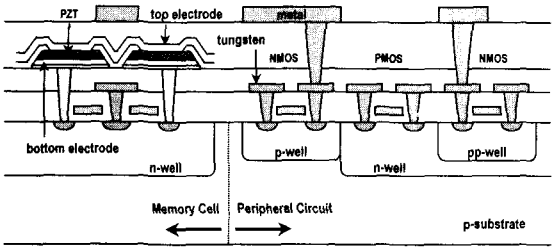



그림 4. Device 단면도
Fig. 4. Process architecture.

capacitors. It is made of tungsten. In order to reduce the fabrication process steps, the source/drain metal of peripheral transistors is made with the same layer as that of bitline. The bridges in the peripheral area also are made by tungsten layer. Before the capacitor process, the surface of the chip is polished by a chemical mechanical polish (CMP) process to allow precision lithography of the capacitor layers. This construction simplifies the process, mitigating differences in height between the cell and the peripheral area. The ferroelectric capacitor is made of PZT with the oxide electrode. The second metal layer (Al) is used for the wordline strapping in cell area. It is also used for long signal lines and power lines in peripheral area.

In drawing cell layout, the capacitor layout has been first formed with the minimum design rules, because the scaling limit of FRAM cell is on a pitch size of the ferroelectric capacitor, that is, etching of the ferroelectric material and its electrode material. Then, cell transistor layout has been formed under the capacitor within the allowed design rules tolerant. The PMOS access transistor can be fabricated with same size as the conventional NMOS access transistor, by controlling threshold voltage implantation and adjusting junction depth. Thus, there is no penalty on cell size due to access transistor. As the result, an 8.32 $um^2$ cell has been obtained. The channel width and length of the cell transistor is 2.6 um and 0.5 um, respectively. The capacitor size is 1.87 $um^2$.

## Ⅳ. Details of Circuit Design

In this section, circuit techniques using the proposed GPPG cell are described to realize a 4-Mb FRAM organized as 512K-word by 8-bit. The design is based on the process technology discussed in the above section.

### 1. Block Array Architecture

<Fig. 5> details the logical and physical organization of memory array architecture. The 1-Mb memory cells are divided into two horizontally mirrored top and bottom 512-Kb blocks. The column signal generators are positioned at the middle of the two blocks and are shared by two blocks. Inside of a 512-Kb block, the sense amplifier (SA), the bitline bias transistor and column gate are located near the column signal generator. The reference circuitry, which provides a reference voltage in the bitlines, is positioned at the other side of sense amplifiers in the array.

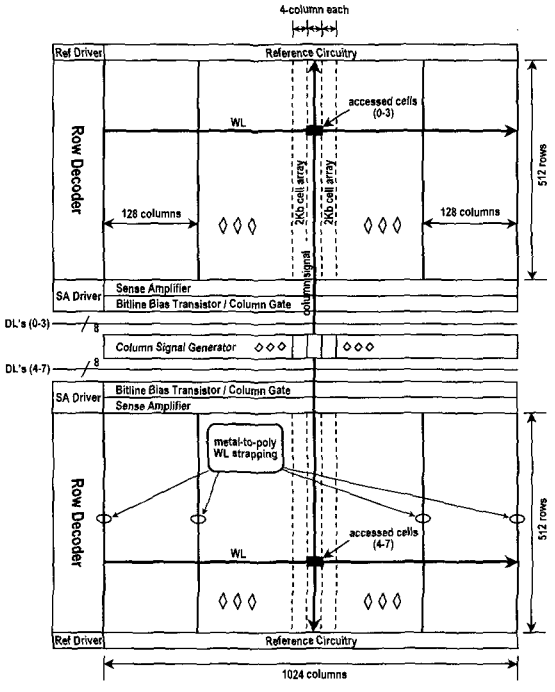



그림 5. Block array 구조

Fig. 5. Block array architecture. (Ref Driver: reference circuit driver, SA Driver: sense amplifier driver, DL: dataline).

Each 512-Kb block contains 512 WL's and 1024 bitline pairs. The 2048 BL's, each coupling to 256 cells, are supported by 1024 SA's. When a 1-Mb unit is selected, two WL's (one from the top 512-Kb block and the other from the bottom 512-Kb block) are activated simultaneously. Each wordline (polycide) supporting 1024 cells is strapped every 128 cells with metal (9 straps/WL). In a column phase, each column signal generator selects two sets of 4-bit data simultaneously, resulting in 8-bit activation. The sense amplifiers in the unselected columns are not latched, and the bitlines in the unselected columns remain to 0 volt. Although 1024 cells are enabled during each wordline access, the data in unselected columns are not activated since there is no voltage difference between the cell plate and the bitline. The 8-column selection during each cycle greatly reduces the memory array power dissipation because the majority of array power budget is allocated to precharge, data sensing and restore of selected columns.

### 2. Row Decoder

In this work, a negative-voltage wordline technique is required: that is, WL's logic "high" level is $V_{DD}$ and logic "low" level is $-V_{PP}$. <Fig. 6> shows a developed row decoder circuit and its simulated waveforms. This circuit consists of a precharged NAND gate, latch and negative level shifter. At the beginning of the access, the precharge signal RPCHG makes node A of the level shifter the ground level so that WL is pulled up to $V_{DD}$ by M1. Transistor M3 is turned on and M4 is turned off, holding the node B at $-V_{PP}$. When the row decoder is selected, the node A and B are pulled up to $V_{DD}$. Now, M1 is turned off and M2 is turned on so that WL is pulled down to $-V_{PP}$ by M2. When the row decoder is deselected, the signal RPCHG returns the level shifter to the initial state. The rising and falling time of WL signal is about 10 ns.

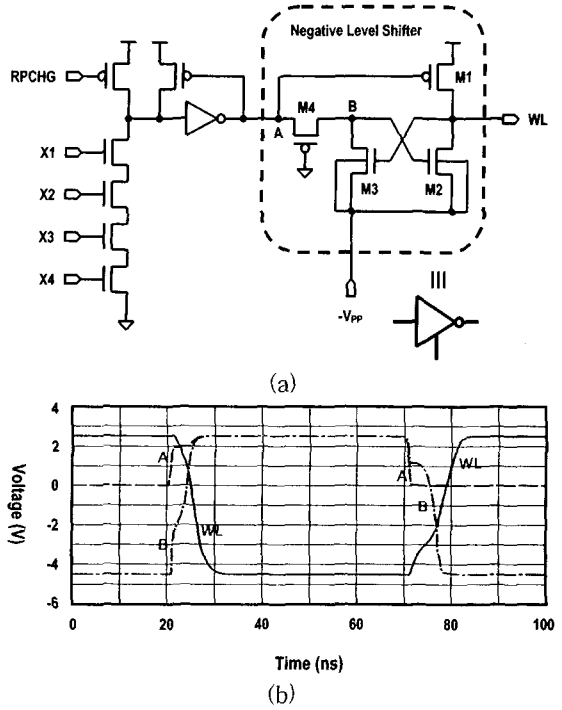



그림 6. 행 디코더: (a) 회로, (b) 모의실험 파형 ($V_{DD}$ = 2.5 V, $-V_{PP}$ = -4.5 V, T = 25 ℃

Fig. 6. Row decoder: (a) circuit configuration, (b) simulated waveforms at $V_{DD}$ = 2.5 V, $-V_{PP}$ = -4.5 V and T = 25 ℃. (X1-X4: row decoding signals).

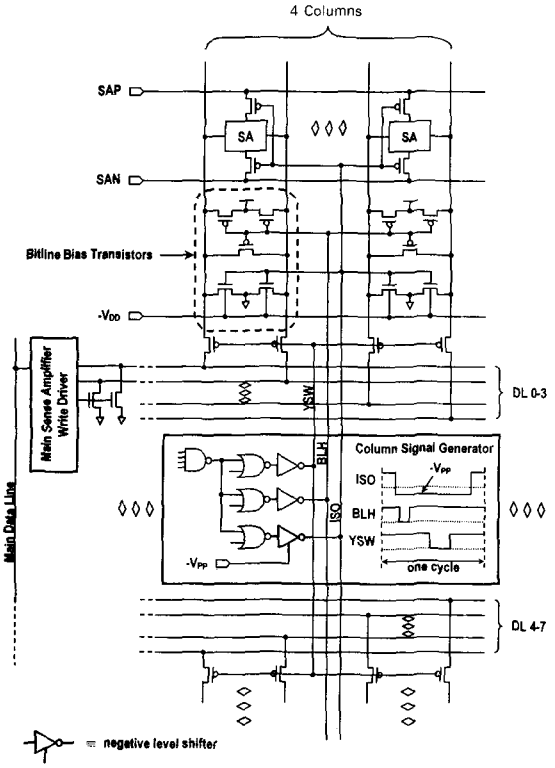



그림 7. 컬럼 회로

Fig. 7. Configuration of column path circuits.

3. Column Path Circuits

<Fig. 7> shows a detailed circuit configuration of bitline sense amplifier, bitline bias transistors, column-path gate and column signal generator. In this design, a column selected SA scheme is employed. The sense amplifier is selected by PMOS transfer gate. For each access, the column signals (ISO, BLH, YSW) enable and disable the bitline bias transistors, sense amplifiers, and column-pass gates, only in two sets of 4 columns. Here, the negative-voltage technique is used once again for ISO signal. The ISO's logic "high" level is $V_{DD}$ and logic "low" level is $-V_{PP}$. The remaining un-accessed columns are undisturbed because the bitlines are clamped to ground, the sense amplifiers are isolated from SAP and SAN signals, and column-path gates stay turned off.

Two set of 4-bit bi-directional data bus transfer data and /data signals between MSA/WDR (main sense amplifier and write driver) and the selected bitlines. For each cycle, dataline (DL) and /dataline (/DL) are initially precharged to 0 volt and then floated. The column-path gate is consisted of a PMOS transistor. The logic "0" level of YSW activates two sets of eight column-pass gates simultaneously. During the read cycle, two sets of 4-bit data are sensed by the bitline sense amplifiers. The data are delivered to datalines. Then, the main sense amplifiers transfer 8-bit data to main datalines. For the write cycle, the write drivers feed two sets of 4-bit data into the selected bitlines.

4. Reference Circuit

In this design, the reference circuit utilizes a ferroelectric capacitor. It offers an advantage to track the memory cell properties. Its configuration and operational timing are shown in <Fig. 8>. It is constructed with dual PMOS gates, a set of

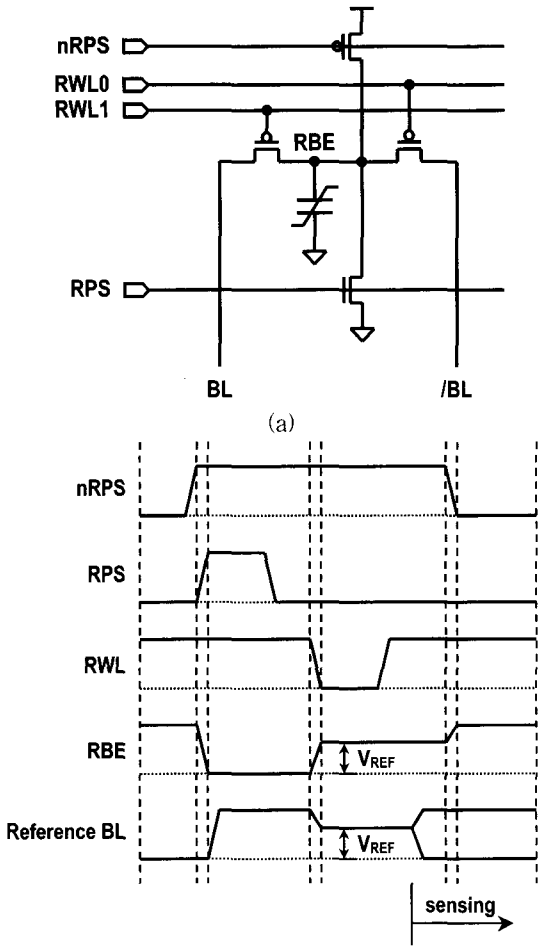



그림 8. Reference 회로: (a) 회로구조, (b) 타이밍
Fig. 8. Reference circuit: (a) circuit configuration, (b) timing.

pre-biasing PMOS and NMOS transistor and one ferroelectric capacitor. Initially, nRPS biases the bottom electrode of the reference capacitor (node RBE) to $V_{DD}$ level. It eliminates the relaxation component, which may result from a ferroelectric capacitor according to time without bias.[4] When accessed, nRPS goes high and the signal RPS makes the node RBE a ground level. When the reference wordline RWL is pulled down to low, the charges in bitline initially precharged to $V_{DD}$ are shared with the reference capacitor. The resulting reference bitline voltage becomes

$$V_{REF} = \frac{C_{BL}(V = V_{DD}) \cdot V_{DD}}{C_{BL}(V = V_{REF}) + C_{RNS}(V = V_{REF})} \quad (3)$$

where $C_{RNS}$ is the non-switching capacitance of reference capacitor. Because the reference capacitor is used in the high state characteristic curve, its size has been designed to be 1.7 times larger than that of the memory cell.

5. Bitline SA Driver

<Fig. 9(a)> shows the bitline SA driver which sets bitline data latches. <Fig. 9(b)> shows its timing diagram. Specially, this circuit needs a careful timing control to correctly amplify a small difference of bitline voltages. When the SAEN goes to high, the SAP begins its ramp-up to $V_{DD}$. If the ramp is too fast, noise will be coupled onto the bitlines, and the sensitivity of the sense amplifier will be reduced.

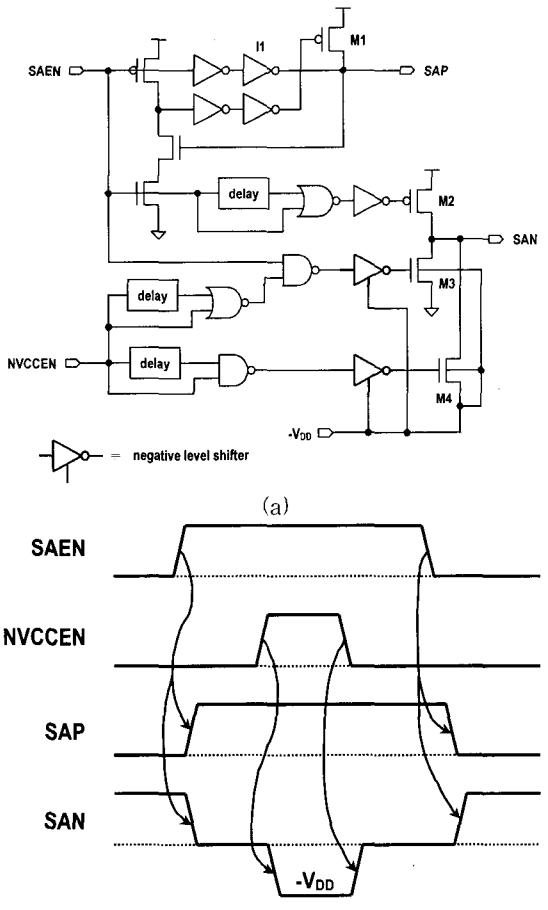



그림 9. 비트라인 센스 증폭기 구동기: (a) 회로, (b) 타이밍
Fig. 9. Bitline sense amplifier driver: (a) circuit configuration, (b) timing.

The initial slow ramp rate of SAP assists the separation of bitline signal. This is accomplished by first activating a small PMOS of the inverter I1. Once sufficient separation has occurred, SAN is pulled low to provide full-rail separation. Then, a large SAP driver M1 is then turned on. The ramp rate of SAP is accelerated. After the read operation is completed, an NVCCEN pulse sequentially turns M3 off and turns M4 on, then turns M4 off and turns M3 on. As a result, a $-V_{DD}$ negative pulse is supplied to SAN. This pulse is transferred into "0" data bitlines through selected bitline sense amplifiers. After finishing the restore operation, the falling of SAEN returns SAP to low. Then, SAN is brought to high to completely disconnect the sense amplifier from the bitlines.

6. Negative Charge Pump

As previously described, the proposed FRAM architecture requires two negative power voltages. First, the read/write operation needs $-V_{DD}$ pulse restore. Second, the wordline and ISO signal need their logic "low" level to be $-V_{PP}$.

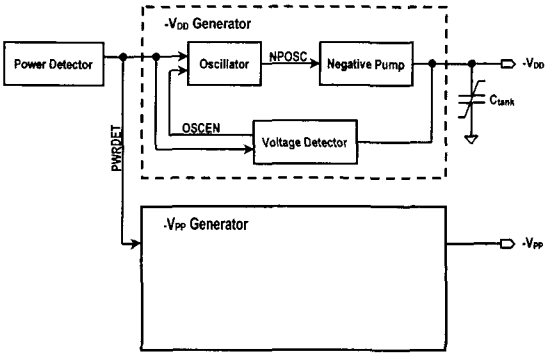



그림 10. Negative 전압생성기. $-V_{DD}$ 생성기와 $-V_{PP}$ 생성기는 동일한 회로구조를 갖고 있음

Fig. 10. Block diagram of negative voltage generator. Both of $-V_{DD}$ generator and $-V_{PP}$ generator have the same circuit configuration.

<Fig. 10> shows the block diagram of negative voltage generator. The circuit consists of oscillator, two-phase negative charge pump and voltage detector. Power detector initiates the operation of charge pump upon power-up. A negative voltage detector limits the pumping voltage to the target value.

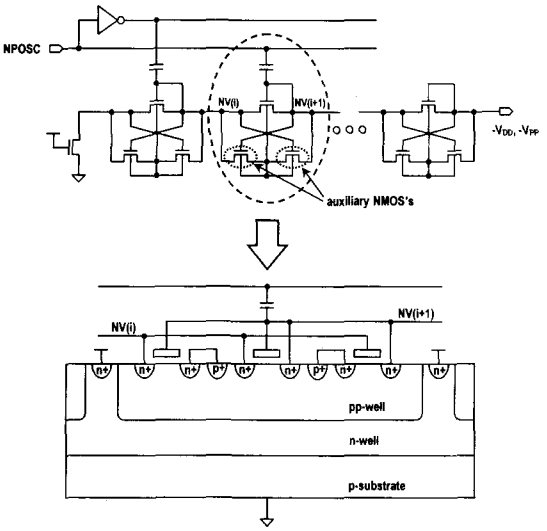



그림 11. 2상 negative 전압 charge 펌프

Fig. 11. Two-phase negative charge pump.

<Fig. 11> shows the schematic and cross-sectional view of the employed negative charge pump. Individual stages are operated by two-phase clock. To reduce the body effect on threshold voltage of the charge transfer transistor, the charge pump circuit is based on the controlled body voltage.[8] For each charge transfer block, two auxiliary NMOS's and one charge transfer NMOS share the body which is separated from the body of the other blocks. These two auxiliary NMOS's control the body bias to prevent the body from floating. By adjusting the body voltage, the back bias effect of threshold voltage is lessened so that it offers a high performance even in low supply voltage.

<Fig. 12> shows circuit simulations for the negative charge pumps, using 0.5-um 5-V CMOS process parameters with triple-well technology and pump capacitances of 10 pF at the condition of 85 ℃. In this simulation, the supply power voltage is ramping up with slew rate of 1-V/50-us. The power-on start signal (PWRDET) is triggered at 2.0 V. As shown in the figure, the $-V_{DD}$ and $-V_{PP}$

negative voltages are settled down to the target value in 6 us after starting the negative pumping. It is done before the supply voltage reaches the minimum operating voltage of 2.3 V. Therefore, no latency after power-up is needed for chip operation.

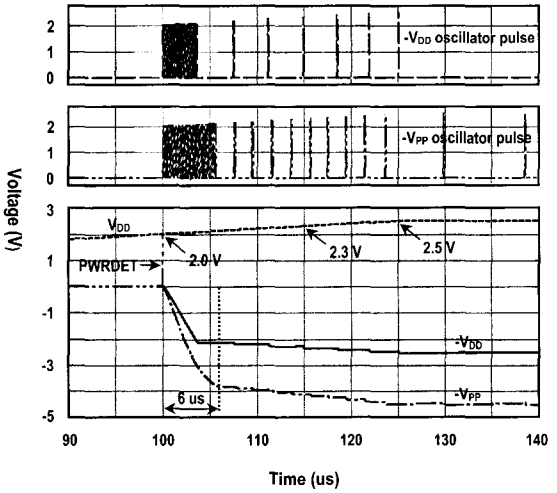



그림 12. Negative charge 펌프의 모의실험 파형 (T = 85 ℃

Fig. 12. Simulated waveforms of negative charge pump at T = 85 ℃.

One thing to be concerned is the stabilization of $-V_{DD}$ power voltage during chip operation. Specially, $-V_{DD}$ voltage control is important because it affects the amount of "0" data polarization. In order to be symmetrically polarized with data "1", the $-V_{DD}$ charge pump circuit needs to extract large current in a short time without any significant voltage drop. To meet the above special requirement, $-V_{DD}$ voltage is pooled in a large tank capacitance of about 1.6 nF. The capacitance is made by the high dielectric ferroelectric capacitor whose unit capacitance is 42 fF/um$^2$. It can be laid under signal interconnection bus without any area penalty. <Fig. 13> shows circuit simulations of two 200 ns cycles at $V_{DD}$ of 2.7 V, oscillation pulse period of 42 ns and temperature of -40 ℃. In the figure, a current of 43 mA peak is the current which a bitline SA driver in each 512-Kb block extracts from the accessed 4 columns with all data "0" during the negative pulse restore. As shown in the simulation, the $-V_{DD}$ charge pump with stabilizing capacitance can keep the $-V_{DD}$ level at a target value of -2.7 V with the maximum deviation of 150 mV. This small variation of $-V_{DD}$ power will not significantly affect the amount of "0" data polarization.

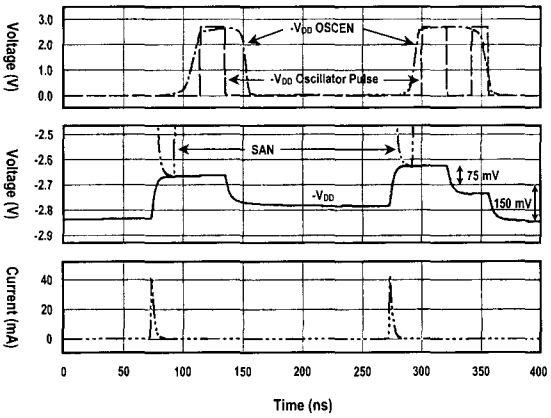



그림 13. 칩 동작 중 $-V_{DD}$ 전압 레벨

Fig. 13. Pumped $-V_{DD}$ voltage level during chip operation.

7. Data Refresh

One drawback of the proposed FRAM architecture is that it requires a cell data refresh operation. As shown in <Fig. 14>, the problem is caused by parasitic junction diode between n-well and the cell internal node. The n-well in the memory array is biased at $V_{DD}$, and the internal node of the memory cell is floating during the standby mode. Hence, due to junction leakage from the reverse-biased junction diode, the voltage level of the cell internal node will rise and finally reach $V_{DD}$. This voltage may destroy the stored data. To prevent this problem, a data refresh is carried out into the memory cell internal node. The refresh operation is done by simply driving the wordlines to $-V_{PP}$ and then to $V_{DD}$ with bitlines biased at 0 volt. When an internal self-refresh signal is activated, the refresh address counter selects individual wordlines in turn. This removes positive leakage voltage, and the memory cell internal node voltages are refreshed to 0 volt. Since this cycle is performed without the help of any

peripheral circuit resources such as sense amplifier, reference circuitry and bitline precharger, the refresh cycle time for each wordline supporting 1024 cells is 30 ns. Thus, a data refresh cycle time for 1-Mb array in <Fig. 5> is less than 16 us. In contrast to the normal read/write cycle, this refresh cycle can execute the massive-parallel operations.

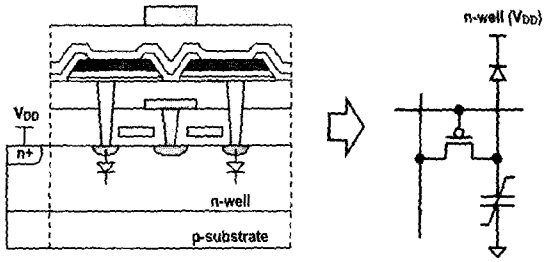



그림 14. N-well 과 셀 내부 노드 간의 기생 접합 diode

Fig. 14. Parasitic junction diode between n-well and cell internal node.

## V. Performance Estimation

<Fig. 15> shows the proposed chip architecture of the 4-Mb FRAM. It consists of eight 512-Kb blocks. All WL drivers are positioned on a single side of the 512-Kb block. Two 512-Kb blocks share column signal generators, composing a 1-Mb double unit. Peripheral circuits are located at the bottom, while two negative charge pump circuits are located at the center of left and right edge. The bonding pins are arranged in the top and bottom of left and right edge. The 8-bit datalines are split into two 4-bit groups inside of 1-Mb double unit. Each 1-Mb double unit is controlled by one of four block control logics arranged at the center of the chip.

In <Fig. 16>, a read operation is confirmed at $V_{DD}$ of 2.5 V and temperature of 25 ℃. The sensing voltage difference of 140 mV has been obtained. It is sufficient for the bitline latch sense amplifier's accurate operation. The access time is 85 ns. The rising and falling delay of negative restore pulse is about 25 ns. The chip can read out the stored data at a minimum cycle of 120 ns. The simulation shows the active current of 12 mA at this condition.

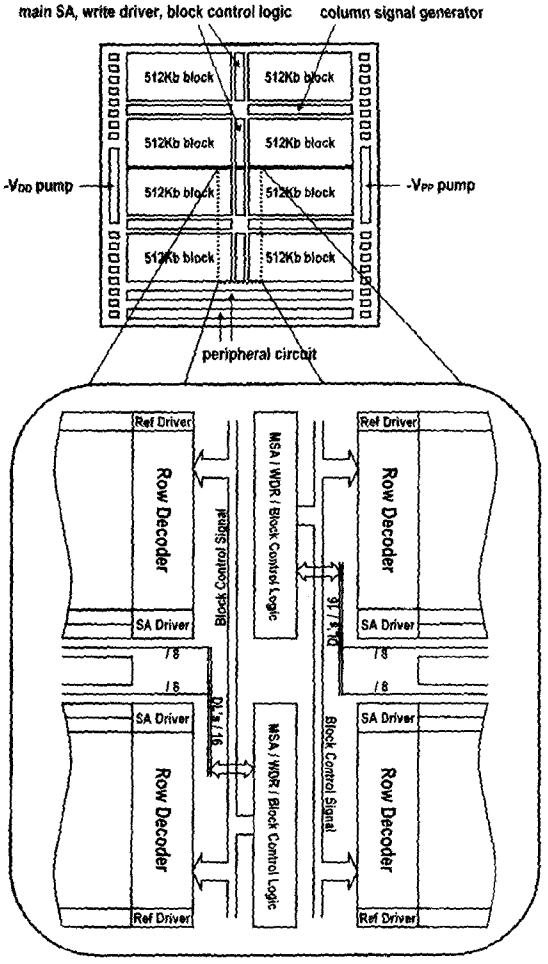



그림 15. 제안된 4-Mb FRAM architecture

Fig. 15. Proposed chip architecture of 4-Mb FRAM.

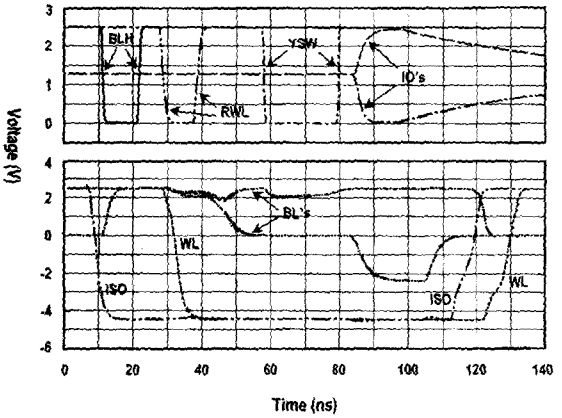



그림 16. 읽기 동작의 파형 ($V_{DD}$ = 2.5 V, T = 25 ℃

Fig. 16. Read cycle waveforms at $V_{DD}$ = 2.5 V and T = 25 ℃.

Another possible concern in the proposed FRAM architecture is the polarization disturbance due to cell plate bump. When the cells are accessed, a transient displacement current through the ferroelectric capacitors flows between the bitline and the common plate. This current may cause a voltage drop along the common plate so that it might destroy some amount of intended polarization of the particular cell capacitors.[7] As shown in <Fig. 17>, the voltage bump occurs when the cell data are read out to the bitlines, when the sense amplifiers amplifies the signal voltage, when the negative-pulse restores the data, and when the bitlines are brought to the ground voltage. The resistance of the common plate (top electrode composed of $Ir/IrO_2$) is 15 Ω/O However, the plates in GPPG cell array are electrically directly connected to the $V_{SS}$ power line. Furthermore, the number of accessed bitlines per wordline is very small (4 bitline pairs in each 512-Kb block). As the result, the plate voltage bump is insignificant, less than 15 mV even at 2.7 V, -40 (℃. No capacitors will suffer a severe polarization disturb in the GPPG cell architecture.

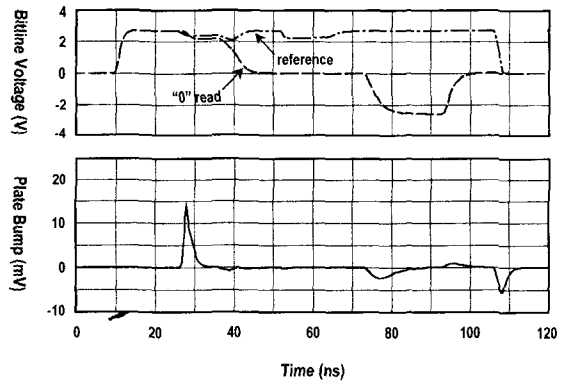



그림 17. 칩 동작 중 plate bump 현상 ($V_{DD}$ = 2.7 V, T = -40 ℃

Fig. 17. Plate bump during chip operation. ($V_{DD}$ = 2.7 V, T = -40 ℃.

## VI. Conclusion

To overcome limitations due to current FRAM cell-plate schemes, a new ferroelectric design concept utilizing grounded-plate PMOS-gate (GPPG) cell has been proposed, and its feasibility has been examined with 4-Mb FRAM design. In this study, design rule and process parameters of 0.5-um ferroelectric storage cell integrated CMOS with triple-well, 1-polycide, 2-metal have been used. Each GPPG memory cell consists of a PMOS access transistor and a ferroelectric data storage capacitor. Its plate is grounded. A unique feature of the proposed FRAM architecture is that it doesn't require the plate decoding, so that it can greatly improve the memory array efficiency. In addition, differently from other reported common-plate cells, this scheme can supply a sufficient voltage of $V_{DD}$ to the ferroelectric capacitor during detecting and storing the polarization on the cell. Thus, there is no restriction on low voltage operation. Furthermore, the proposed architecture can minimize the memory array power by selecting only needed 8-bit data. This proposed design technique can be a promising candidate in future high density ferroelectric memory development.

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