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# Preparation and Electronic Defect Characteristics of Pentacene Organic Field Effect Transistors†

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**Abstract :** Organic materials have considerable attention as active semiconductors for device applications such as thin-film transistors (TFTs) and diodes. Pentacene is a *p*-type organic semiconducting material investigated for TFTs. In this paper, we reported the morphological and electrical characteristics of pentacene TFT films. The pentacene transistors showed the mobility of 0.8 $cm^2/Vs$ and the grains larger than 1 $\mu m$. Deep-level transient spectroscopy (DLTS) measurements were carried out on metal/insulator/organic semiconductor structure devices that had a depletion region at the insulator/organic-semiconductor interface. The duration of the capacitance transient in DLTS signals was several ten of seconds in the pentacene, which was longer than that of inorganic semiconductors such as Si. Based on the DLTS characteristics, the energy levels of hole and electron traps for the pentacene films were approximately 0.24, 1.08, and 0.31 eV above $E_v$, and 0.69 eV below $E_c$.

*Keywords* : pentacene, organic transistor, DLTS, mobility, defect.

## Introduction

For the last several years, the organic electro-optics and electronics have attracted considerable attention due to the remarkable progress in organic light emitting devices (OELDs), organic thin film transistors (OTFTs), photovoltaic cells, and photodetectors.[1-6] In particular, the characteristics and the performance of the pentacene field-effect transistors (FETs) have made such devices viable for applications requiring large area coverage, mechanical flexibility, and low overall cost.[2,3] However, despite the great potential, their performance has been limited by the poor material qualities originated from high rate of defects and trap densities in organic materials.[7]

Deep-level transient spectroscopy (DLTS) technique has been used to measure the energy level, concentration, and capture cross section of defects and to describe electrically the active localized states formed within the built-in field region of inorganic and organic semiconductors.[8] This study reports on the characteristics of the deep defects in the pentacene film by using the DLTS measurement. The pentacene is a well-known aromatic molecule and has shown the field-effect mobilities as large as 1.5 $cm^2/Vs$ in earlier works by Lin *et al.*[9] This study also argues that the characteristics of pentacene TFTs can be improved by using a self-organizing material between $SiO_2$-gate dielectrics and the pentacene-active materials. Since not only the crystallinity but also the interface defects and traps between the pentacene and gate dielectrics were well known to be significant in the operation of TFT devices, we investigated the concentration and the energy level of the defects in the pentacene film transistors.

## Experimental

**Preparation of Pentacene Films.** Pentacene was purchased from Aldrich Chemical Co. and was purified using vacuum sublimation at $10^{-3}$ Torr or lower. The pentacene thin films were deposited *in situ* on $SiO_2$/Si substrates by using a conventional thermal evaporator at the pressure below $10^{-6}$ Torr. The substrate - a heavily doped, thermally oxidized silicon wafer - was treated with hexamethyldisilazane (HMDS) as the self-organizing material, which had been used to improve the quality of the organic/dielectric interface,[10] and was maintained at 60 °C during the depositions. The deposition rate was about 1 Å/s. The thickness of the films was in the range of 50-400 nm. The surface morphology and chemical compositions of the films were examined by an atomic force microscopy (AFM) and an x-ray photoelectron spectroscopy (XPS), respectively.

**Measurements of Electric Properties.** The organic TFT structure that we used for this study is shown in Figure 1.

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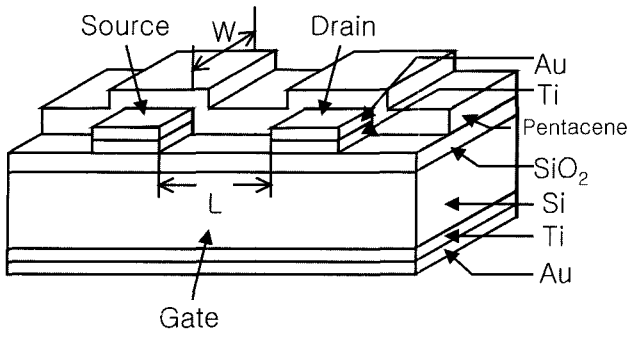


**Figure 1.** Schematic organic-TFT structure of the pentacene film deposited on Si substrate. The heavily doped (< 5 Ωcm), *n*-type silicon substrate acted as the gate, and thermal oxide layer acted as the gate dielectrics in organic TFTs.

The heavily doped, *n*-type silicon substrate acted as the gate, and thermal oxide layer acted as the gate dielectrics in organic TFTs. The characterization of TFTs was conducted at room temperature using a Hewlett-Packard 4145B semiconductor parameter analyzer at various gate voltages. To measure the capacitance properties of a metal/insulator/organic semiconductor (MIS) structure device, Au/Cr film was deposited as an electrode (area: 3.14 $mm^2$) on the pentacene film by dc sputtering through a shadow mask. The electronic charge concentrations and deep-level defects were investigated by DLTS.

## Results and Discussion

We evaluated the nature of the channel conductivity with zero gate bias. This result indicates that the pentacene is doped (*p*-type) in the as-deposited condition, similar to the results of Jackson *et al.*[2] Figure 2(a) shows the typical plot of drain current $I_{DS}$ versus drain voltage $V_D$ at various gate voltages $V_G$ for the pentacene TFT with channel length of 10 μm and width of 50 μm, and the gate dielectric thickness of 300 nm. When the gate electrode was biased negatively with respect to the grounded source electrode, pentacene TFTs operated in the accumulation mode and the accumulated charges were holes. The field-effect mobility, which was measured in the saturation regime ($V_D > V_G$) due to the pinch-off of the accumulation layer,[11] was approximately 0.8 $cm^2$/Vs. The log($I_{DS}$) versus $V_G$ characteristics at the $V_D$ of -100 V is shown in inset of Figure 2(a). The on/off ratios of approximately $10^5$ were achieved between $I_{DS}$ currents at $V_G$ = -100 V and $V_G$ = 0 V measured at a certain $V_D$ in the saturation regime.

An AFM image of the pentacene film with a thickness of 50 nm deposited onto an HMDS-treated $SiO_2$/Si substrate is shown in Figure 2(b). The image was observed over the area of 7 μm × 7 μm with a noncontact mode, and the scan frequency was 0.5 Hz. The pentacene film contained dendritic

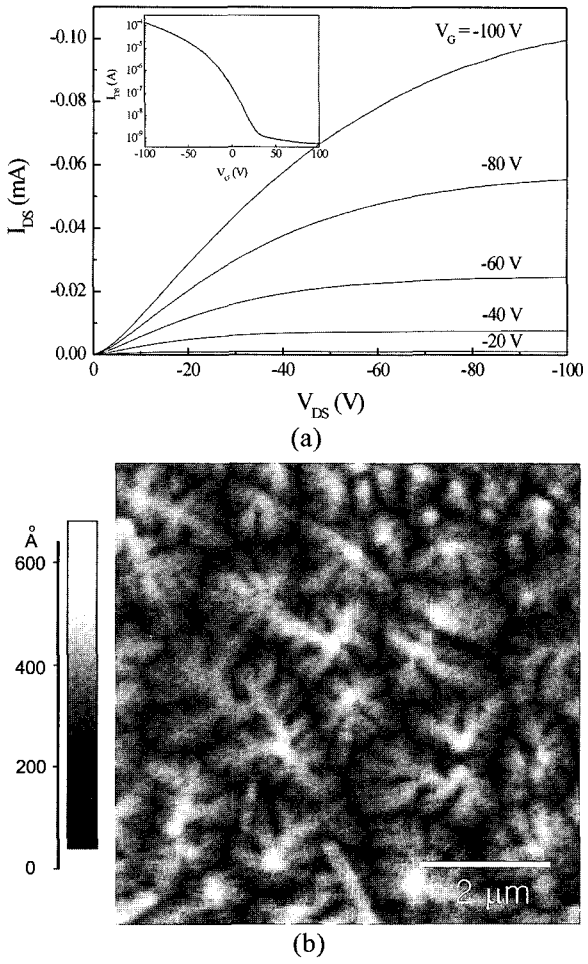


**Figure 2.** (a) $I_{DS}$-$V_D$ characteristics at various gate voltages $V_G$ for a pentacene TFT fabricated with channel length of 10 μm and width of 50 μm. The inset is the log($I_{DS}$)-$V_G$ characteristics at the $V_D$ of -100 V. (b) AFM image of the pentacene film with a thickness of 50 nm.

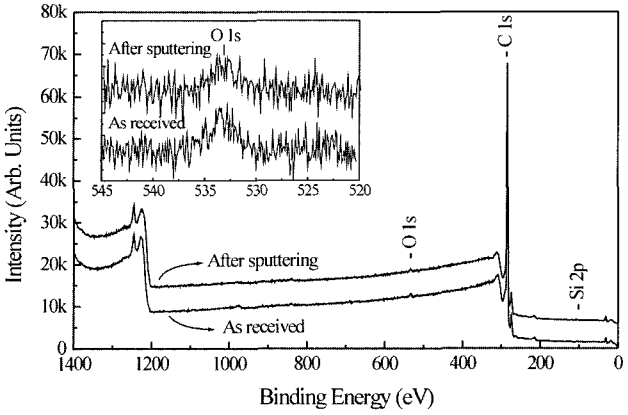


**Figure 3.** XPS spectra of the pentacene film with a thickness of 50 nm. The spectra were taken as received and after 1 min *in situ* Ar sputter cleaning of the sample surface.

grains. The average grain size, root-mean-square surface-roughness, and peak-to-valley roughness were approximately 2 $\mu$m, 51 Å, and 238 Å, respectively. The film roughness did not increase significantly for the films thicker than 50 nm.[2,10]

The chemical compositions of the pentacene films were investigated by an XPS. Figure 3 shows the XPS spectra of the pentacene film with a thickness of 50 nm. The spectra were taken as received and after 1 min *in situ* Ar-sputter cleaning of the sample surface. The high resolution XPS measurements of O(1s) electron binding energy for the sample are shown in the inset of Figure 3. In X-ray photoelectron spectra, the oxygen and silicon impurities were detected on the surface. After Ar-sputter cleaning, the Si ion disappeared and the ratio of the oxygen ion decreased to be approximately 1%.

To investigate the interface trap characteristics of pentacene thin films, we employed the DLTS technique developed by Lang.[12] Figure 4 illustrates the sequences of the applied electrical pulse (Figure 4(a)), the consequent capacitance transient behavior corresponding to the electrical pulse shape (Figure 4(b)) and the energy band bendings happened in the MIS capacitor (Figures 4(c)-(e)). In the steady state ($t < -T$), a constant bias voltage $V_a$ is initially set to the gate electrode of the MIS capacitor and the interface of the semiconductor closed to the insulator is kept in depletion with the width $W_a$ (steady-state; Figure 4(c)). Then at $t = -T$, a negative pulse $\delta V$ (= $V_b$ - $V_a$) is applied to the gate electrode of the MIS in superposition to a constant bias voltage $V_a$ so that the interface of the semiconductor is driven into accumulation of weak depletion (capture process; Figure 4(d)). This pulse makes the interface states located below $E_a$ be filled with holes and, if the pulse duration is large enough, leads the Fermi level to its equilibrium value $E_b$. By quickly returning the bias voltage to its constant value $V_a$ after making the interface traps located below the Fermi level (in Figure 4(c)) be filled up with holes ($t > 0$), the holes are emitted from the filled traps above the Fermi level (in Figure 4(d)) with characteristic emission rates that depend exponentially on temperature (emission process; Figure 4(e)).[13] The variation of capacitance $C(t)$ is represented by the change of depletion layer depth $W(t)$. In the depletion approximation it be-comes[12,13]

$$C(t) = \left[\frac{1}{C_i} + \frac{W(t)}{\varepsilon_s}\right]^{-1},$$

where $C_i$ is the insulator capacitance per unit area, $\varepsilon_s$ the dielectric constant of the organic semiconductor.

In this study, DLTS signals were measured in the temperature range from 50 to 320 K. To fill traps, the initial voltage of -25 V was applied toward heavily doped silicon for 0.5 s. Then, the specimen was biased to 25 V and the transient capacitance was recorded. The emission rate window $e_p^{-1}$ ranged from 0.12 to 12 Hz. Because the temporal length of the transient capacitance in organic materials is generally larger than that in inorganic semiconductors,[14] a low $e_p^{-1}$

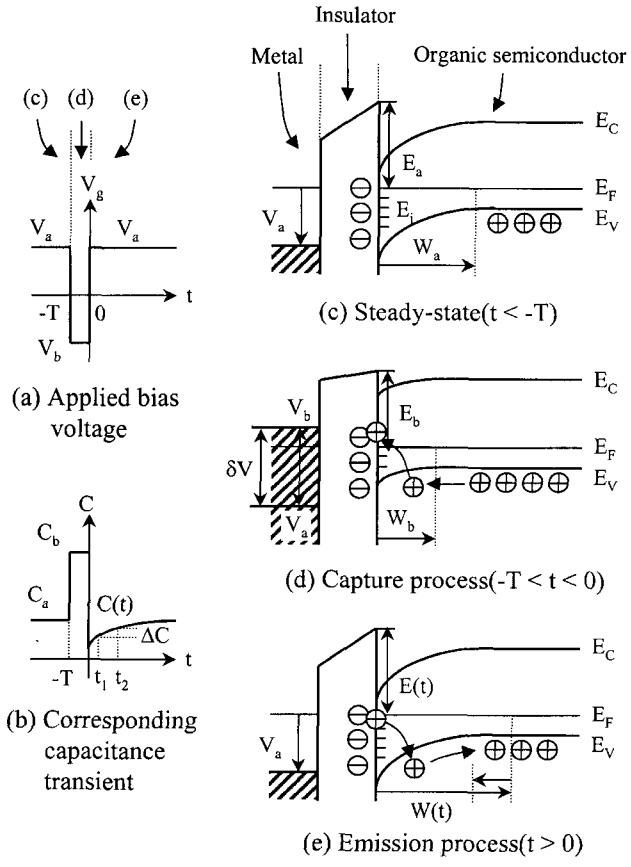


**Figure 4.** (a) Sequences of the applied bais voltage, (b) the consequent capacitance transient behavior, and the energy band bendings of a MIS capacitor in (c) steady-state, (d) capture, and (e) emission processes.

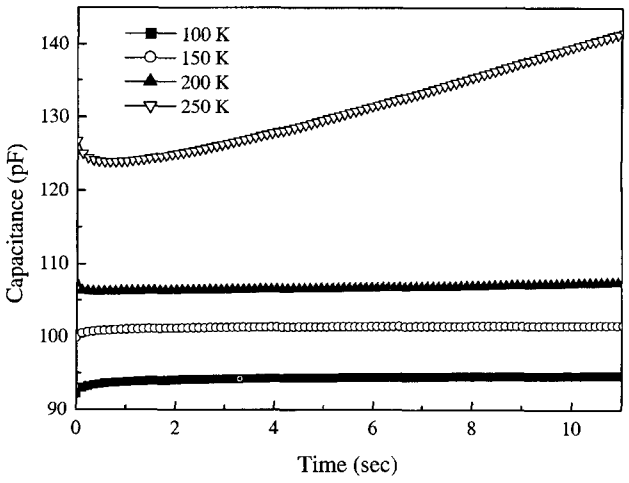


**Figure 5.** Typical plots of transient capacitance $C(t)$ versus time $t$ at 100, 150, 200, and 250 K.

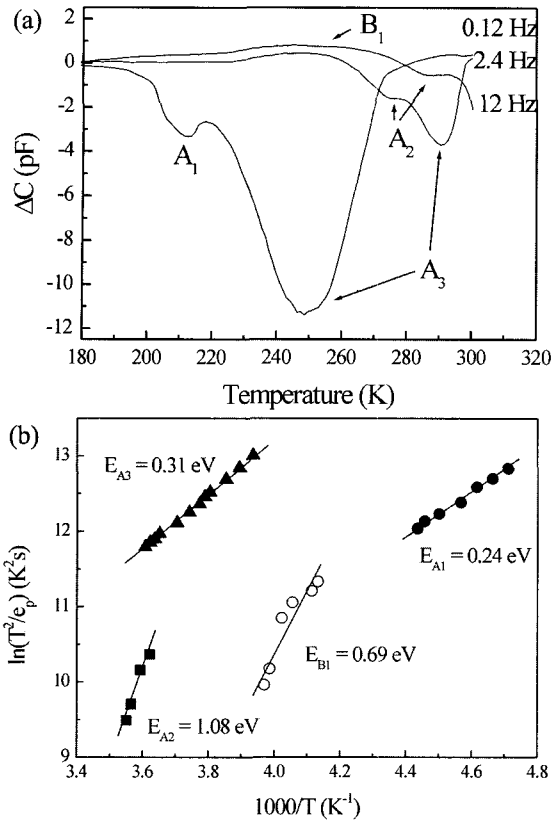


**Figure 6.** (a) DLTS spectra of the pentacene MIS capacitor. The emission rate window $e_p^{-1}$ ranged from 0.12 to 12 Hz (b) Arrhenius plots of $\ln(T^2/e_p)$ versus $1000/T$, determined from the DLTS spectra.

was introduced in the DLTS measurement. Figure 5 shows the typical plots of transient capacitance $C(t)$ versus time $t$ at 100, 150, 200, and 250 K. Figures 6(a) depicts the DLTS spectra for the case of pentacene MIS capacitors. Four completely different trap centers (one positive and three negative peaks, labeled $B_1$, $A_1$, $A_2$, and $A_3$ respectively for convenience) were found in the temperature range of 180 to 300 K. The positive and negative directions of the peaks indicate respectively the possible emissions from minority and majority carrier traps. These traps can be caused by the presence of not only chemical impurities but also grain boundaries. Figure 6(b) shows the Arrhenius plot of $\ln(T^2/e_p)$ vs $1000/T$ for negative and positive DLTS peaks. The activation energies of $A_1$, $A_2$, $A_3$, and $B_1$ were labeled $E_{A1}$, $E_{A2}$, $E_{A3}$, and $E_{B1}$, respectively. The energy levels were obtained from the slope of the least-square fit lines. The values of $E_{A1}$, $E_{A2}$, $E_{A3}$, and $E_{B1}$ in the pentacene MIS capacitor evaluated by the fitting were approximately 0.24, 1.08, 0.31, and 0.69 eV, respectively. The trap densities have been determined to be[15]

$$N_t = \frac{2n_h \Delta C}{C_o},$$

where $n_h$ is the hole concentration in shallow acceptor levels, $\Delta C$ the transient capacitance change due to a saturating injection pulse, and $C_o$ the specimen steady-state capacitance. The densities of deep-level traps -$A_1$, $A_2$, $A_3$, and $B_1$ - evaluated by using this equation and employing the hole concentration of $1.7\times 10^{16}$ cm$^{-3}$,[14] were approximately $4.2\times 10^{15}$, $9.6\times 10^{14}$, $6.5\times 10^{15}$, and $2.6\times 10^{14}$ cm$^{-3}$, respectively. From the XPS data, there may be the chemical impurities containing oxygen such as anthraquinone and pentacenequinone in the pentacene film. Vannikov and other researchers reported that the depth of traps formed by anthraquinone in anthracene was 0.6 eV below $E_c$.[16] These impurities, as well as dislocation contents and grain boundaries, are strong candidates for trapping levels in pentacene films.[17]

## Conclusions

In summary, we used the pentacene as the active semiconducting material in thin-film transistors. The dendritic grains in the pentacene film were observed by an AFM, and the average grain size was approximately 2 $\mu$m. The field-effect mobility of the pentacene measured in the saturation regime was approximately 0.8 cm$^2$/Vs. In the XPS data of the Ar-sputtered pentacene film, the oxygen ion of approximately 1% was detected as the chemical impurity. We investigated the electronic charge concentrations and the interface trap characteristics of the pentacene thin film using by DLTS measurements. Based on the DLTS of the pentacene MIS capacitors, the concentrations and the energy levels of the hole and electron traps were approximately 0.24, 1.08, and 0.31 eV above $E_v$, and 0.69 eV below $E_c$.

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