A New EEPROM with Side Floating Gates Having Different Work Function from Control Gate

Youngjoon Ahn, Sangyeon Han, Hoon Kim, Jongho Lee[1], and Hyungcheol Shin

Abstract - **A new flash EEPROM device with p^+ poly-Si control gate and n^+ poly-Si floating side gate was fabricated and characterized. The n^+ poly-Si gate is formed on both sides of the p^+ poly-Si gate, and controls the underneath channel conductivity depending on the number of electron in it. The cell was programmed by hot-carrier-injection at the drain extension, and erased by direct tunneling. The proposed EEPROM cell can be scaled down to 50 nm or less. Shown were measured programming and erasing characteristics. The channel resistance with the write operation was increased by at least 3 times.**

Index Terms— **EEPROM, flash memory, MDSFET, hot carrier injection, direct tunneling.**

I. Introduction

A flash EEPROM has been widely applied to electronic equipments in the areas of computer, multimedia, and telecommunication [1]. Those advanced electronic equipments strongly need high density and high performance flash memories. However, now conventional flash memory devices are faced with scaling-down problem because they have very poor short channel effect (SCE) due to non-scalable gate oxide (8 nm). To overcome the challenge, several approaches have been reported [2]-[4]. But much work is still needed to obtain reasonable candidate for the future flash memory cells.

Therefore, in this paper, we propose a new flash EEPROM structure which has p^+ main control gate and n^+ side gates at both sides of the control gate as storage nodes. The proposed structure can be scaled-down to sub-50 nm regime because the device has the electrically induced S/D extensions under the floating storage side gates, and therefore its short channel effect can be suppressed. Also fabrication process is compatible with a standard CMOS process flow.

II. Device Structure

Fig.1 shows a schematic cross-section of the proposed flash EEPROM, which has a p^+ poly-Si main gate acting as the Control Gate (CG) and n^+ poly-Si side gate acting as the Storage Gate (SG). The potential on the SG is determined by capacitive coupling between the CG and the source/drain. If the potential on the SG is larger than the "effective" threshold voltage of the side-gate device, an inversion layer is induced under the SG. Since very thin extended S/D regions are induced electrically, the ultra shallow S/D junction suppresses the SCE. The threshold voltage (V_T) of side-gate NMOSFET is very low (normally turn-on) due to the n^+ poly-Si gate and low channel doping, so that the electron concentration induced under the SG is high during turn-on. Therefore, the resistance of electrically induced S/D regions becomes low as the side-channel doping decreases. The V_T of main gate NMOSFET is around 1 V because of the work function of the p^+ poly-Si main gate. Therefore, we can lower the channel doping, which leads to high

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channel mobility and low V_T fluctuation due to random dopant effect [5].

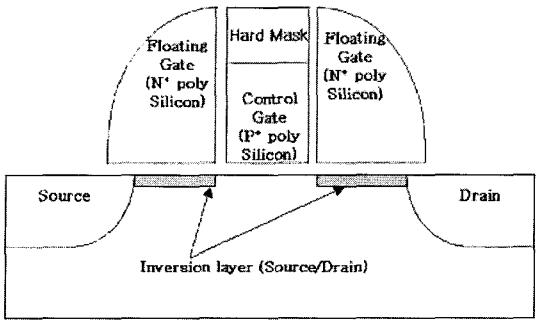


Fig. 1 A schematic cross-section of the proposed EEPROM.

The key process steps are as follows. After LOCOS process for device isolation, 3 nm gate oxide was grown in dry-O_2 ambient at 800 °C for 9 min. Poly-Si is deposited and doped by B^+ ion implantation for the CG, then Tetraethyl orthosilicate (TEOS) oxide hard mask was formed by 50 nm E-beam lithography and Reactive Ion Etch (RIE). After defining the CG, ultra thin ECR N_2O radical oxidation was done at 400 °C. A layer of poly-Si (25 nm) for n^+ side-gate was deposited by LPCVD and doped by 45° tilled As implantation. Indium and arsenic implantation were performed to form halo and shallow S/D regions, respectively. At this point, thin oxide spacer and selective epi, and silicide process could be used to reduce parasitic S/D resistance. However, in our mix-and-match device fabrication, extra deep source/drain implantation after oxide spacer formation was done to reduce the parasitic S/D resistance. After deep S/D implantation, implanted dopants were activated using RTA at 1000 °C for 6 sec.

III. Principle of Operation

The write operation of the proposed flash EEPROM is shown in Fig. 2. The write operation of the flash EEPROM is achieved by drain-side-injection of channel hot electron from the electrically induced drain extension to the SG. To program a cell, the CG is raised to 2.5 V, the drain is raised to 4.5 V, and the source and the substrate are connected to a ground voltage. Then, electrons flow from the source to the drain, and the electron flow in this region generates so-called hot electrons that are injected into the SG from the electrically induced drain extension. The SG is negatively charged, and the potential of the SG is lowered, and fewer electrons are induced under the SG. As a result, the resistance of the electrically induced drain-side-inversion layer under the SG increases, resulting in a decrease of the drain current.

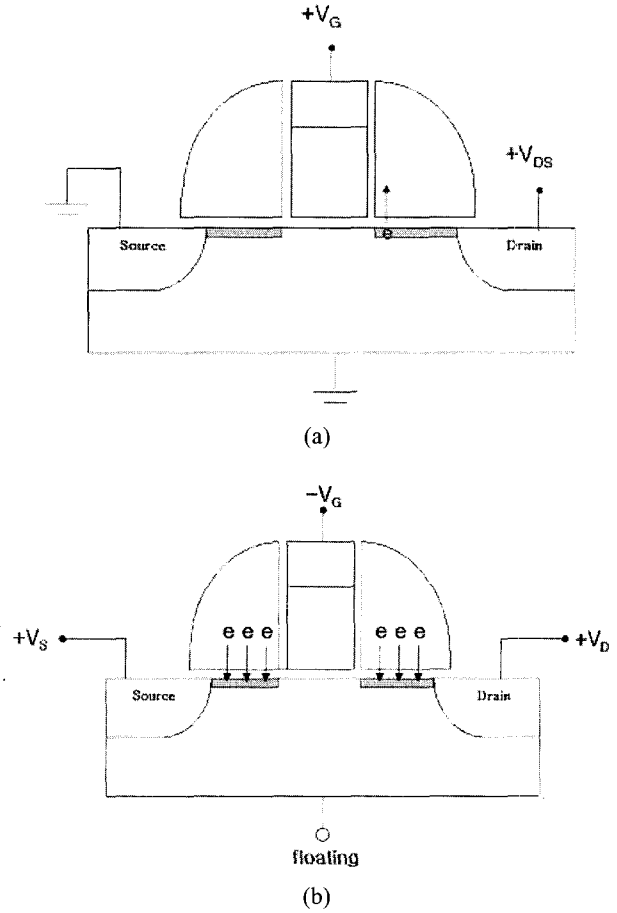


Fig. 2 Write/erase bias condition. (a) and (b) show the electron movement with write operation (a) and erase operation (b), respectively.

The erasing operation is achieved by Fowler-Nordheim tunneling of electrons from the SG to the Si substrate under the SG. To erase a cell, a negative voltage is applied to the CG, and high positive voltages are applied to the drain and the source while keeping the substrate floating. Electrons in the SG tunnel into the p-type substrate. Then the SG is discharged, and the potential of the SG is raised to the initial state. As a result, the resistance of the electrically induced drain-side-inversion layer under the SG decreases, resulting in an increase of the drain current.

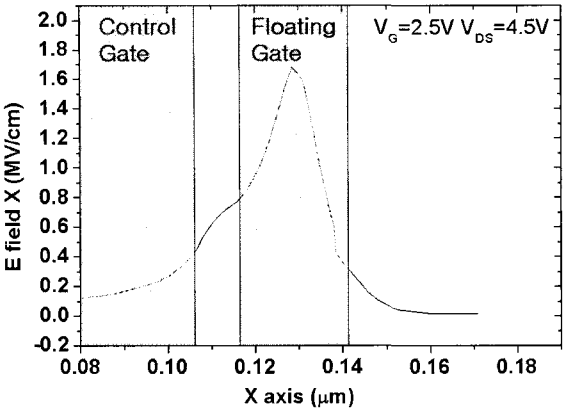
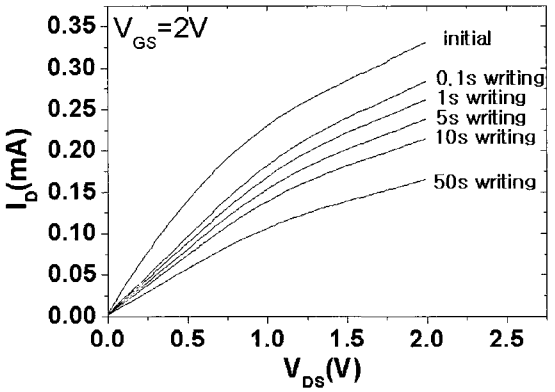
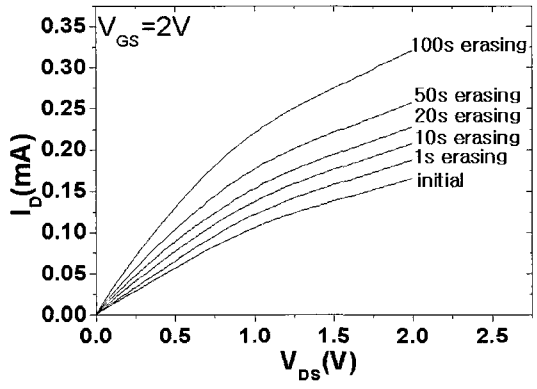


Fig. 3 imulated horizontal electric field.



(a)



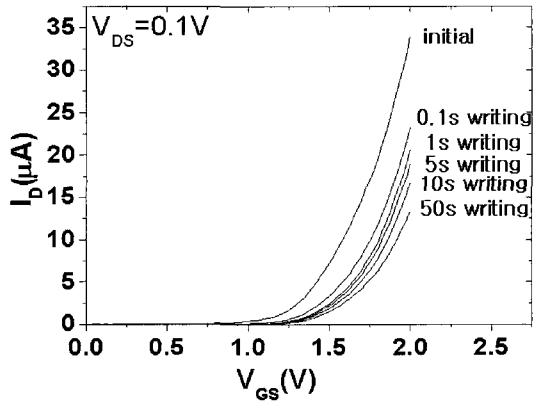
(b)

Fig. 4 I_D-V_{DS} characteristics with write/erase operation. Figs. (a) and (b) show I_D-V_{DS} characteristics with writing and erasing, respectively.

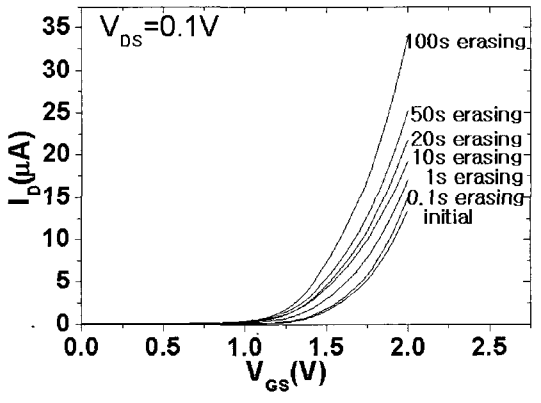
IV. Results and Discussion

Fig. 3 shows simulated horizontal electric field profile at the poly-Si/SiO_2 interface of proposed structure. The result was obtained by using ATLAS device simulator [6]. The CG and drain biases were given to 2.5 V and 4.5 V, respectively. Others were set to a ground voltage. In Fig. 3 the peak field appears under the drain-side-SG. This result shows the hot electron injection occurs under the drain-side-SG.

Fig. 4 (a) shows I_D-V_{DS} characteristics of the EEPROM with different programming times. The programming is performed by hot carrier injection by applying 2.5 V and 4.5 V to the CG and the drain, respectively. The drain current decreases as the programming time increases. Fig. 4 (b) shows I_D-V_{DS} characteristics of the EEPROM with different erasing times. The erasing is done by Fowler-Nordheim tunneling by applying –2 V, 6 V and 6 V to the CG, the source and the drain, respectively. The drain current increases by the decreases of the channel resistance with increasing erasing time.



(a)

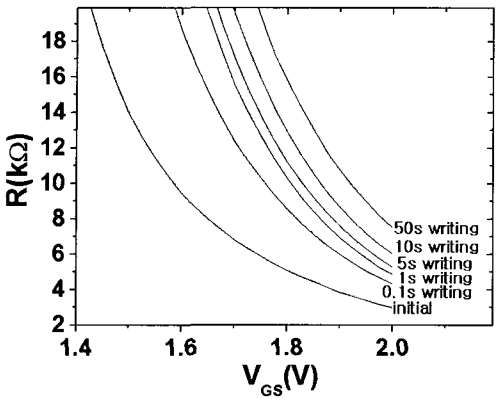


(b)

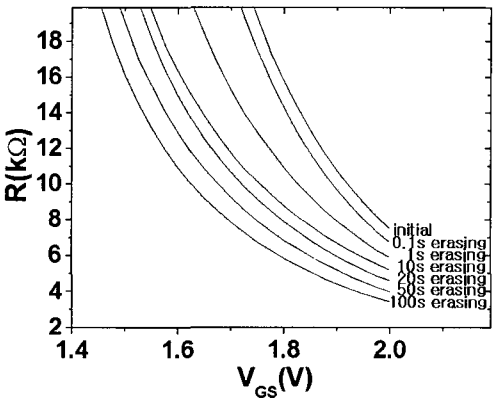
Fig. 5 I_D-V_{GS} characteristics with write(a)/erase(b) operation.

Fig. 5 (a) shows I_D-V_{GS} characteristics with different

programming time. After programming, the resistance of the electrically induced drain-side-inversion layer under the SG increases, and thus I_D decreases. Fig. (b) shows the increase of I_D with the increase of the erasing time.



(a)



(b)

Fig. 6 Channel resistance characteristics with write(a)/ erase(b) operation.

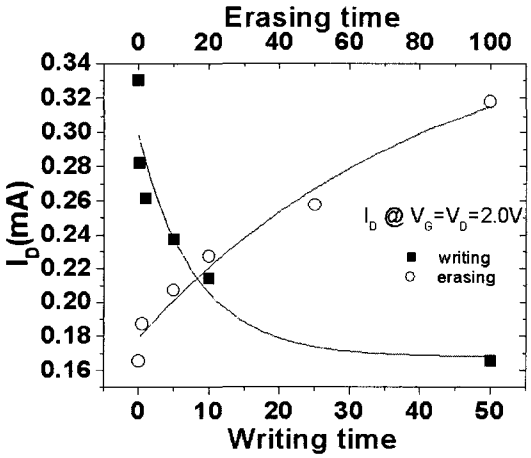
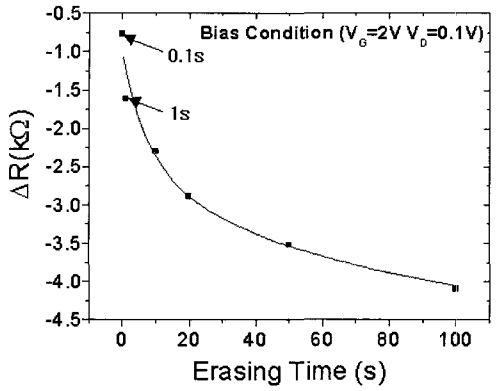
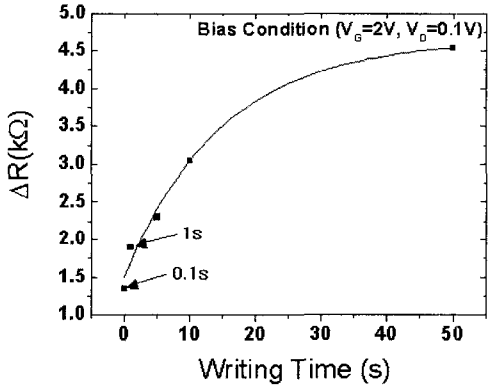


Fig. 7 I_D versus writing and erasing times. Writing bias conditions are V_{GS} = 2.5 V, V_{DS} = 4.5 V. Erasing bias conditions are V_G = - 2 V, V_D = V_S = 6V.

Fig. 6 shows channel resistance characteristics with write/erase operation. The resistance versus the gate bias as a parameter of writing time is shown in Fig. 6(a). The resistance increases as the writing time increases. Fig. 6(b). shows the resistance of the electrically induced drain extension for different erasing times.



(a)



(b)

Fig. 8 Resistance change with erasing(a)/writing(b) time.

Figs. 7 and 8 show memory characteristics of a proposed EEPROM with programming/erasing times. Fig. 7 shows the change of the drain current with writing time after applying V_{GS}=V_{DS}=2 V. After 50 s programming, the drain current drops from 0.33 mA to 0.17mA. Erasing characteristics with time are also shown after applying biases for the erasing. Fig. 8 shows the resistance change (ΔR) of the electrically induced drain extension with programming time after applying V_{GS}=2.0 V, V_{DS}=0.1 V. After 50 s programming, the resistance increases by 3 times (4.5 kΩ). The ΔR with the erasing time is also shown in Fig. (b). Here, the writing time is relatively long, and the device structure

needs to be optimized. From the SG memory structure, we designed SONOS memory device.

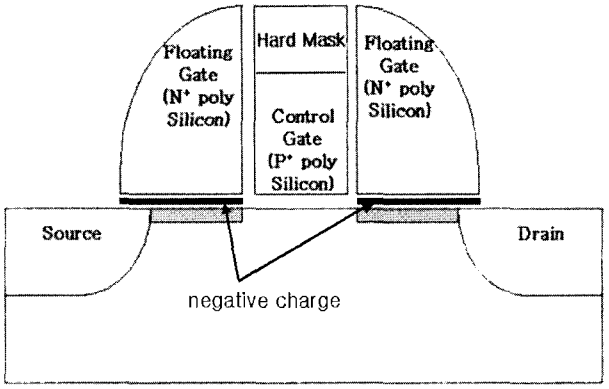


Fig. 9 Simulated device structure.

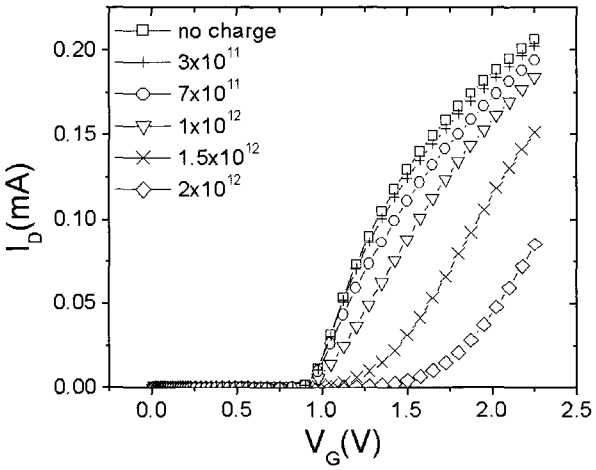


Fig. 10 I_D-V_{GS} characteristics with programming charge density.

In Fig. 9, shown is SG SONOS memory structure that has a layer of nitride for charge storage at 2 nm position from the Si surface. The nitride layer has many traps which can store charges. Total equivalent oxide thickness under the SG is 7 nm. The SG SONOS memory device is considered briefly as a possible memory structure using the SG structure.

Fig. 10 shows simulated I_D-V_{GS} characteristics of SG SONOS memory device with different programming charge densities. Simulated device structure is shown in Fig. 9. The simulation was performed with negative charge (electron) at interface between the SG and underneath tunneling oxide. For the negative oxide charge density less than about 1×10^{12} coul/cm^2, V_T shift was not observed because the V_T of main gate device large (~1V). Actually, by the programming charge, the V_T of the SG device was increased to a value less than 1V, so the channel resistance of the SF was increased, resulting in the decrease of the drain current. The V_T shift in the simulation data was clear for a given charge density larger than 1×10^{12} coul/cm^2. A charge density of 2×10^{12} coul/cm^2 shifts the V_T by 1.1V which is reasonable in memory operation.

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V. CONCLUSIONS

A Flash EEPROM with p^+ main gate and n^+ side gates has been fabricated and characterized. The cell is programmed by hot-carrier-injection from the electrically induced drain-side-inversion layer to the storage gate and erased by Fowler-Nordheim tunneling. The proposed EEPROM structure has very good device scalability and compatibility with conventional CMOS process flow. The channel resistance under the storage gates was changed by at least 3 times by programming. Further study on the flash memory structure is needed to optimize writing, erasing, and endurance characteristics.

We think that the proposed structure can be a candidate for future high-density flash memory.

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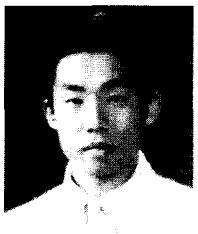

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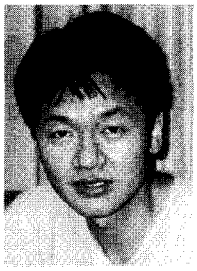

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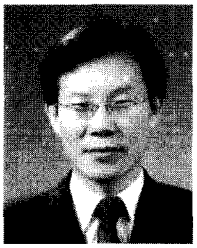

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