# Aspects of Hard Breakdown Characteristics in a 2.2-nm-thick $SiO_2$ Film

**Kenji Komiya and Yasuhisa Omura**

*Abstract* - **This paper mainly discusses the hard breakdown of 2.2-nm-thick $SiO_2$ films. It is shown that the hard breakdown event of a 2.2-nm-thick $SiO_2$ film greatly depends on the applied electric field. It is strongly suggested that the local weak spots created by applying a low initial stress to a 2.2-nm-thick $SiO_2$ film resist the onset of hard breakdown. In other words, it is anticipated that the stored electrostatic energy is fast dissipated by trap-assisted tunneling in 2.2-nm-thick $SiO_2$ film. Consequently, it is strongly suggested that 2.2-nm-thick $SiO_2$ films are intrinsically quite robust.**

*Index Terms* — **silicon oxide, hard breakdown, stress-induced leakage current, immunity**

## I. INTRODUCTION

The gate oxide thickness of metal-oxide-semiconductor (MOS) devices is being reduced step by step to match the reductions in integrated circuit scale [1]. The minimum gate oxide thickness is limited by the maximum allowable leakage current and device reliability. It is quite important to understand the degradation mechanisms of ultra-thin gate oxide films since we must design robust MOS devices [2].

For oxide films thicker than 3 nm, it is known that the time-to-dielectric-breakdown depends on electric field applied to the film. Degradation mechanisms have been classified into analog-mode soft breakdown, digital-mode soft breakdown, and hard breakdown (HBD)[3]. Weibull plots are widely used to assess thin-oxide reliability physics since they well integrate cumulative degradation data from many samples. Recent reports suggest that Weibull plots can be made in some cases for oxide films thinner than 2 nm, and that only HBD will be observed in most cases [4].

This paper compares HBD events in constant-voltage stressed 2.2-nm-thick $SiO_2$ films formed by various techniques. Background physics of the HBD events are also discussed to interpret phenomena observed.

## II. DEVICE FABRICATION

To examine hard breakdown mechanisms, we fabricated MOS capacitors on n-Si (001) substrates. 2.2-nm-thick oxide films were formed on bare silicon by the rapid thermal oxidation (RTO) technique or the conventional furnace tube oxidation (FO) technique. To create the RTO films, surface oxidation was carried out at 900 C in a dry-oxygen atmosphere for 12 sec. Surface oxidation was carried out at 950 C in a dry-oxygen atmosphere for 23 sec to create 3.3-nm-thick oxide RTO films. 2.2-nm-thick FO films were created by carrying out surface oxidation at 700 C for 20 min for in a dry-oxygen atmosphere. Next, phosphorus-doped poly-Si film was deposited by the low-pressure chemical-vapor deposition technique. The effective gate area was $3x10^4$ $\mu m^2$. Since the poly-Si electrode patterns were formed by wet-etching to minimize process-induced damage, we could evaluate the intrinsic properties of ultra-thin oxide films without any extrinsic influence.

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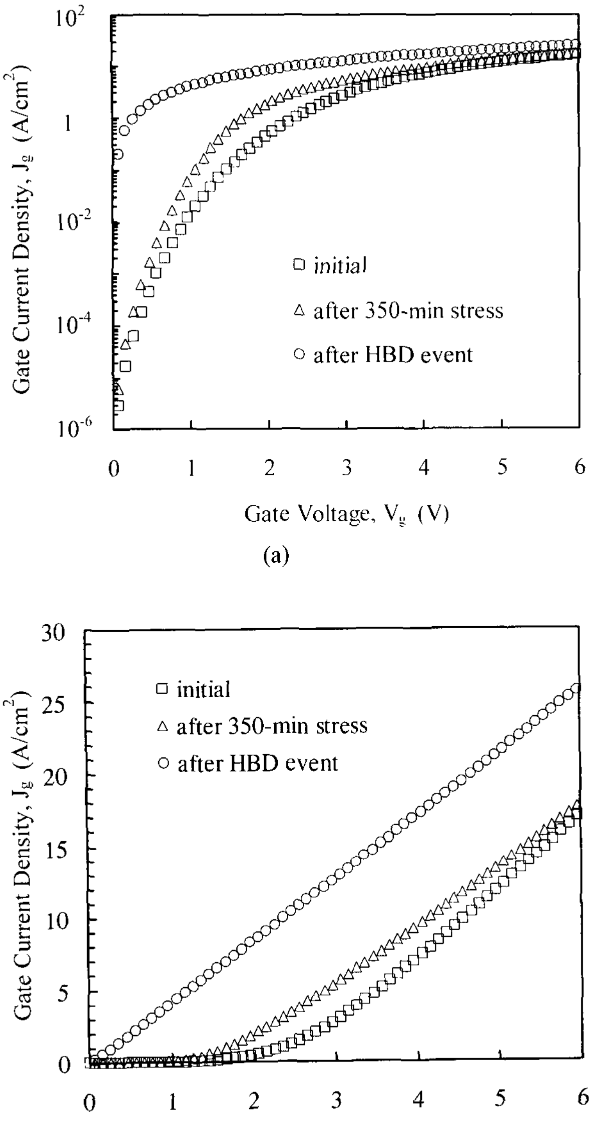


(a)

(b)

**Fig. 1.** Gate voltage ($V_g$) dependence of gate current density ($J_g$) for 2.2-nm-thick $SiO_2$ film. (a) $J_g$ versus $V_g$ characteristics in a logarithmic scale. (b) $J_g$ versus $V_g$ characteristics in a linear scale.

## III. RESULTS AND DISCUSSION

Gate voltage ($V_g$) dependencies of initial gate current, stress-induced leakage current (SILC), and post-HBD gate current for several 2.2-nm-thick films (RTO) are shown in Figs. 1(a) and 1(b); in Fig. 1(a), the vertical axis is a logarithmic scale to show the initial gate current and the SILC clearly, and in Fig. 1(b), the vertical axis is a linear scale to show the post-HBD gate current clearly. SILC was observed after constant-voltage stress (CVS) of 10.3 V (47 MV/cm) had been applied to the film for 6 hours. Since the gate current saturates as a function of stress time for a certain fixed stress condition (see Fig. 3(a)), it is concluded that the post-stressed gate current is SILC, not soft breakdown [5,6]. We also concluded that soft breakdown was not observed after additional CVS because the additional CVS did not include remarkable digital changes in leakage current and fluctuation amplitude under the stress [7]. HBD occurred when additional CVS, 17.6 V (80 MV/cm) for 10 msec, was applied to the film after measuring the SILC characteristics. When the post-stressed gate current at $V_g$ of 1 V increases by two orders, it has been concluded that HBD has occurred (see Fig. 1). The fundamental aspects of gate current characteristics shown in Fig. 1 were reproduced by 100 samples. Regarding these observations, three significant experimental results were noted. (i) Although CVS of 10.3 V (47 MV/cm) was applied to a 2.2-nm-thick oxide film for 10 hours, HBD was not observed. (ii) When CVS of 11.4 V (52 MV/cm) was applied to a 2.2-nm-thick oxide film for 10 msec, HBD was always observed. (iii) HBD was not observed when CVS of 13 V (60 MV/cm) for 10 min was applied to the oxide film after CVS of 10.3 V (47 MV/cm) was applied to the film for 10 min.

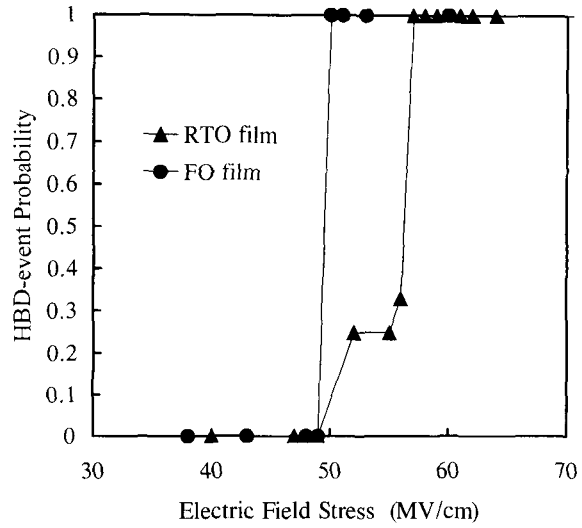
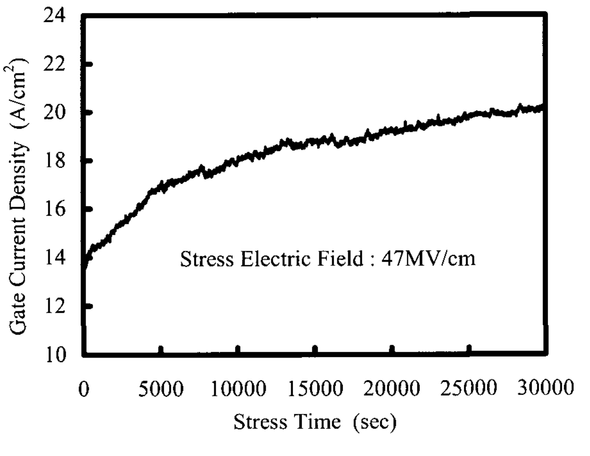
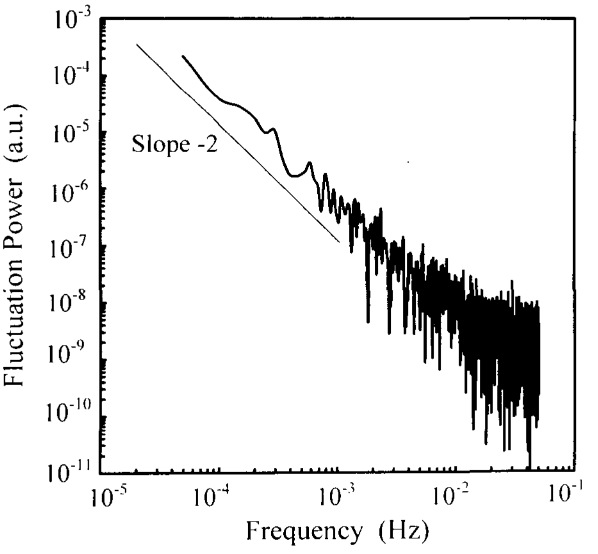


**Fig. 2.** HBD-event probability versus electric field stress.

Results (i) and (ii) suggest that the HBD of 2.2-nm-thick oxide films is strongly related to electric field stress because CVS conditions for (i) and (ii) are almost identical. So, we investigated the HBD-event probability as a function of electric field stress. The dependence of HBD-event probability on electric field stress is shown in Fig. 2; 10 samples were tested for each stress condition. When the electric field stress is below 50 MV/cm, HBD does not occur, even if CVS of 11 V is imposed for more than 10 hours. This finding is independent of the oxidation technique used.



(a)



(b)

**Fig. 3.** Gate current density dependence on time under CVS for 2.2-nm-thick RTO film. Constant voltage for stressing is 10.3 V (a). Gate current density dependence on time under CVS (b) Fluctuation power dependence of gate current on frequency under CVS.

In the case of 2.2-nm-thick FO films, electric field stress higher than 50 MV/cm always triggers HBD within 10 msec. In the case of 2.2-nm-thick RTO films, the electric field stress must be higher than 57 MV/cm to trigger HBD. For electric field stress ranging from 50 MV/cm to 55 MV/cm, the HBD-event probability for RTO films has a finite value ranging from 0 to 1; it is considered that this reflects the non-uniformity of oxide quality, including surface roughness. Thus, the critical electric field with regard to HBD is found in Fig. 2.

We must investigate gate current behavior under CVS from point of view of film robustness. So, gate current dependence on time under the CVS condition of 10.3 V (47 MV/cm) is shown in Fig. 3(a) for the RTO film; several devices were tested. It is clearly found that the device does not show the HBD event even after CVS for 30000 sec, although the gate current moderately increases with stress time and saturates. So, we have to conclude that 2.2-nm-thick $SiO_2$ film is inherently robust. Recently, H. S. Momose et al demonstrated the reliability of 2-nm-thick $SiO_2$ films [8], where electrical stress of about 16 MV/cm was applied to devices and they showed very short lifetime. This should be interpreted that process-induced damage has reduced film lifetime. We also inspected the feature of voltage fluctuation seen in Fig. 3(a). Fourier transform of voltage fluctuation is shown Fig. 3(b). The fluctuation power shows typical $1/f^2$ spectra, which strongly suggests that there exist specific defects characterized by a single energy level.

On the other hand, aforementioned results (ii) and (iii) suggest that breakdown-immunity is improved when a stress, which is not strong enough to trigger HBD event, is applied to the oxide film as a first step. The relationship between stress method and the occurrence of HBD for RTO films is summarized in Fig. 4. In method (A), one-second CVS of 14 V (64 MV/cm) was applied to the oxide film; HBD was always observed. In method (B), one-second CVS of 14 V (64 MV/cm) was applied to the oxide film after the application of CVS of 10.8 V (49MV/cm) for 10 min; at this point, however, HBD was not observed. Next, HBD was always observed, after one-second CVS of 18.7 V (85 MV/cm) was applied to the film. In method (C), after CVS of 10.8 V (49 MV/cm) for 600 sec, CVS of 14 V (64 MV/cm) was applied to the oxide film for 5 sec. After that, an additional CVS of 18.7 V (85 MV/cm) was applied to the oxide film for 40 sec; this method seemed to prevent

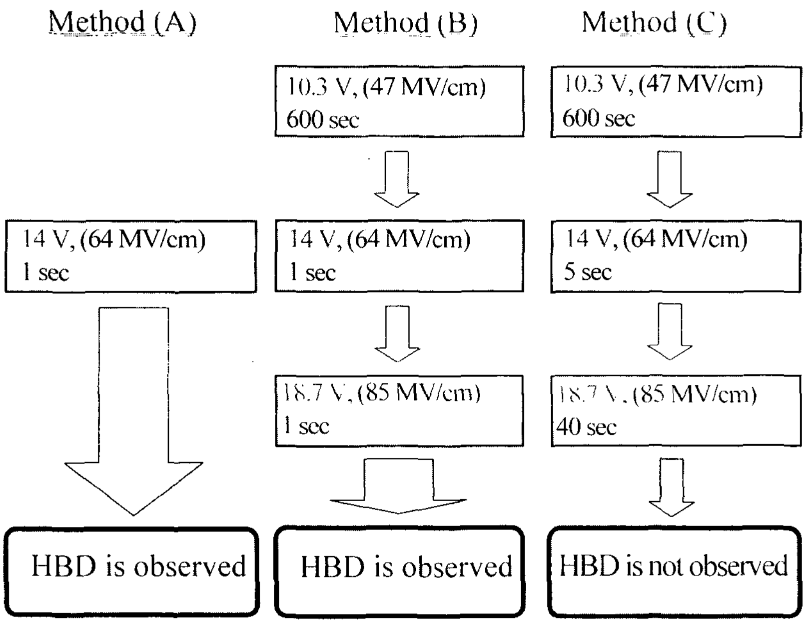


**Fig. 4.** Relationship between stress methods and occurrence of HBD for RTO film.

HBD completely. Similar results were also obtained for FO films. Comparing method (B) to method (A) clearly shows that applying a weak initial stress, which does not lead to HBD, improves the films' breakdown-immunity. Comparing method (C) to method (B) indicates that this immunity is drastically improved as the duration period of the weak initial stress increases.

So, we discuss the influence of low stress voltage prior to high stress voltage which should lead to HBD. When CVS of 11 V (50 MV/cm) is applied to the oxide film, the energy of 660 J/cm$^2$ is dissipated per second by the stress current. Assuming that the present MOS structure is expressed as a parallel circuit composed of a resistor and a capacitor, the capacitance value is equal to 4.6x10$^{-10}$ F, the tunnel resistance value is approximately equal to 1 kΩ and so the discharging time constant is estimated to be about 5x10$^{-7}$ sec. When we assume that a 100-% step-up of gate current is observed at the HBD event, the electrostatic energy of about 10$^6$ J/cm$^2$ should be emitted per second [9]. The energy dissipated by the stress current (660 J/cm$^2$ per sec.) is much smaller than the electrostatic discharge energy. This suggests that the low stress current under the weak CVS condition probably makes traps in the SiO$_2$ film, but seldom triggers HBD.

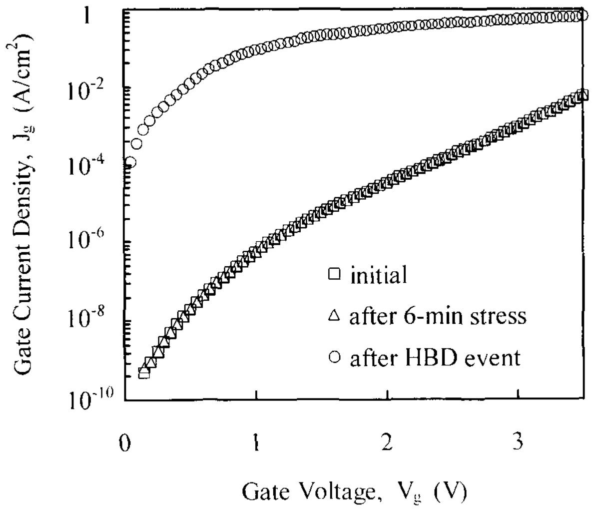


**Fig. 5.** Gate voltage ($V_g$) dependence of gate current density ($J_g$) for 3.3-nm-thick SiO$_2$ film.

In addition, we examined the difference between the breakdown mechanisms of about 2-nm-thick oxide films and over 3-nm-thick oxide films. We consider why the breakdown immunity is improved by applying a weak initial stress to the film. In order to estimate the trap density of thin SiO$_2$ films, the simple method proposed by D. J. DiMaria et al. is utilized [6]. When we consider the case of a 2.2-nm-thick SiO$_2$ film (RTO) to which

CVS of 10.8 V (49 MV/cm) has been applied for 6 hours (Fig. 1), *the estimated magnitude of created trap density* is about 3.7 (arbitrary units). For comparison, gate voltage ($V_g$) dependencies of initial gate current, stress-induced leakage current (SILC), and post-HBD gate current for 3.3-nm-thick film (RTO) are shown in Fig. 5. SILC was observed after constant-voltage stress (CVS) of 4.3 V (13 MV/cm) had been applied to the film for 360 sec. In this case, the estimated magnitude of created trap density is about 0.058 (arbitrary unit). This is much smaller than the value for the case of a 2.2-nm-thick $SiO_2$ film, which seems to be a discrepancy. However, this is resolved by the following consideration.

It can be argued that many local traps created in the 2.2 nm film release the stored electrostatic energy fast by trap-assisted tunneling because the effective tunnel resistance of 2.2-nm-thick $SiO_2$ film is relatively small, which prevents HBD. *In the* 3.3-*nm-thick* $SiO_2$ *film*, on the other hand, local traps created in the film release the stored electrostatic energy very slowly by quite limited trap-assisted tunneling because the effective tunnel resistance of 3.3-nm-thick $SiO_2$ film is large; relatively high electrostatic energy is stored across the film. Consequently, a local weak spot, in the 3.3-nm-thick $SiO_2$ film, readily induces the HBD [10].

## IV. CONCLUSION

This paper mainly discussed the hard breakdown of 2.2-nm-thick $SiO_2$ films. It has been shown that the hard breakdown event of a 2.2-nm-thick $SiO_2$ film greatly depends on the applied electric field. It is strongly suggested that the local weak spots created by applying a low initial stress to a 2.2-nm-thick $SiO_2$ film resist the onset of hard breakdown. In other words, it is anticipated that the stored electrostatic energy is fast dissipated by trap-assisted tunneling in 2.2-nm-thick $SiO_2$ film. Consequently, it is strongly suggested that 2.2-nm-thick $SiO_2$ films are intrinsically quite robust.

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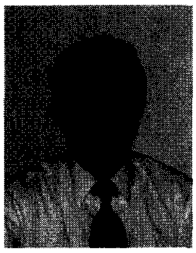

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He has invented various SOI devices – for example - the lateral unidirectional bipolar-type insulated-gate transistor (Lubistor), the high-gain cross-current tetrode (HXT) MOS device, and tunneling-barrier junction (TBJ) SOI MOSFET using SIMOX technology. He has patents for Lubistor in Japan, U.S.A., Canada, United Kingdom, France, Germany, Netherlands, Italy, and Korea. He has 30 patents in Japan and several patents in U. S. A. for SIMOX device technology. He was honored with the Annual Young Researcher Award in 1981 from IEICE, Japan. He has worked on ultra-thin MOSFET/SIMOX device technology over 20 years. Last decade, he demonstrated 0.1-μm-gate CMOS/SIMOX devices with a long lifetime in 1991 IEEE IEDM and 1992 Int. Conf. on Solid State Devices and Materials (SSDM). He also demonstrated mesoscopic transport characteristics of 50-nm-channel SOI MOSFETs with 2- or 6-nm-thick silicon film in order to indicate perspectives of future SOI devices in 1997.

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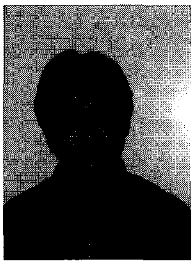

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