Ta/TaN$_x$ Metal Gate Electrodes for Advanced CMOS Devices

S. J. Lee and D. L. Kwong

Abstract— **In this paper, the electrical properties of PVD Ta and TaN$_x$ gate electrodes on SiO_2 and their *thermal stabilities are investigated.* The results show that the work functions of TaN$_x$ gate electrode are modified by the amount of N, which is controlled by the flow rate of N_2 during reactive sputtering process. The thermal stability of Ta and TaN$_x$ with RTO-grown SiO_2 gate dielectrics is examined by changes in equivalent oxide thickness (EOT), flat-band voltage (V_{FB}), and leakage current after post-metallization anneal at high temperature in N_2 ambient. For a Ta gate electrode, the observed decrease in EOT and leakage current is due to the formation of a Ta-incorporated high-K layer during the high temperature annealing. Less change in EOT and leakage current is observed for TaN$_x$ gate electrode. It is also shown that the frequency dispersion and hysteresis of high frequency CV curves are improved significantly by a post-metallization anneal.**

Index Terms — **Metal gate electrode, Gate stack engineering, CMOS Fabrication process.**

I. INTRODUCTION

Dual poly-Si gate has been used as a gate electrode for CMOS devices. However, as aggressive device scaling continues, poly-Si gate is being considered to be phased out due to its inherent limitations. First, the poly-depletion effect at the poly-Si/oxide interface, caused by insufficient dopant activation, results in drive current degradation [1], and this effect becomes more serious as the supply voltage and gate oxide thickness are scaled down [2]. Second, the Boron penetration for p-MOSFET is another major concern, particularly for ultra thin SiO_2, which induces traps in the gate oxide, resulting in the degradation of mobility and reliability [3]. Finally, poly-Si can't meet the requirements of resistivity for future gate electrode [4].

For these reasons, increasing demands for the development of metal gate electrode replacing dual poly-Si gate have recently emerged. However, in order to replace conventional poly-Si gate, metal gate must meet the stringent requirements. One of the key issues for metal gate electrode is the control of its work function which should be compatible to both n- and p-MOSFETs. Considering the device performance and the impact of short-channel effects for sub-100nm technology, the optimal gate electrode work function should be near the conduction and valence band edges for n- and p-MOS devices, respectively [5]. Also, these metal gate electrodes must have required thermal stability with underlying gate oxide during high temperature device processing steps.

In this paper, the work function modification and the thermal stability of Ta and TaN$_x$ gate electrodes are investigated, using RTO-grown SiO_2 as the gate dielectric.

II. EXPERIMENTS

In this work, MOS capacitors were fabricated on p-type (100) silicon wafers. After standard RCA cleaning

Manuscript received July 12, 2002; revised September 11, 2002.
Microelectronics Research Center, Department of Electrical and Computer Engineering, The University of Texas, Austin, TX 78712, USA
E-mail: sungjoo@aist.go.jp **Tel :** 81-298-49-1641

and final HF dip, 20~25 Å SiO_2 gate dielectric was grown by RTO (Rapid Thermal Oxidation) at 950 °C. The TaN_x gate electrodes (200~250 nm) were deposited directly on SiO_2 by reactive sputtering of Ta and N_2. The N ratio in the TaN_x films is controlled by the flow rate of N_2. The gate patterning was done with dry-etching of TaN_x gate electrode by RIE, followed by the post-metallization anneal performed in N_2 ambient at 800 ~ 1000 °C.

The resistivity of TaN_x gate was obtained by 4-point probe measurement, and the capacitance was measured by LCR meter (HP4276) and IV characteristics were measured by semiconductor parameter (HP4145). The EOT of MOS capacitors were extracted from a simulation program considering quantum mechanical (QM) effects [6].

III. Results and Discussion

Fig. 1 shows the resistivity of TaN_x gate and V_{FB} of MOS capacitors as a function of N_2 flow rate used in reactive sputtering. First, as the N_2 flow rate increases, it is observed that the resistivity of TaN_x gate is increased from 0.025 mΩ·cm (N_2: 0 sccm, i.e. Ta gate) to 3.121 mΩ·cm (N_2: 10 sccm), indicating that the N ratio (x) of TaN_x gate is modified by controlling the flow rate of N_2. The flat-band voltages of MOS capacitors with SiO_2 are also increased, i.e., shifted to positive, as increasing the N ratio in TaN_x gate. The positive shift of V_{FB} is caused by the increase of work function of TaN_x gate electrode.

In Fig. 2, the high-frequency C-V curves of SiO_2 gate dielectrics (EOT~25 Å) with (a) poly-Si gate doped with $POCl_3$, (b) Ta gate (N_2 : 0sccm), and (c) TaN_x gate (N_2 : 10sccm) are compared. Since the work function of $POCl_3$-doped poly-Si gate is ~ 4.2 eV, the work functions of Ta gate and TaN_x gate are estimated to be ~ 4.43 eV and ~ 4.75 eV, respectively, from the differences of flat-band voltages, assuming the insignificant differences in the amount of fixed charges in these gate stacks. Considering the required work function for n-MOS device (~4.2 eV) and p-MOS device (~5.1 eV), the obtained work function of Ta gate is slightly higher for n-MOS device, and more N in TaN_x is needed in order to get proper work function for p-MOS devices.

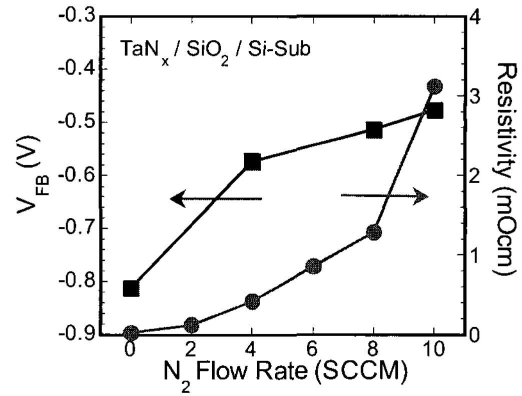

Fig. 1. Resistivity and V_{FB} of TaN_x / SiO_2/ Si-sub gate stacks as a function of N_2 flow rate.

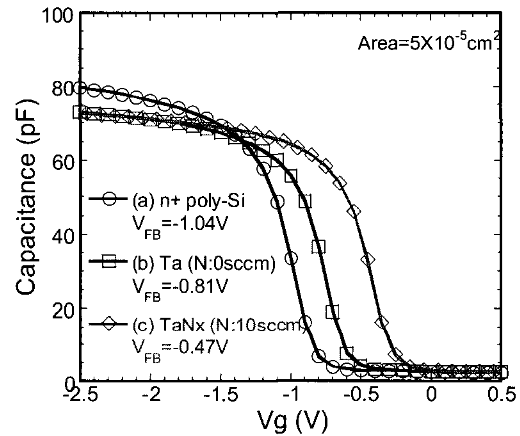

Fig. 2. High-frequency CV of SiO_2 with (a) n+ poly-Si, (b) Ta, and (c) TaN_x gate electrodes.

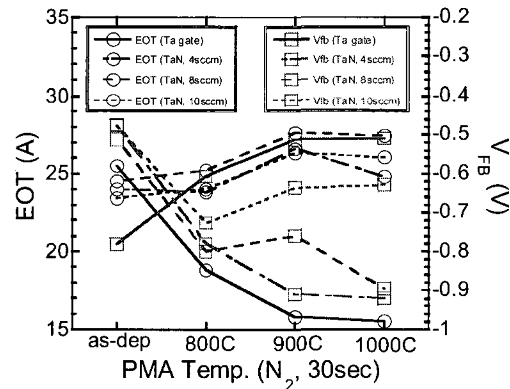

Fig. 3. EOT and V_{FB} of Ta and TaN_x gated SiO_2 devices as a function of anneling temperature.

The thermal stability of these TaN_x gate electrodes with underlying SiO_2 gate dielectric is examined with post-metallization anneal in N_2 at high temperature. Fig. 3 shows the changes in EOT and V_{FB} of TaN_x / SiO_2 gate

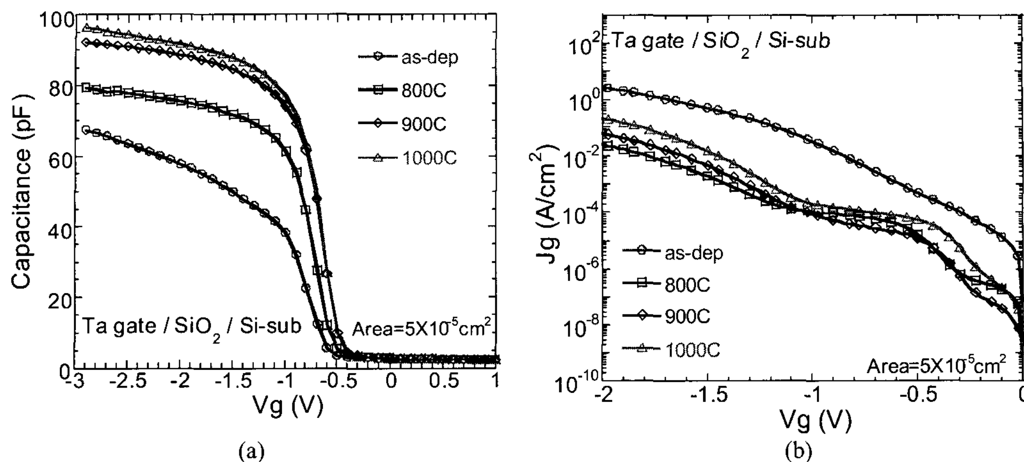

Fig. 4. (a) C-V and (b) I-V of Ta gated SiO_2 for as-deposited and after post-metallization anneal.

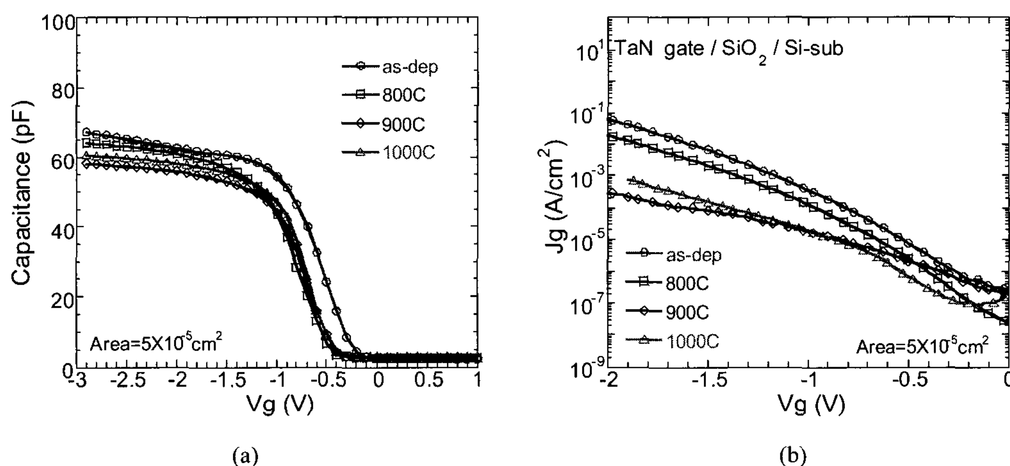

Fig. 5. (a) C-V and (b) I-V of TaN_x gated SiO_2 for as-deposited and after post-metallization anneal.

stacks as a function of annealing temperature. The changes in EOT of gate stacks can result from the interaction at the gate/dielectric interface as well as the oxidation of the Si-substrate due to oxygen diffusion through the gate stack during high temperature annealing. For the Ta gate (N_2 : 0sccm), the EOT of the as-deposited Ta gate devices decreases as the annealing temperature increases (from 26 Å to 15 Å). This result suggests that during the post-metallization annealing process, a Ta-incorporated high-K dielectric layer is formed at the Ta / SiO_2 interface while consuming some of the underneath SiO_2. Both the formation of high-K layer and the consumption of low-K SiO_2 layer contribute to the overall EOT reduction. This conclusion is also supported by the leakage current reduction data to be discussed later. In addition, the positive shift of V_{FB} is observed as the annealing temperature increases. This result can be explained by the modification of the effective work function caused by the interaction ofTa and SiO_2 [7].

For the TaN_x gate electrodes (N_2 : 4~10 sccm), less increase (~3 Å) in EOT is observed as the annealing temperature increases. This result indicates that the interaction with SiO_2 is suppressed for N-incorporated TaN_x gate. The small increase in EOT may result from the oxidation of the Si-substrate due to oxygen diffusion to the SiO_2 / Si interface during high temperature annealing. The V_{FB} of annealed TaN_x devices shifted negatively compared to the as-deposited device, possibly caused by the modification of work function from the changes in orientation and phase of TaN films [8].

Fig. 4 shows the (a) C-V and (b) I-V characteristics of Ta / SiO_2 gate stack for several annealing conditions.

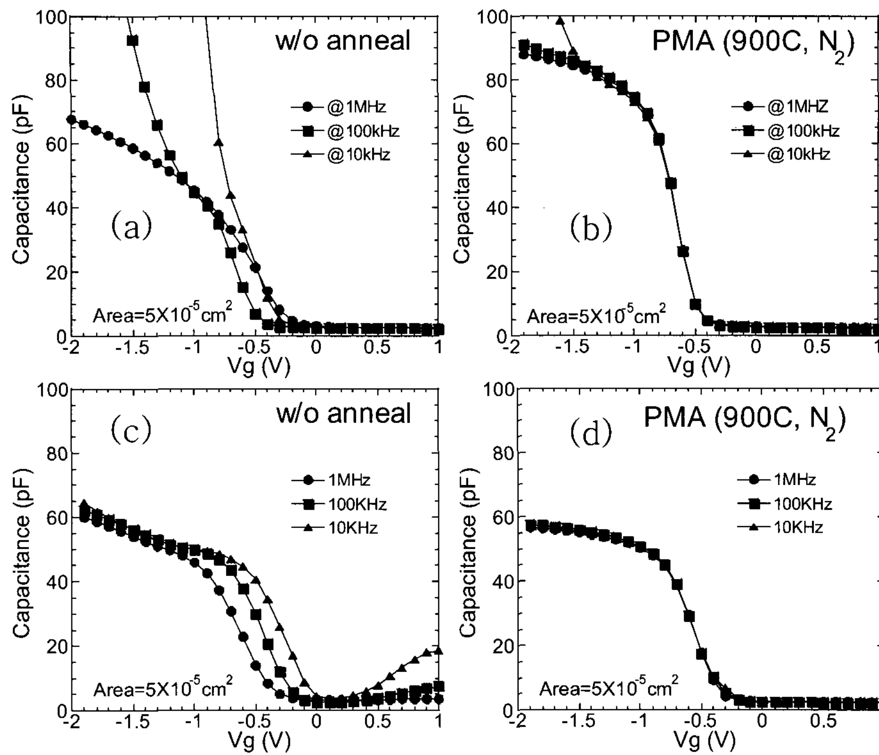

Fig. 6. Frequency dispersion of (a) Ta gate without anneal, (b) Ta gate after 900C anneal, (c) TaN_x gate without anneal, (d) TaN_x gate after 900C anneal.

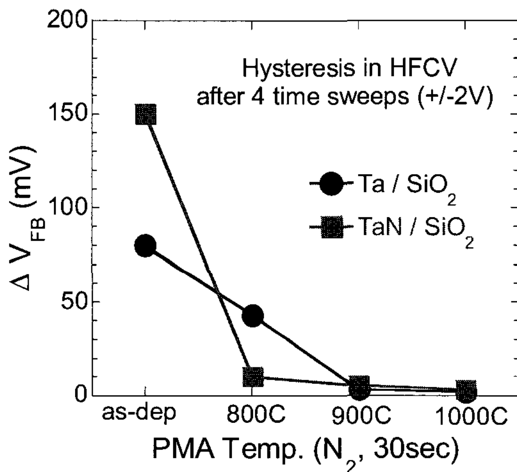

Fig. 7. Hysteresis of Ta and TaN_x gated SiO_2 as a function of anneling temperature.

The increase in accumulation capacitance indicates a decrease in EOT as the annealing temperature increases. It should be noted that the leakage current of the annealed device is also reduced compared to the as-deposited device. This result also supports the argument that the decrease in EOT is caused by the formation of a high-K layer with simultaneous consumption of underlying SiO_2, so that the physical thickness of the resulting gate dielectric is actually increased. Therefore, for a given EOT, the tunneling leakage current is reduced. Removal of plasma damage by the post-metallization anneal may have also contributed to the leakage current reduction. The C-V and I-V characteristics of TaN_x / SiO_2 gate stack are shown in Fig. 5. As discussed before, less change in capacitance is seen with some decrease in leakage current.

The frequency dispersion of Ta and TaN_x gated devices are compared in Fig. 6. As-deposited devices of both Ta and TaN_x gate show significant dispersions in C-V at 10 k ~ 1 MHz, indicating the existence of interface states and traps. However, after post-metallization anneal in N_2, the C-V show negligible dispersions for 10 k ~ 1 MHz (Fig. 6 b, d). We have also examined the hysteresis in C-V, measured by the V_{FB} shift after 4 time sweeps between +2V and -2V, as a function of annealing temperature in Fig. 7. For both Ta and TaN_x gated devices, the hysteresis is reduced to less than 10 mV after 900 °C annealing.

IV. Conclusion

We have investigated the electrical properties of PVD Ta and TaN_x gate electrodes on SiO_2 and their thermal stabilities. The results show that the work functions of TaN_x gate electrode are modified by the amount of N, which is controlled by the flow rate of N_2 during reactive sputtering process. The thermal stability of Ta and TaN_x with RTO-grown SiO_2 gate dielectrics is examined by changes in equivalent oxide thickness (EOT), flat-band voltage (V_{FB}), and leakage current after post-metallization anneal at high temperature in N_2 ambient. For a Ta gate electrode, the observed decrease in EOT and leakage current is due to the formation of a Ta-incorporated high-K layer during the high temperature annealing. Less change in EOT and leakage current is observed for TaN_x gate electrode. It is also shown that the frequency dispersion and hysteresis of high frequency CV curves are improved significantly by a post-metallization anneal.

References

[1] K. F. Schuegraf, et al., *Symp. VLSI Tech.*, p. 86, 1993
[2] M. Rodder, et al., *IEDM'96*, p. 563, 1996
[3] T. Kuroi, et al., *IEDM'93*, p. 325, 1993
[4] *The National Technology Roadmap for Semiconductors*, 2001 ed., Semiconductor Industry Association
[5] Indranil De, et al., *Solid-State Electronics*, **44**, 1077, 2000
[6] J. R. Hauser et al., *Characterization and Metrology for ULSI Technology*, p. 235, 1998
[7] Y-. C. Yeo, et al., *Symp. VLSI Tech.*, p, 2001
[8] H. B. Nie, et al., *Appl. Phys.* A 73, 229, 2001

Sungjoo Lee Dr. Lee received the B. S. degree in electrical engineering from the Seoul National University in 1989, and the M.S. and Ph. D degrees in electrical engineering from University of Texas at Austin, USA in 2000 and 2002, respectively. After he joined the Microelectronic Research Center of University of Texas in theSolid State Electronics divisions in 1998, his research field has been focused on the development of new high-K gate dielectrics and characterization of performance and reliability of CMOS devices. He is currently working for the MIRAI project high-K gate stack group, Tsukuba, Japan. His present interests and activities cover the development and characterization of advanced metal gate electrode / high-K gate stacks for sub 100nm VLSI technologies and the study of reliability characteristics of high-K gate dielectrics.

Dim-Lee Kwong received his B.S. degree in Physics and M.S. degree in Nuclear Engineering, both from the National Tsing Hua University, Taiwan, in 1977 and 1979, respectively. In 1982 he received the Ph.D. degree in Electrical Engineering from Rice University and received Best Dissertation Award. He was an Assistant Professor of Electrical Engineering Department at the University of Notre Dame during the years 1982-1985. He was a Visiting Scientist at the IBM General Technology Division, Essex Junction, Vermont during the summer of 1985 working on 4 Megabit DRAM technology. He joined The University of Texas at Austin, Microelectronics Research Center and Department of Electrical and Computer Engineering in 1985 as an Assistant Professor. He was promoted to Associate Professor in 1986 and to Full Professor in 1990.

Dr. Kwong received numerous awards including the IBM Faculty Development Award in 1984 and the Engineering Foundation Award from The University of Texas at Austin in 1994, holds the Earl N. and Margaret Brasfield Endowed Fellowship, is the author of more than 210 referred journal and more than 200 referred conference proceeding publications, and has been awarded with more than 11 U.S. patents. His current areas of research interests include rapid thermal CVD technology for the growth and deposition of semiconductor materials compatible with ULSI processes, advanced dielectrics for logic, analog, and memory devices, metal gate electrode, shallow junctions, diffusion barrier materials and processes, and diffusion modeling of ion-implanted species during rapid thermal annealing.