Device characterization and Fabrication Issues for Ferroelectric Gate Field Effect Transistor Device

Byoung –Gon Yu, In-Kyu You, Won-Jae Lee*, Sang-Ouk Ryu, Kwi-Dong Kim, Sung-Min Yoon, Seong-Mok Cho, Nam-Yeal Lee, and Woong-Chul Shin

Abstract - **Metal-Ferroelectric- Insulator- Silicon (MFIS) structured field effect transistor (FET) device was fabricated and characterized. Important issues to realize ferroelectric gate field effect transistor device were summarized in three sections. The choice of interlayer dielectric was made in the consideration of device functionality and chemical reaction between ferroelectric materials and silicon surface during fabrication process. Also, various ferroelectric thin film materials were taken into account to meet desired memory window and process compatibility. Finally, MFIS structured FET device was fabricated and important characteristics were discussed. For feasible integration of current device as random access memory array cell address schemes were also suggested.**

Index Terms – **SBT, sol-gel, FRAM, ferroelectric, thin film, capacitor, gate dielectric, hysteresis loop, TEM**

I. INTRODUCTION

In recent years, FRAM (ferroelectric random access memory) has drawn great attention in needs of functionality and low power consumption for a system on a chip and mobile device applications.[1] Great progress in manufacturing and material engineering technology has driven integration of ferroelectric memory devices up to 32 MB (Samsung Electronics).[2] However, the memory density developed till now is still too low compared to DRAM devices. To increase a number of memory unit in a silicon wafer device structure must be improved to utilize the area effectively. There are three well-known device structures for FRAM. In early stage a memory unit consists of 2transitor and 2capacitor (2T/2C) based on DRAM memory structures. Later, semiconductor industries have tried to develop FRAM with 1T/1C structures because of cell effectiveness. As shown in Fig. 1 a 1T/1C structure has one MOSFET transistor and one ferroelectric capacitor as a memory unit. Although 1T/1C structure showed possibility to make high density FRAM devices the stored data must be restored as a original state after reading, which is so called "destructive readout". Recently researchers try to realize another possible way to increase density of memory cell, yet achieve more effective method to write and read the stored data. One transistor type ferroelectric memory (1-Tr FRAM) utilizes ferroelectric thin film material as gate oxide in MOSFET device.[3] While 1-Tr FRAM has many advantages such as non-volatile data storage, non-destructive readout, low power consumption and cell effectiveness it still needs to overcome several obstacles for reliable operation of the device.

To realize reliable 1-Tr FRAM devices, at first, ferroelectric thin film-silicon interface has to be controllable in the current CMOS fabrication process. The integration of ferroelectric material directly on silicon is extremely hard. Therefore, high dielectric

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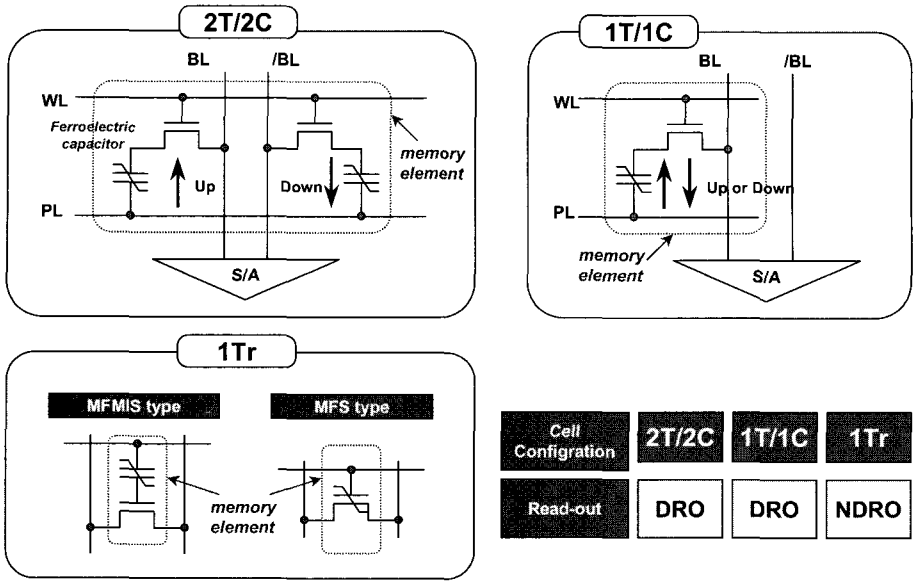

Fig. 1. Types of Ferroelectric memories.

constant-insulating layer in between ferroelectric material and silicon surface is required to control interface reaction and to obtain good retention characteristics. Moreover, film deposition and etching technique must be refined to maintain good ferroelectric characteristics. In this paper, we present modeling of device structure, selection of material and fabrication of 1-Tr FRAM device array. Especially, 1-Tr FRAM characteristics utilizing $SrBi_2Ta_2O_9$ (SBT) thin film and their performance dependence on process technique and inter-dielectric materials such as Si_3N_4/SiO_2 compound material and Al_2O_3 were investigated. For reliable fabrication of 1-Tr FRAM, CMOS compatible device fabrication techniques are also presented.

II. Application of Ferroelectric Thin Films on Mfis-fet devices

A. *Section of ferroelectic and inter-dielectric layer materials*

Structures of devices using FRAM may be categorized into field effect transistor (FET)-type and capacitor-type; manufactured goods at the present time use the latter type. In both cases, ferroelectric materials play important role in functionality of the FRAM devices. In the case of FET-type FRAM, a metal-ferroelectric-semiconductors (MFS) have been studied for over 30 years world wide but, reliable products have not been yet demonstrated due to the difficulty of forming reliable ferroelectric thin films directly on silicon.[4, 5] Elements in the films may diffuse into silicon, forming uncontrollable oxide layers and thus degrading interface characteristics. To solve these problems, metal-ferroelectric-insulator-semiconductors (MFIS) structures have been suggested and increasingly studied. Among insulators (inter-dielectric layers), silicon dioxide, silicon nitride, CeO_2, ZrO_2, MgO, and others are used.[6-9] In general, Metal-Ferroelectric-Insulator-Silicon(MFIS) is composed of series capacitor of each layers. Therefore, dielectric constants of each layer are important device operation factor in the device. For a series capacitor, a ferroelectric material having reasonable saturation polarization value has a benefit to reduce risk of thin inter-dielectric breakdown. Moreover, the dielectric constant of inter-dielectric layer must be comparatively high to reduce depolarization field applied to ferroelectric films under short circuited state.

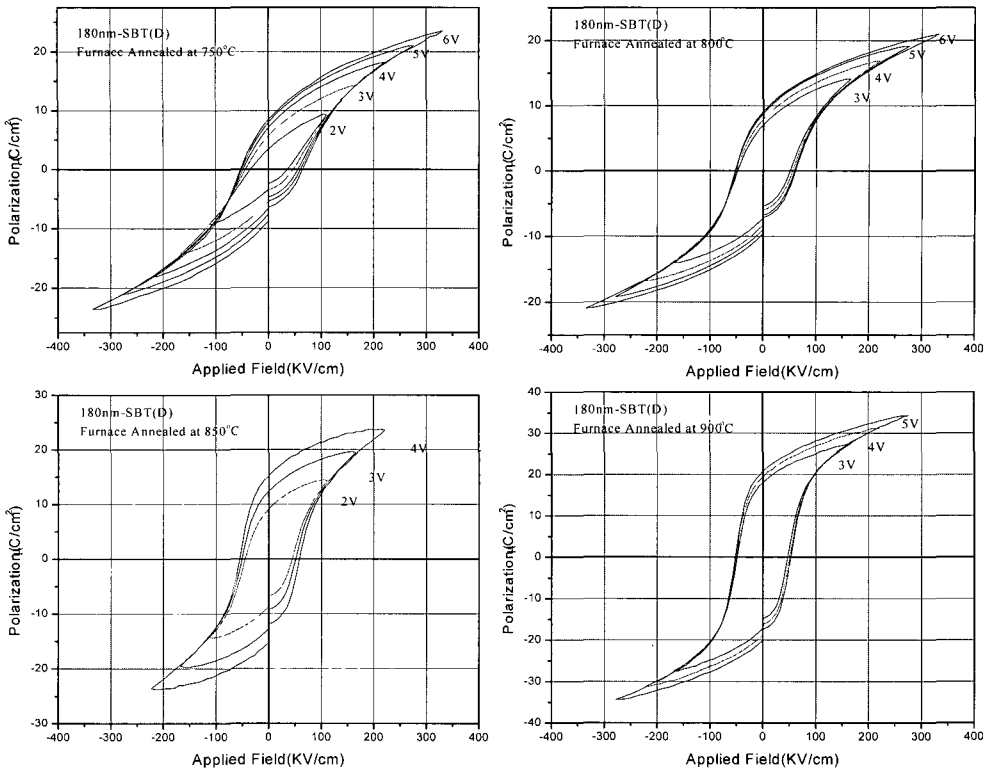

Fig. 2. Typical hysterisis behavior of SBT thin films as a function of annealing temperatures.

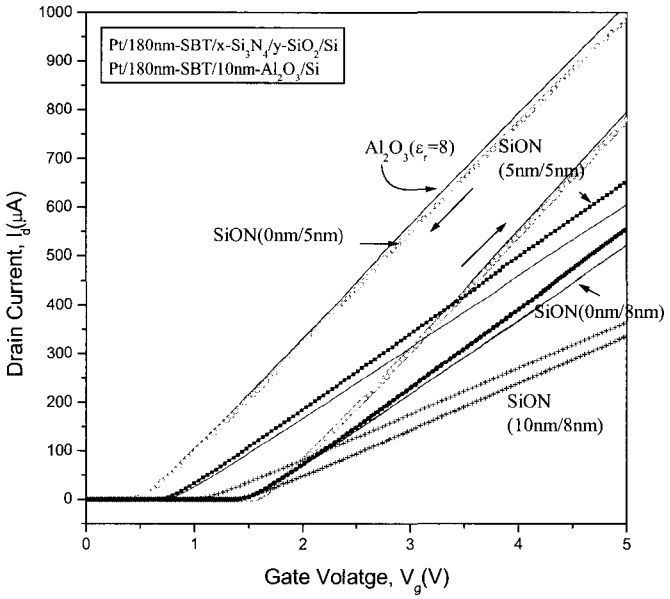

Fig. 3. The transistor current-voltage curves of MFIS structures having various insulator structures.

The most widely researched materials until now are PZT($PbZr_xTi_{1-x}O_3$), $BaMgF_4$ and $SrBi_2Ta_2O_9$ thin films. Among ferroelectric materials $BaMgF_4$ thin film has been widely researched for direct integration on bare silicon surface therefore its structural simplicity in the device.[10] However, it has been reported that spontaneous polarization vector in a $BaMgF_4$ film on Si(100) is parallel to the sample surface, and thus use of

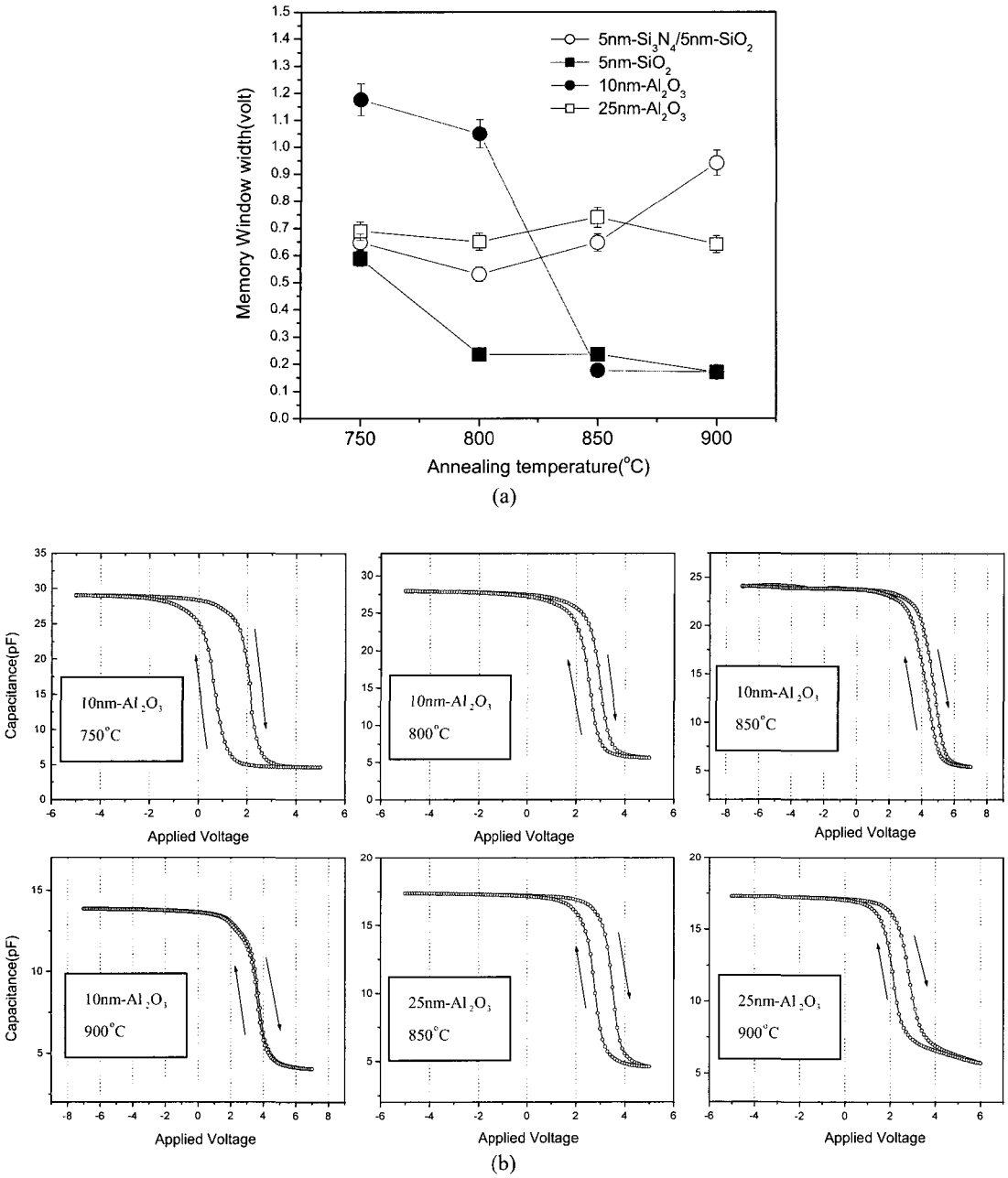

Fig. 4. Characteristics of SBT thin films on various insulator layers in MFIS structures (a) memory window of SBT thin films according to annealing temperatures and insulator thickness (b) C-V curves of SBT thin films in $Pt/SBT/Al_2O_3/Si$ structures.

Si(111) is necessary. Since $SrBi_2Ta_2O_9$ thin films have been applied to FRAM device many researches has been performed using $SrBi_2Ta_2O_9$ as ferroelectric material.[11] $SrBi_2Ta_2O_9$ has a merit over PZT for its lower polarization value, low leakage current density and lower dielectric constant by which possible reduction of device operating voltage. Typical ferroelectric hysterisis loop on $Pt/Ti/SiO_2/Si$ substrates is shown in Fig. 2. For higher annealing temperature ferroelectric P-E loop becomes upright square shape. But, at annealing temperature higher than 850 °C the film showed leaky properties possibly due to bottom electrode instability. Measured dielectric constant of the $SrBi_2Ta_2O_9$ films was about 150. From these results, the electrical properties of $SrBi_2Ta_2O_9$ films showed the most suitable characteristics on the application of MFIS-FET devices.

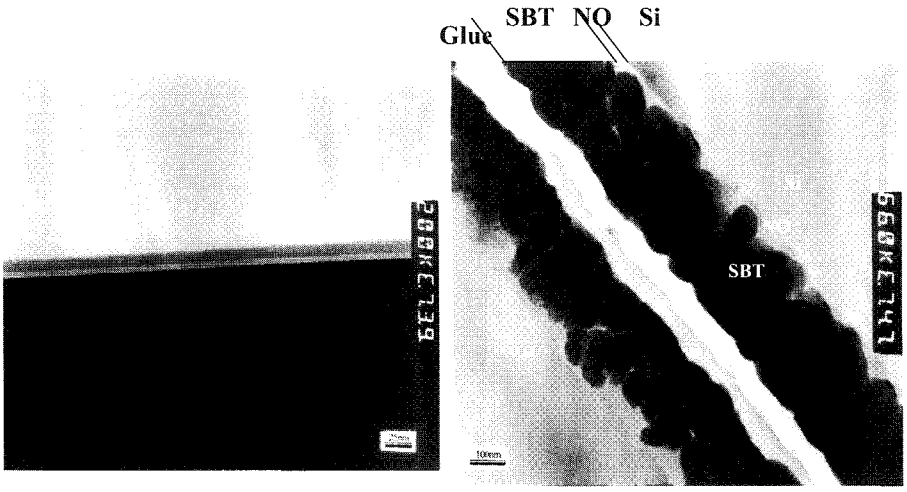

Fig. 5. TEM images of SBT/NO/Si structure. SBT was annealed at 850 °C

Here, we tried to evaluate various inter-dielectric films in the Pt/SBT/Insulator/Si structure based on the method developed by Miller and McWhorter. Figure 3 shows transistor current – voltage curves of MFIS structures. The remanent polarization, coercive field and dielectric constant of SBT films used in this calculation are about $0.5\mu C/cm^2$, 50kV/cm and 150, respectively. The threshold voltage shift associated with hysterisis varies with the dielectric constant and thickness of the insulating layers. As the relative capacitance value of the inter-dielectric can influence the hysterisis window, it is predicted that the 10nm-Al_2O_3, 5nm-Si_3N_4/5nm-SiO_2 and 5nm-SiO2 structures could be applied for use in real device.

B. *Cacteristics of SBT layer in MFIS structures*

Various parameters of ferroelectrics and inter-dielectrics affecting the current driving capability and hysteretic memory window have been studied to determine reasonable parameters for thin films in real applications. Based on above evaluation, the very stable oxides Si_3N_4/SiO_2 (NO) or Al_2O_3 were used in the structure as an insulator layer. Two insulators NO and Al2O3 were formed using LPCVD and atomic layer deposition (ALD) system respectively.

The memory windows of MFIS structures using NO and Al_2O_3 layers under different thickness and annealing conditions are shown in Fig. 4. It is expected that the memory window of MFIS structure increased with decreasing Al_2O_3 layer thickness. The increasing thickness of the layer with a lower dielectric constant induces reduction of the field applied to the ferroelectric which results in the reduction of the hysteretic window width.[12] While the hysteretic window width in the MFIS structure with a 25nm-Al_2O_3 layer was almost constant as annealing temperatures increased, the width in MFIS with a 10nm-Al_2O_3 layer decreased dramatically. The dependence of the memory window on the thickness of the inter-dielectric could be attributed to the formation of an interfacial layer between the ferroelectric and the other layers. A reaction between layers or the diffusion of constituent elements consisting of ferroelectrics and inter-dielectrics can be dominant in MFIS structures with very thin inter-dielectrics when they are annealed at high temperatures. Therefore it is thought that an optimum thickness exists because too thin an insulator cannot prevent reaction between the ferroelectric and Si, which indicates that an optimum thickness may be derived from considering the two opposing effects of larger window width and reduced reaction from inter-diffusion for whichever insulator is used. As shown in Figs. 4, while the hysteresis window in the C-V curves of SBT films deposited on NO structures exists in the zero voltage region, a shift in the hysteresis window to the positive direction on the Al_2O_3 structure was observed. It was also confirmed that SBT deposition and annealing at high temperature generated a large positive-shift in the C-V curves compared to the C-V characteristics of the MIS structure with Pt/Al_2O_3/Si and the MFIS structure (Pt/SBT/Al_2O_3/Si). It may be possible that the SiO_2 layer

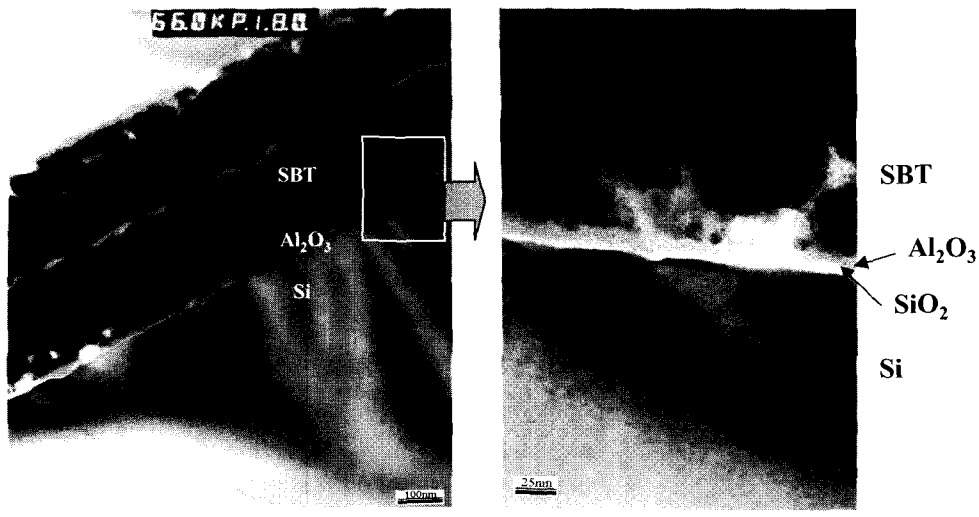

Fig. 6. The TEM images of the interface between SBT films and Al_2O_3/Si displaying SiO_2 formation at the interface. SBT was annealed at 850 °C

is formed at the interface between Al_2O_3 and Si during high temperature annealing in oxygen ambient and that SBT crystallization extracts oxygen from the Al_2O_3 layer, resulting in the generation of oxygen vacancies, which produce electrons. It is well known that the positive shift in flat-band voltage in metal-oxide-semiconductor (MOS) systems results from the negative charge in the oxide layer.[13] The interface trap density around the midgap for the SBT/insulator/Si system is in the range of 10^{11}-10^{12} $(eV \cdot cm^2)^{-1}$. Furthermore, the trap density in the band gap for almost all samples decreases as the energy approaches the midgap.

The TEM morphologies for two different MFIS structures are shown in Figs. 5 and 6. Figure 5 shows TEM images of the MFIS structure (Pt/SBT/NO/Si). The SBT film deposited on the NO structure was annealed 850°C in oxygen ambient. With increasing annealing temperatures, the roughness of the interface was increased, but no significant reaction of SBT films and silicon substrate was detected. However, inter-dielectrics composed of 5nm-SiO_2 displayed a penetration of the grain node in SBT films into the insulator and the silicon, which definitely indicates that thinner layers cannot prevent the interface reaction resulting in an insufficient window.

The microstructures of SBT/Al_2O_3/Si structures were also observed by TEM, and Fig. 6 shows TEM images of a MFIS structure (Pt/SBT/Al_2O_3/Si) whose SBT film was annealed at 850°C in oxygen ambient. The formation of SiO_2 at the interface between Al_2O_3 and Si during high-temperature annealing was confirmed in TEM images. The thickness of the inter-dielectric layer and the roughness were increased as annealing temperature was increased, and the thickness of the inter-dielectric layer between SBT films and Si substrate was increased in the SBT/10nm-Al_2O_3/Si structure shown in Fig.6.

A analysis by SIMS was performed with an O_2^+ primary ion beam, and a low energy (3keV) primary beam was used to improve depth resolution. Figure 7 shows the SIMS depth profiles of SBT films deposited on NO/Si and Al_2O_3/Si structures and annealed at 850°C in oxygen ambient. Inter-diffusion between elements of ferroelectric SBT films and Si in the SIMS depth profiles of SBT films on Al_2O_3/Si structures was found, while the profile of the SBT film on the NO/Si structure has a sharp interface. Because inter-diffusion and an increase in interface roughness in the SBT films prepared on a thin insulator layer such as 10nm-Al_2O_3 at high annealing temperature is observed, the selection of a good insulator and parameter control are required for the use of MFIS-FRAMs.

III. Fabrication of MFISFET device

Source-drain formation and gate module fabrication

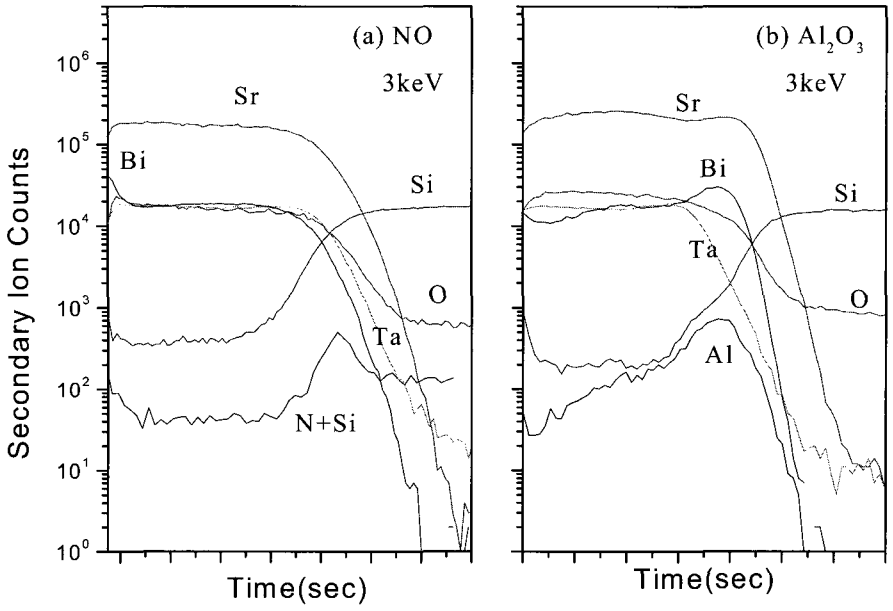

Fig. 7. The SIMS depth profiles of SBT films on (a) NO/Si structure and (b) Al_2O_3/Si structures annealed at 850 °C

are two important processes to fabricate the MFISFET device. Depending on which process proceeds in advance, fabrication scheme divided into self align and non-self align process. In non-self align process source-drain are formed prior to the formation of gate dielectric. Regardless of simpler self-align process, non-self align scheme is a preferred way to fabricate MFISFET device. As conventional FETs need high thermal budgets for diffusion junction the ferroelectric gate dielectric may loose its original characteristics after high temperature thermal cycles during source-drain formation. Also, contamination of gate module can be suppressed by forming source-drain prior to gate dielectric. Also, contamination of gate dielectric during ion implantation can be suppressed by forming source-drain prior to gate dielectric formation.

For the fabrication of MFISFET device, as shown in Fig. 8, we have adapted non-self align process. As we have seen in the previous chapter Si_3N_4/SiO_2 dielectric materials showed stable interface state on silicon surface and were chosen as inter-dielectric insulator in the current MFISFET device. The (100) p-type Si wafer was thermally oxidized to form SiO_2 film and Si_3N_4 thin film was deposited using low pressure chemical vapor deposition (LPCVD) after forming source and drain region at 900°C. SBT thin films were deposited by metal organic decomposition (MOD) spin coating. Top electrode of Pt was then deposited using DC sputtering at 200°C after SBT films were annealed at 800 °C for 30min. in O_2. The resulting Pt/SBT/NO gate module was etched by inductively coupled plasmas(ICP)-reactive ion etcher using metal masks. After etching Pt/SBT/NO gate module, SiO_2 was deposited as an inter-layer-dielectric material using LPCVD at 380°C. TiW layers were deposited for metallization and all the lithography processes on the back-end process was made by contact aligner. The structure of fabricated device is shown briefly in Fig. 8.

After fabrication of MFISFET cross section of the device was analyzed by scanning electron microscopy. Figure 9 shows that the cross section of MFISFET(Width/length of gate=10/3μm) structure. Actual the gate length is 3μm. The distance between gate module and metal contact area was intentionally enlarged to make the process easier. Source and drain region was made by non-self alignment structure before the gate was formed. The Pt/SBT/NO gate module is formed conformably with an interlayer dielectric of SiO_2 film.

Drain current (I_D) – Gate voltage(V_G) characteristics were measured with HP4156B semiconductor parameter analyzer. Figure 10 shows I_D-V_G characteristics of n-

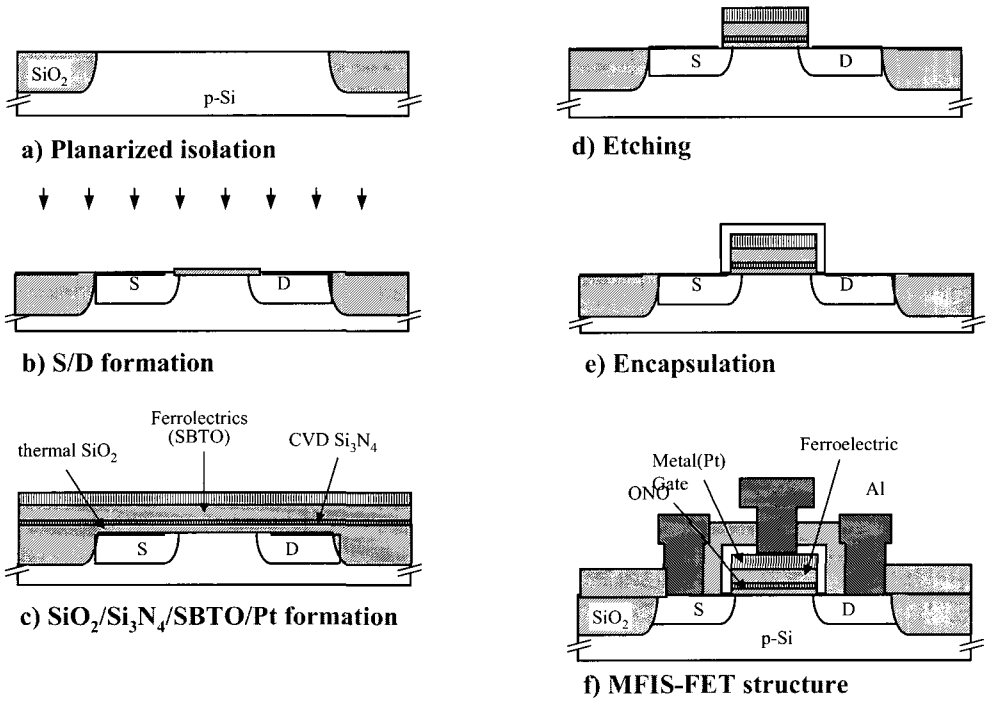

Fig. 8. Process flow of MFISFET device using non-self aligned scheme.

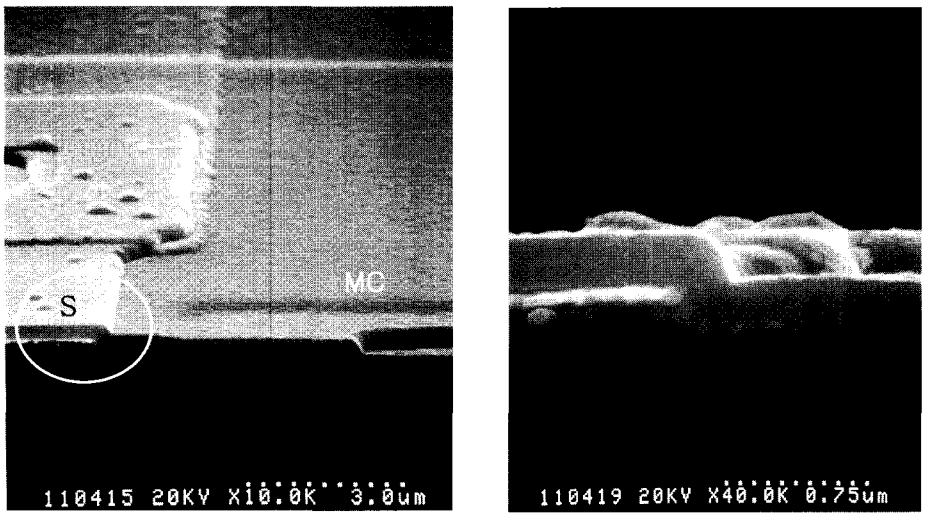

Fig. 9. Cross sectional images of MFISFET (a) Overall image of MFISFET (b) Enlarged image of S region.

channel MFISFET and p-channel MFISFET having the various NO films. In Fig. 10(a), hysteresis loops were obtained with a counter-clockwise trace as indicated by the arrow by sweeping V_G from –15V to +15V. These hysteresis behaviors are the ferroelectric nature of SBT films. Memory window of MFISFET varies with the thickness of NO films. When the thickness of NO film is 30/50Å, memory window is less than 0.2V, which indicates that the thickness of NO films is too thin to play a role as a buffer layer. Memory window increases up to about 2.0V as the thickness of NO film is 50/50Å but decreases as the thickness of NO film is 60/50Å. As silicon nitride is thicker, silicon nitride film may stress SiO_2 film so that the interface between SiO_2 and Si substrate becomes unstable, which results in degrading the memory window characteristics. we also found

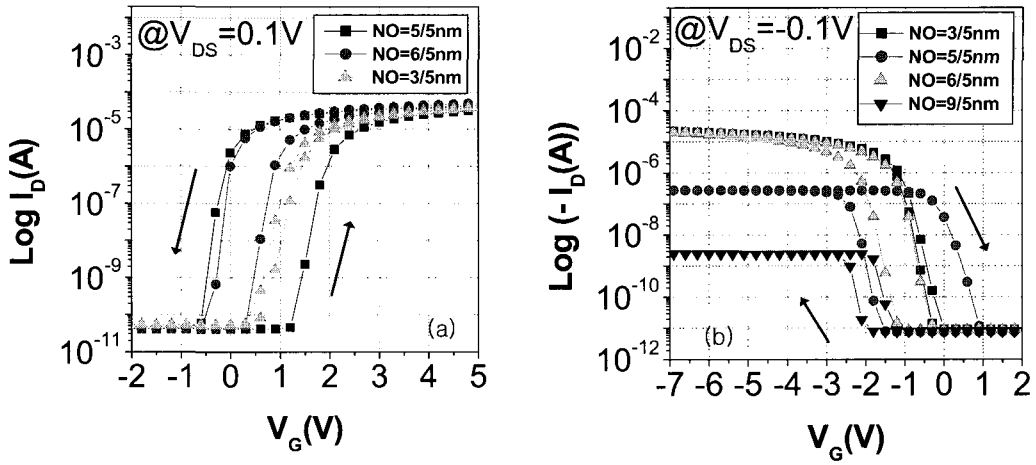

Fig. 10. ID-VG characteristics of n-channel(a) and p-channel(b) MFISFET having various thickness of NO films.

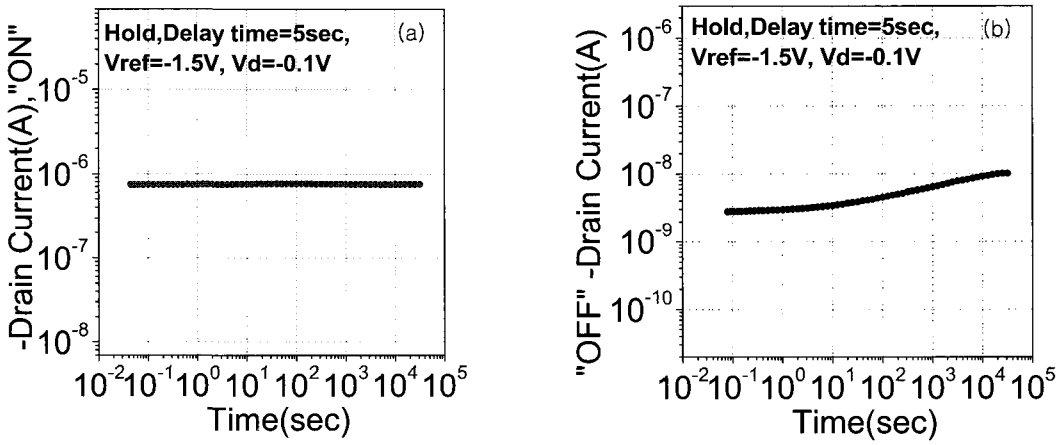

Fig. 11. Data retention characteristics of p-channel MFISFET.

similar phenomenon in I_D-V_G memory window characteristics of p-channel MFIS-FET as shown in fig.10 (b).

To check the reliability of MFISFET device data retention test was performed using HP4156B. In the figure 11, the reference voltage for the 'write' of the MFISFET was –1.5 V. The gate was written by rectangular pulse of –15V with the width of 5 seconds. After writing the gate, I_{ON} and I_{OFF} were read with the reference voltage of –1.5V. I_{ON} was retained up to $4x10^4$ seconds. It holds more than 90% of the initial data after the retention time period, while I_{OFF} degraded as the retention time increased. After the retention time of 10^3 seconds the device still hold the difference of I_{ON} and I_{OFF} data by more than 100 times, which indicates the existence of physically induced charge by ferroelectric polarization.

IV. Cell Addressing Schemes for MFIS-FET Arrays

So far, we have discussed about single FET device with ferroelectric gate material. In this chapter, we propose cell addressing scheme for MFIS-FET arrays. The major problem of one-transistor-type FRAM is selection of single cell during write operations because we have no additional switch for individual cell [14,15].

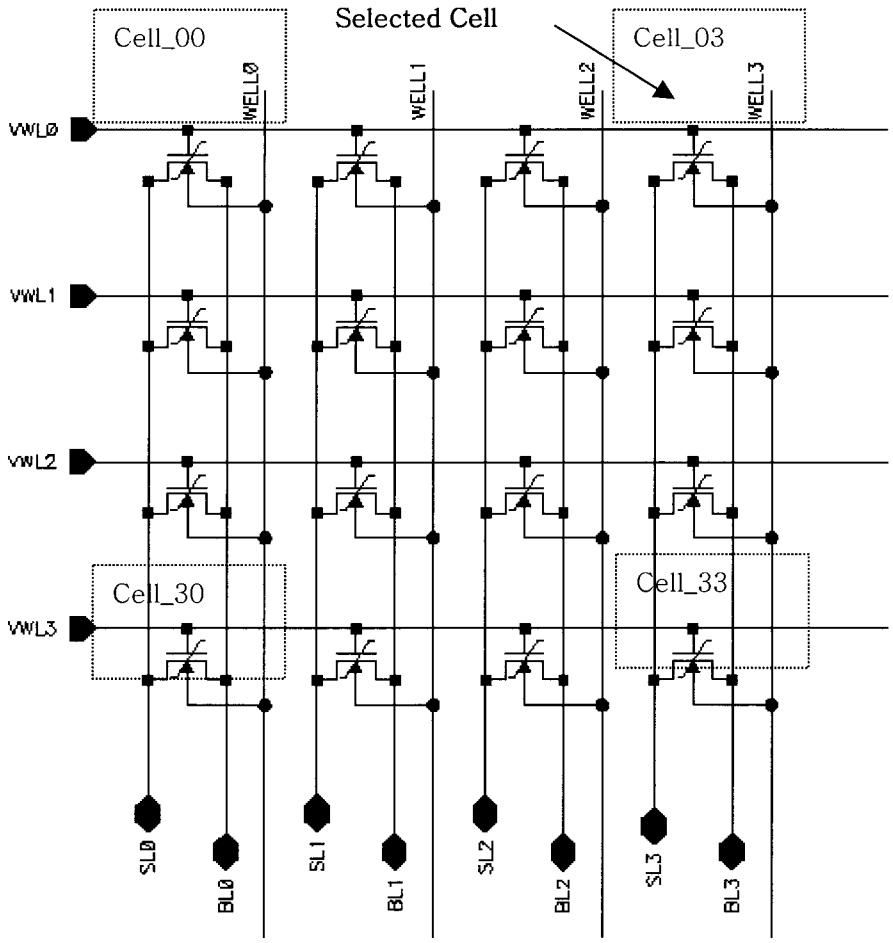

Fig. 12. Equivalent circuit of a 4x4 array of the proposed single FRAM with floating well structures.

To overcome this restriction, each well is isolated from adjacent columns, hence, the well bias can be controlled individually and can be floating state. The cells in a same column are placed on the same well and the cells driven by same WL are consisted a raw of array as shown in Fig.12.

To write state of "0" to a selected cell, a program voltage "-VPG" is applied to the selected WL, and the potential of well, SL and BL in the selected column are biased to ground, while all unselected WLs, wells, SLs and BLs are floated. Then the voltage difference across gate and channel of the selected cell is "–VPG". On the other hand, the potentials of wells and WLs of unselected cells are determined by the voltage sharing between parasitic gate and well capacitance. Writing state of "1" is performed by similar manner as shown in Fig. 13. The program voltage "-VPG" is applied to well, SL and BL in the selected column, and selected WL is biased to ground, while all unselected WLs, wells, SLs and BLs are floated. Then the voltage difference across gate and channel of the selected cell is "VPG", but, the electrode potential of a unselected cell is determined by the voltage sharing between gate capacitance and well parasitic capacitance. During the read operation, the read voltage VRG (about 1.2 volt) and VBR is applied to selected WL and BL, respectively.

There are a few remaining issues of this proposed structure. The first is successful fabrication of MFSFETs and memory array because deposition of ferroelectric thin films on silicon substrate has several known physical problems not solve until now. Also, adapting the device technologies to reduce parasitic well capacitance of bulk MOSFET is unclear. An SOI structured MFSFET may be a possible solution.

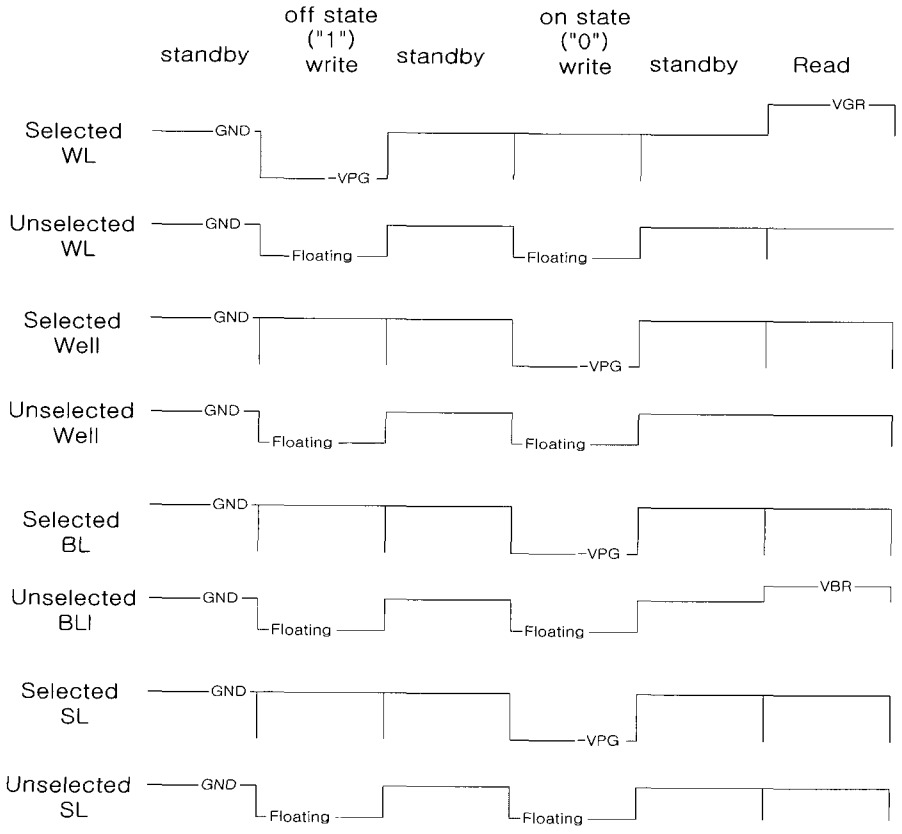

Fig. 13. The wave forms for write and read operations to selected and unselected cells.

V. CONCLUSIONS

There are still many obstacles remained to realize a single transistor type ferroelectric random access memory. In this paer we have discussed about current situation of MFISFET-type memory; i.e., issues about ferroelectric material itself, interfacial control of ferroelectric thin films on insulator material, and selection of appropriate insulator layers. As a conclusion, key technologies to realize MFISFET memory are firstly, to minimize interfacial interaction during process between ferroelectric thin films to insulator layer and insulator layer to silicon substrate. Failure of controlling interfacial phenomena leads to device malfunctioning, secondly, selection (which includes engineering of ferroelectric thin films for more stable process conditions) of ferroelectric thin films and insulator layers. In addition to polarization characteristics of ferroelectric material the matching dielectric characteristics of the insulator layer is one of the most important feature to maximize functionality of MFISFET devices. Lastly, yet very important to realize MFISFET device as a memory array, developing circuit architecture to minimize cell disturbance and loss of stored data is another goal to be achieved for integrated circuit operation.

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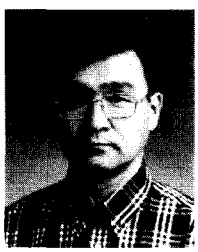

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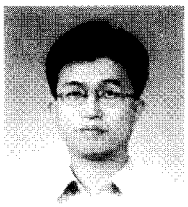
He joined ETRI in 2000 as a senior researcher in the Advanced Micro-electronics Technology lab. His special interests is application of ferroelectric thin films on memory devices and infrared ray detecting devices.

Sung-Min Yoon Dr. Yoon was born in Seoul, Korea in 1970. He received the B.S. in Department of Inorganic Material Engineering from Seoul Nati onal University, Seoul, Korea, 1995, the M.S. and Ph.D. in Department of Applied Electronics from Tokyo Instit ute of Technology (TIT), Tokyo, Jap an, 1997 and 2000, respectively. His Ph.D. work focused on the fabrication of an adaptive-learning neuron-chip using ferroelectric memory device. He was with Frontier Collabo rative Research Center, TIT as a Research Fellow of Rese arch & Development Association for Future Electron Devices (FED), Japan, from 2000 to 2001. Currently, he is a Senior Research Engineer at Electronics and Telecommunications Research Institute (ETRI), Korea. His research interests include the characterization of ferroelectric and insulator thin films, device physics and process technologies for functional nano-devices.

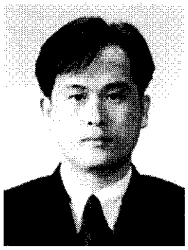
He is a member of the Japan Society of Applied Physics.

He was awarded the Japan Society of Applied Physics Award for Research Paper Presentation in 1999, the Teshi ma Prize in 1999, and SSDM Young Researcher Award in 1999.

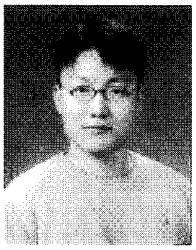


Seong M. Cho Dr. Cho received the B.S., M.S., and Ph.D. Degree in Materials Engineering from Pohang University of Science and Technology (POSTECH), Korea, in 1992, 1994, and 2001, respectively. After getting M.S. Degree, he had joined Samsung Electronics, Korea, in 1994, where he had worked for the development of lithography technology for 256M and 1G DRAM until 1996.

He joined ETRI in 2001 as a senior researcher in the Advanced Micro-electronics Technology laboratory. Now, his research interests are mainly focused on the device applications of ferroelectric thin films such as IR detector, ferroelectric random access memory (FRAM) etc.



Woong-Chul Shin Dr. Shin received the B.S., M.S., and Ph.D. degrees all in materials Engineering from Chungnam National University, Daejon, Korea, in 1996, 1998, and 2002, respectively. His doctoral research was engaged in the researches on characteristics of ferroelectric thin films by MOCVD for FRAM applications. He is now a Postdoctoral Research Fellow at the Basic Research Laboratory in Electronics and Telecommunications Research Institute(ETRI), Korea, where he has been working on the development of ALD process and process integration of FeRAM's. His current research interests include device and process technologies in FRAM's, and Nano device Technologies.



Nam-Yeal Lee Mr. Lee received his B.S. Degree from Department of Semiconductor Engineering in Cheongju university in 1999 and the M.S. degrees from the graduate school of Cheongju university in 2001, where he did many Research works for the FeRAM devices using the ferroelectrics materials. Now, he work as a Research Engineer in the Basic Research Laboratory., Multi-Functional Device Team, ETRI