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Conformal Al_2O_3 Nanocoating of Semiconductor Nanowires by Atomic Layer Deposition

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Abstract - Various semiconductor nanowires such as GaN, GaP, InP, Si_3N_4, SiO_2/Si, and SiC were coated conformally with aluminum oxide (Al_2O_3) layers by atomic layer deposition (ALD) using trimethylaluminum (TMA) and distilled water (H_2O) at a temperature of 200°C. Transmission electron microscopy (TEM) revealed that Al_2O_3 cylindrical shells conformally coat the semiconductor nanowires. This study suggests that the ALD of Al_2O_3 on nanowires is a promising method for preparing cylindrical dielectric shells for coaxially gated nanowire field-effect transistors.

Keywords: nanowire, atomic layer deposition (ALD), Al_2O_3 coating

1. Introduction

A variety of semiconductor nanowires have been investigated due to their great potential in the application of optical and electronic devices [1, 2]. To realize the optical and electronic devices utilizing semiconductor nanowires, protection of the nanowires from oxidation, nitrification, and wetting is crucial; in ambient air, the surface of Si nanowires are oxidized to form SiO_2 layers surrounding themselves and GaP nanowires are nitrified [3]. Coating of semiconductor nanowires is therefore required to retain their optical, electrical, and physical properties.

Aluminum oxide (Al_2O_3) exhibits many excellent electrical and optical properties including high dielectric constant, very low permeability of alkali ions, high thermal conductivity, and transparency over a wide range of wavelengths [4–6]. Due to these characteristic properties, extensive attempts have been made to utilize Al_2O_3 in the fields of capacitor dielectrics and gate oxides in memory devices, insulating layers in electroluminescent display devices, waveguide, and corrosion-resistant coating films on metals [7]. More recently, Al_2O_3 barrier layers deposited on Si by atomic layer deposition (ALD) technique have been investigated to study electrical and reliability characteristics of $Si/Al_2O_3/Si$ capacitor structures for the future application of DRAM [8–10].

Lieber's group has recently realized the fabrication of a coaxially gated nanowire field-effect transistor (FET) [11]. The coaxially gated nanowire FET has drawn much attention due to its capacitance enhancement compared to planar gates utilized for nanowire FETs. In this FET, the active channel is a Ge shell and the gate dielectric is a SiOx shell. The concept of the coaxially gated nanowire FET is applicable to other semiconductor nanowires. For the fabrication of the coaxially gated nanowire FETs using other semiconductor nanowires including GaN, GaP, InP, Si_3N_4, SiO_2/Si, SiC, and ZnO semiconductor nanowires, the cylindrical gate dielectrics should be formed on these nanowires; for the SiO_2/Si nanowire, the SiO_2 shell also could be a cylindrical gate dielectric. The motive of this study is therefore to suggest a straightforward method for the formation of the cylindrical dielectric with a dielectric constant higher than SiO_2 on any of semiconductor nanowires; dielectric constant is 3.9 and 10.5–12 for SiO2 and Al_2O_3, respectively.

In this study, GaN, GaP, InP, Si_3N_4, SiO_2/Si, SiC, and ZnO semiconductor nanowires were first synthesized by a variety of growth methods and then deposited conformally with Al_2O_3 by ALD. The structural and chemical properties of the deposited Al_2O_3 were investigated by transmission electron microscopy (TEM), selected area electron diffraction (SAED) pattern, and energy-dispersive X-ray (EDX) spectroscopy. In this paper, the experimental results of the Al_2O_3-deposited GaN semiconductor nanowires are described in detail as a representative case and other Al_2O_3-deposited nanowires are briefly described and compared.

2. Experimetal procedure

Semiconductor nanowires have been synthesized using a variety of growth methods. The synthesis procedures of the GaN, GaP, SiC, and ZnO nanowires are briefly described as follows. (1) GaN nanowires were synthesized from Fe nanoparticles deposited on a Si substrate during the evapo-

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ration from a mixture of Ga and GaN powders at temperatures of 950–1100°C [12]. (2) GaP nanowires were prepared from the evaporation of ball-milled GaP powders at 1100°C. They were grown on an Ni nanoparticles-deposited alumina substrate at a temperature of 900°C [3]. (3) SiC nanowires were synthesized from the reaction of a Si (100) wafer with a mixture of Ga and GaN powders at a temperature of 1100°C under a flow of the CH_4 (99.95%) and H_2 (99.999%) mixture [13]. (4) ZnO nanowires were formed on an Si substrate from the evaporation of ball-milled ZnO powders at 1380℃ for three hours while Ar was flown into the chamber at a rate of 500 sccm [14]. The detailed synthetic procedures of the InP, Si_3N_4, and SiO_2/Si nanowires will be reported elsewhere.

Al_2O_3 was deposited on the synthesized semiconductor nanowires at a growth temperature of 200℃ using the ALD technique. Trimethylaluminum (TMA) and distilled water were utilized as precursors for deposition [4]. The process pressure was 250 and 230 mTorr for the dosing of chemical precursors and the Ar purging, respectively. Precursor elements must be alternately dosed to the semiconductor nanowires. The dosing time and purging time were 1 and 20 sec, respectively. 100 process cycles were performed for the deposition of Al_2O_3; one cycle of the deposition of Al_2O_3 consists of TMA dosing, Ar purging, H_2O dosing, and Ar purging. TEM images, EDX spectra, and SAED patterns of the semiconductor nanowires were taken by transmission electron microscopy (TEM, Philips CM30) or high-resolution transmission electron microscopy (HRTEM, JEOL JEM-2010).

3. Results and discussion

Fig 1 is a TEM image of a nanowire selected from GaN nanowires grown on an Si (100) substrate; its diameter and length are 60 nm and 20 ㎛, respectively. The XRD pattern taken for the GaN nanowires showed that its lattice structure is wurtzite (not shown here). The SAED pattern in the inlet of Fig. 1 indicates that the growth direction of the GaN nanowire is parallel to the [0001] lattice direction. Fig 2 is a TEM image of a selected GaN nanowire deposited with Al_2O_3 by ALD; the Al_2O_3 shell is marked by the arrows. The TEM image illustrates that an Al_2O_3 shell with the cap surrounds the GaN nanowire. The Al_2O_3 shell is 20 nm in thickness; its thickness is substantially uniform along the nanowire. The inset of Fig. 2 shows the SAED pattern of the Al_2O_3-deposited GaN nanowire. This pattern shows the halo overlapped with a set of single-crystal electron diffraction spots, while that of the bare GaN nanowire shows only the spots (see the inset of Fig. 1).

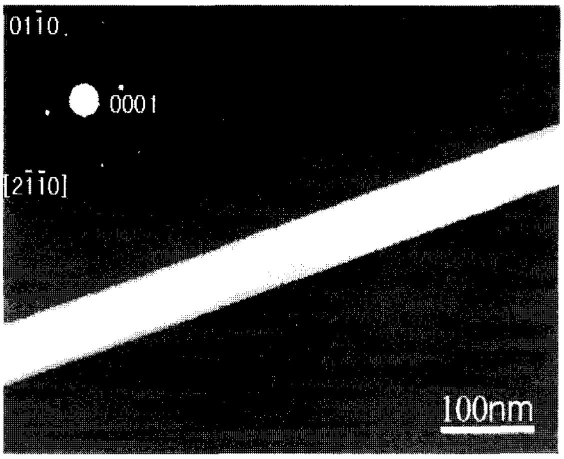

Fig. 1 TEM image of a selected GaN nanowire grown on a Si (100) substrate. The SAED pattern in the inlet indicates that the growth direction is parallel to the [0001] lattice direction.

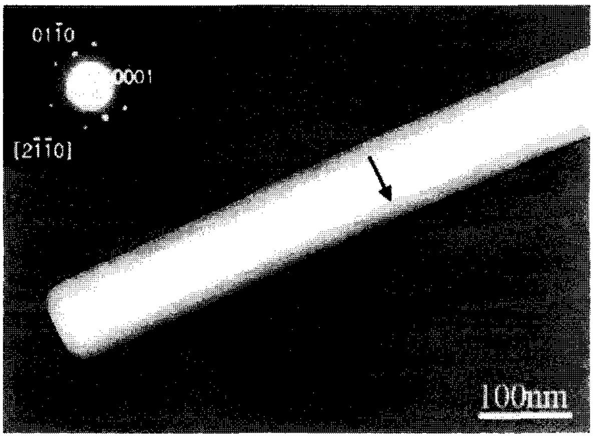

Fig. 2 TEM image of a selected GaN nanowire coated with Al_2O_3 by ALD. The Al_2O_3 shell is marked with an arrow. In the inset, the SAED pattern shows a halo overlapped with the single-crystal electron diffraction spots.

The presence of the halo in the SAED pattern indicates that Al_2O_3 deposited on GaN nanowire is amorphous. Fig 3 shows the representative EDX spectra taken from a (a) bare and (b) Al_2O_3-deposited GaN nanowires. The EDX spectrum taken from the Al_2O_3-deposited GaN nanowire exhibits Al- and O-related peaks, indicating that the deposited part is indeed Al_2O_3; the Cu-related peak is due to the presence of Cu grids. The TEM, SAED, and EDX illustrate that the GaN nanowire is deposited cylindrically with amorphous Al_2O_3 material.

The lattice structures, lattice constants, growth directions, and diameters (or thicknesses) of the semiconductor nanowires and Al_2O_3 shells are summarized in Table 1. Fig 4 shows TEM images of GaP, InP, Si_3N_4, SiO_2/Si, SiC, and ZnO nanowires deposited with Al_2O_3 by ALD; the Al_2O_3 shells are marked by arrows. The TEM images of the deposited nanowires illustrate that the cylindrical Al_2O_3

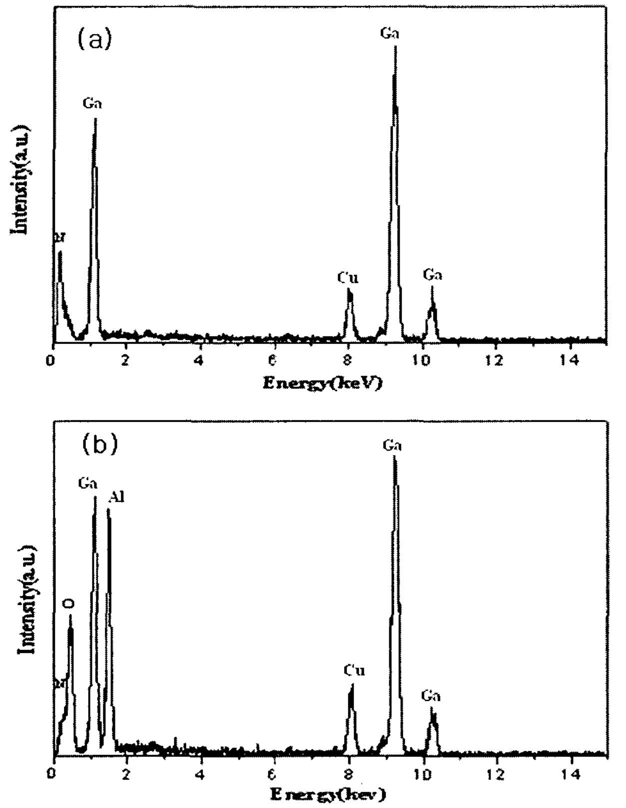

Fig. 3 EDX spectra taken from (a) bare and (b) Al_2O_3-deposited GaN nanowires.

shells surround conformally the six different semiconductor nanowires, as observed for the Al_2O_3-coated GaN nanowire. For these Al_2O_3–coated nanowires, the Al_2O_3 shells are 20 nm in thickness. The cross sections of the cylindrical shells surrounding the GaP, InP, Si_3N_4, SiO_2/Si, SiC, and ZnO nanowires are circular. The thicknesses of the Al_2O_3 shells are uniform along the nanowires. This observation reveals that these six different semiconductor nanowires all are deposited conformally with Al_2O_3. SAED patterns of these six different nanowires coated by Al_2O_3 showed the halo patterns that are the same as for the Al_2O_3-deposited GaN nanowire, indicating that the Al_2O_3 shells on all the semiconductor nanowires are amorphous. The deposition of the amorphous Al_2O_3 on semiconductor nanowires by ALD is associated with the relatively low growth temperature (200°C); Iizuka et al. report that growth temperatures above 800°C are required to obtain the crystalline Al_2O_3 layers [15].

The thicknesses of Al_2O_3 coating shells (on the seven different semiconductor nanowires) prepared with five different cycles were precisely measured by TEM. The thicknesses of the Al_2O_3 shells for each of the five different cycles are the same for all semiconductor nanowires.

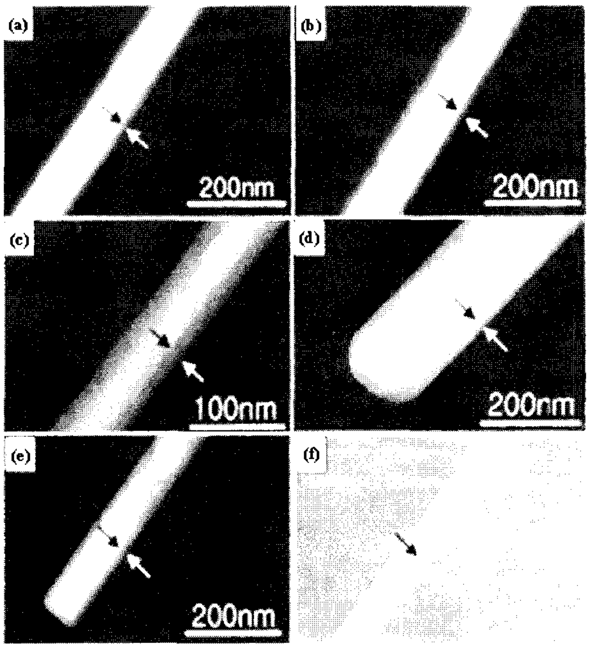

Fig. 4 TEM images of (a) GaP, (b) InP, (c) Si_3N_4, (d) SiO_2/Si, (e) SiC, and (f) ZnO (f) nanowires deposited with Al_2O_3 using ALD. The Al_2O_3 shells are marked by arrows.

The deposition rate of the Al_2O_3 coating may be determined to be 0.20 nm/cycle. This value agrees with the growth rate for flat Si surfaces [4]. These indicate that the growth rate of the Al_2O_3 nano-shells deposited by ALD does not depend on the kind of semiconductor material as well as crystal structure. Moreover, the thickness of a Al_2O_3 coating layer is substantially uniform for semiconductor nanowires having different chemical components, different lattice structures, and different lattice constants (see the details in Table 1). The excellent uniformity is due to the amorphous properties of the Al_2O_3 coating material and its excellent sticking capability. If the Al_2O_3 coating layer is not amorphous, the thickness of the Al_2O_3 coating layer

Table 1 Characteristics of semiconductor nanowires and Al_2O_3.

Material	Lattice structure*	Lattice constant (¨)	Growth direction	Diameter (D) or thickness (T) (nm)
GaN	W	a=3.190 , c=5.189	[0001]	60(D)
GaP	Z	a=5.451	[111]	140(D)
InP	Z	a=5.861	[111]	50(D)
Si_3N_4	W	a=7.754 , c=5.622	$[2\bar{1}\bar{1}0]$	40(D)
SiO_2	A	-	-	50(T)
Si	D	a=5.392	[111]	40(D)
SiC	Z (3C)	a=4.359	[111]	65(D)
ZnO	W	a=3.250, c=5.205	$[11\bar{2}0]$	20(D)
Al_2O_3	A	-	-	20(T)

*wurtzite (W), zinc blende (Z), amorphous (A), and diamond (D) would depend on the structural and compositional properties and therefore would be nonuniform. For instance, the TiO_2 and ZnO films deposited by ALD are microcrystalline and these deposited layers are nonuniform on the nanometer scale [16–18]. The uniform thickness observed for all the nanowires also reveals the excellent sticking capability of the Al_2O_3 material, which our observation indicates is independent of semiconductor substances.

5. Conclusion

GaN, GaP, InP, Si_3N_4, SiO_2/Si, SiC, and ZnO semiconductor nanowires were deposited cylindrically with amorphous Al_2O_3 via ALD. TEM images and SAED patterns of the deposited semiconductor nanowires reveal that 20 nm-thick Al_2O_3 cylindrical shells surround the semiconductor nanowires. Comparison of these Al_2O_3 shells deposited on the seven different semiconductor nanowires illustrates that the crystal structure and chemical components of the shells deposited by ALD using TMA and distilled water are independent of the chemical component, lattice structure, and growth direction of the nanowire. Our study shows that the ALD has an excellent capability to deposit Al_2O_3 cylindrically on any semiconductor nanowires, suggesting that the ALD of Al_2O_3 on nanowires is a promising methods to prepare cylindrical dielectric shells in coaxially gated nanowire field-effect transistors.

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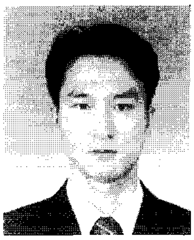

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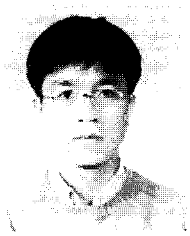

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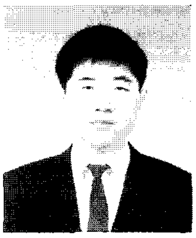

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