Dielectric property and conduction mechanism of ultrathin zirconium oxide films

J.P. Chang; Y.S. Lin

Dept. of Chemical Engineering, University of California, Los Angeles, California 90095

Stoichiometric, uniform, amorphous ZrO$_2$ films with an equivalent oxide thickness of ~1.5nm and a dielectric constant of ~18 were deposited by an atomic layer controlled deposition process on silicon for potential application in metal-oxide-semiconductor (MOS) devices. The conduction mechanism is identified as Schottky emission at low electric fields and as Poole-Frenkel emission at high electric fields. The MOS devices showed low leakage current, small hysteresis (<5mV), and low interface state density (~2x10$^{11}$/cm$^2$/V). Microdiffraction and high-resolution transmission electron microscopy showed a localized monoclinic phase of α-ZrO$_2$ and an amorphous interfacial ZrSiO$_4$ layer which has a corresponding dielectric constant of 11.


High-k dielectrics by UV photo-assisted chemical vapour deposition

Q. Fang; J.Y. Zhang; Z.M. Wang; G. He; J. Yu; Ian W. Boyd

Dept. Electronic & Electrical Engineering, University College London, Torrington Place, London UK

An overview of our recent work on thin films of metal oxides deposited on silicon by a novel excimer lamp-assisted ultraviolet injection liquid source CVD (UVILS-CVD) process for advanced high-k gate dielectrics applications will be presented. Recent results on TiO$_x$, Ta$_2$O$_5$, ZrO$_2$, HfO$_2$, and TiO$_2$-doped Ta$_2$O$_5$ will be demonstrated. The physical, structural, interfacial

Berkeley, California 94720
properties and electrical characterization of the as-deposited and UV-annealed new high dielectric constant (high-k) materials, determined using ellipsometry, Fourier transform infrared spectroscopy, X-ray photoelectron spectroscopy, UV spectrophotometry, SEM, TEM, and C-V, I-V measurements, showed that good quality layers could be produced. The investigation of high-k dielectrics grown by the UVILS-CVD process clearly demonstrates that low cost, high power density excimer lamp systems can provide an interesting alternative to conventional UV lamps and excimer lasers for industrial large-scale low temperature materials processing. UVILS-CVD is a promising technique for the controlled deposition of ultra thin high-k metal-oxide dielectrics for deep sub-micron CMOS devices at temperatures as low as 350°C.

출처
Microelectronic Engineering, Volume:1 2002 000-000

논문제목
Annealing Effects On Ultra thin MOS Capacitors

저자
Alvin Chi-hai Ng, Jun Xu, J. B. Xu, W. Y. Cheung

소속
Dept. of Electronic Engineering, Chinese university of Hong Kong, Shatin, the New Territories, Hong Kong

초록
Silicon oxide with thickness less than 9 nm is fabricated by tube furnace oxidation. Nitrogen is added to dilute the oxidation rate. Aluminum dots with radius of 0.05 cm are deposited on the oxide. High frequency capacitance-voltage (HF C-V), conductance-voltage (G-V) and current-voltage (I-V) characteristics are measured. Annealing under nitrogen atmosphere is carried out with different time and at different temperatures. Densities of the interface states before and after annealing are compared. After annealing, a decrease in density of the interface states is found. Experiments show that 450°C annealing for 30 minutes has the lowest density of the interface states.

출처

논문제목
Effective electron mobility in Si inversion in metal-oxide-semiconductor systems with a high-k insulator: The role of remote phonon scattering
저자
Massimo V. Fischetti, Deborah A. Neumayers, and Eduard A. Cardier

소속
IBM Research Division, Thomas J. Watson Research Center, P.O. Box 218 Yorktown Heights, New York 10598

초록
The high dielectric constant of insulators currently investigated as alternatives to SiO₂ in metal-oxide-semiconductor structures is due to their large ionic polarizability. This is usually accompanied by the presence of soft optical phonons. We show that the long-range dipole field associated with the interface excitations resulting from these modes and from their coupling with surface plasmons, while small in the case of SiO₂, for most high-k materials causes a reduction of the effective electron mobility in the inversion layer of the Si substrate. We study the dispersion of the interfacial coupled phonon-plasmon modes, their electron-scattering strength, and their effect on the electron mobility for Si-gate structures employing films of SiO₂, Al₂O₃, AlN, ZrO₂, HfO₂, and ZrSiO₅ for “SiO₂-equivalent” thickness ranging from 5 to 0.5 nm.

출처

논문제목
Epitaxial growth of yttrium-stabilized HfO₂ high-k gate dielectric thin films on Si

저자

소속
Dept. of Applied Physics, The Hong Kong Polytechnic University, Hong Kong, China

초록
Epitaxial yttrium-stabilized HfO₂ thin films were deposited on p-type (100) Si substrates by pulsed laser deposition at a relatively lower substrate temperature of 550 °C. Transmission electron microscopy observation revealed a fixed orientation relationship between the epitaxial film and Si; that is, (100)Si//(100)HfO₂ and [001]Si//[001]HfO₂. The film/Si interface is not atomically flat, suggesting possible interfacial reaction and diffusion. X-ray photoelectron spectrum analysis also revealed the interfacial reaction and diffusion evidenced by Hf silicate and Hf-Si bond formation at the interface. The epitaxial growth of the yttrium stabilized HfO₂ thin film on bare Si is via a direct growth
mechanism without involving the reaction between HF atoms and SiO\textsubscript{2} layer. High-frequency capacitance-voltage measurement on an as-grown 40-A yttrium-stabilized HfO\textsubscript{2} epitaxial film yielded an effective dielectric constant of about 14 and equivalent oxide thickness to SiO\textsubscript{2} of 12 A. The leakage current density is 7.0 × 10e-2 A/cm\textsuperscript{2} at 1 V gate bias voltage.

- 출처

- 논문제목
  Basic characteristics of metal-ferroelectric-insulator-semiconductor structure using a high-k Pr\textsubscript{0.7}O\textsubscript{3} insulator layer

- 저자
  Minoru Noda, Kazushi Kodama, Satoshi Kitai, Mitsue Takahashi, Takehsi Kanashima, and Masanori Okuyama

- 소속
  Area of Materials and Device Physics, Department of Physical Science, Graduate School of Engineering Science, Osaka University, 1-3 Machikaneyama-Cho, Toyonaka, Osaka, 560-8531, Japan

- 초록
  A metal-ferroelectric [Sr\textsubscript{1-x}Bi\textsubscript{x}Ta\textsubscript{2}O\textsubscript{6} (SBT)]-high-k-insulator(Pr\textsubscript{0.7}O\textsubscript{3})-semiconductor(Si) structure has been fabricated and evaluated as a key part of metal-ferroelectric-insulator-semiconductor-field-effect-transistor MFIS-FET memory, aiming to improve the memory retention characteristics by increasing the dielectric constant in the insulator layer and suppressing the depolarization field in the SBT layer. A 20-nm Pr\textsubscript{0.7}O\textsubscript{3} film grown on Si(100) showed both a high of about 12 and a low leakage current density of less than 1 × 10e-8 A/cm\textsuperscript{2} at 1.5 MV/cm. A 400-nm SBT film prepared on Pr\textsubscript{0.7}O\textsubscript{3}/Si shows a preferentially oriented (103) crystalline structure, grain size of about 130 nm and surface roughness of 3.2 nm. A capacitance-voltage hysteresis is confirmed on the Pt/SBT/Pr\textsubscript{0.7}O\textsubscript{3}/Si diode with a memory window of 0.3 V at a sweep voltage width of 12 V. The memory retention time was about 1.104 s, comparable to the conventional Pt/SBT/SiO\textsubscript{2}N\textsubscript{2}/Si. The gradual change of the capacitance indicates that some memory degradation mechanism is different from that in the Pt/SBT/SiON/Si structure.

- 출처
  Journal of Applied Physics, Volume:93 Issue:7 April 2003 Page(s): 4137-4143

- 논문제목
  Atomic layer chemical vapor deposition of ZrO\textsubscript{2}-based dielectric films: Nanostructure and nanochemistry

- 저자
  S. K. Dey

- 소속
  Chemical and Materials Engineering, and Electrical Engineering, Arizona State University, Tempe, Arizona 85287-6006

- 초록
  A 4 nm layer of ZrO\textsubscript{2} (targeted x=2) was deposited on an interfacial layer (IL) of native oxide (SiO\textsubscript{2}, t=1.2 nm) surface on 200 nm Si wafers by a manufacturable atomic layer chemical vapor deposition technique at 300°C. Some as-deposited layers were subjected to a post-deposition, rapid thermal annealing at 700°C for 5 min in flowing oxygen at atmospheric pressure. The experimental x-ray diffraction, x-ray photoelectron spectroscopy, high-resolution transmission electron microscopy, and high-resolution parallel electron energy loss spectroscopy results showed that a multiphase and heterogeneous structure evolved, which we call the Zr-O/IL/Si stack. The as-deposited Zr-O layer was amorphous ZrO\textsubscript{2}-rich Zr silicate containing about 15% by volume of embedded ZrO\textsubscript{2} nanocrystals, which transformed to a glass nanoceramic (with over 90% by volume of predominantly tetragonal-ZrO\textsubscript{2} (t-ZrO\textsubscript{2}) and monoclinic-ZrO\textsubscript{2} (m-ZrO\textsubscript{2}) nanocrystals) upon annealing. The formation of disordered amorphous regions within some of the nanocrystals, as well as crystalline regions with defects, probably gave rise to lattice strains and deformations. The interfacial layer (IL) was
partitioned into an upper SiO$_2$-rich Zr silicate and the lower SiO$_2$. The latter was sub-toxicometrical and the average oxidation state increased from Si0.85 in SiO$_{20}$ as-deposited to Si1.32 in SiO$_{20}$ (annealed). This high oxygen deficiency in SiO$_2$ was indicative of the low mobility of oxidizing specie in the Zr-O layer. The stacks were characterized for their dielectric properties in the Pt/(Zr-O/IL)/Si metal oxide-semiconductor capacitor (MOSCAP) configuration. The measured equivalent oxide thickness (EOT) was not consistent with the calculated EOT using a bilayer model of ZrO$_2$ and SiO$_2$, and the capacitance in accumulation (and therefore, EOT and kZr-O) was frequency dispersive, trends well documented in literature. This behavior is qualitatively explained in terms of the multi-layer nanostructure and nanochemistry that evolves.

- 출처
  Journal of Applied Physics, Volume:93 Issue:7 April 2003
  Page(s): 4144-4157

- 논문제목
  Interfacial properties of ZrO$_2$ on silicon

- 저자
  Y.-S. Lin, R. Puthenkovilakam, and J. P. Chang

- 소속
  Dept. of Chem. Engineering, University of California, Los Angeles, California

- 초록
  The interface of zirconium oxide thin films on silicon is analyzed in detail for their potential applications in the microelectronics. The formation of an interfacial layer of ZrSiO$_2$ with graded Zr concentration is observed by the x-ray photoelectron spectroscopy and secondary ion mass spectrometry analysis. The as-deposited ZrO$_2$/ZrSiO$_2$/Si sample is thermally stable up to 880°C, but is less stable compared to the ZrO$_2$/SiO$_2$/Si samples. Post-deposition annealing in oxygen or ammonia improved the thermal stability of as-deposited ZrO$_2$/ZrSiO$_2$/Si to 925°C, likely due to the oxidation/nitridation of the interface. The as-deposited film had an equivalent oxide thickness of ~1.3 nm with a dielectric constant of ~21 and a leakage current of 3.2 x 10e-3 A/cm$^2$ at 1.5 V. Upon oxygen or ammonia annealing, the formation of SiO$_2$ and SiH$_4$NO at the interface reduced the overall dielectric constants.

- 출처
  Journal of Applied Physics, Volume:93 Issue:10 May 2003
  Page(s): 5945-5952

- 논문제목
  Dielectric properties of Pr$_2$O$_3$ high-k films grown by metalorganic chemical vapor deposition on silicon

- 저자
  Raffaella Lo Nigro, Vito Raineri, and Corrado Bongiorno

- 소속
  IMM, sezione di Catania, CNR, Stradale Primosole n 50, 95121 Catania, Italy

- 초록
  Praseodymium oxide (Pr$_2$O$_3$) thin films have been deposited on Si(100) substrates by metalorganic chemical vapor deposition using praseodymium tris-2,2,6,6-tetramethyl-3,5-heptandionate as source material. Film structural, morphological, and compositional characterizations have been carried out. Dielectric properties have been studied as well by capacitance-voltage and current-voltage measurements on metal-oxide-semiconductor capacitors of several areas. The Pr$_2$O$_3$ films have shown a dielectric constant =23-25 and a leakage current density of 8.8 x 10e-8 A/cm$^2$ at +1 V.

- 출처

담담위원: 윤일구 교수(연세대)