Dielectric property and conduction mechanism of ultrathin zirconium oxide films

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Abstract
Stoichiometric, uniform, amorphous ZrO2 films with an equivalent oxide thickness of ~1.5nm and a dielectric constant of ~18 were deposited by an atomic layer controlled deposition process on silicon for potential application in metal-oxide-semiconductor (MOS) devices. The conduction mechanism is identified as Schottky emission at low electric fields and as Poole-Frenkel emission at high electric fields. The MOS devices showed low leakage current, small hysteresis (<5mV), and low interface state density (~2x1011/cm2eV). Microdiffraction and high-resolution transmission electron microscopy showed a localized monoclinic phase of α-ZrO2 and an amorphous interfacial ZrSiO4 layer which has a corresponding dielectric constant of 11.

References
Page(s): 3666-3668

High-k dielectrics by UV photo-assisted chemical vapour deposition

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Abstract
An overview of our recent work on thin films of metal oxides deposited on silicon by a novel excimer lamp-assisted ultraviolet injection liquid source CVD (UVILS-CVD) process for advanced high-k gate dielectrics applications will be presented. Recent results on TiO2, Ta2O5, ZrO2, HfO2, and TiO2-doped Ta2O5 will be demonstrated. The physical, structural, and interfacial properties of these high-k dielectrics will be compared with those of conventional SiO2 and Si3N4.
properties and electrical characterization of the as-deposited and UV-annealed new high dielectric constant (high-k) materials, determined using ellipsometry, Fourier transform infrared spectroscopy, X-ray photoelectron spectroscopy, UV spectrophotometry, SEM, TEM, and C-V, I-V measurements, showed that good quality layers could be produced. The investigation of high-k dielectrics grown by the UVILS-CVD process clearly demonstrates that low cost, high power density excimer lamp systems can provide an interesting alternative to conventional UV lamps and excimer lasers for industrial large-scale low temperature materials processing. UVILS-CVD is a promising technique for the controlled deposition of ultra thin high-k metal-oxide dielectrics for deep sub-micron CMOS devices at temperatures as low as 350°C.

출처
Microelectric Engineering, Volume:1, 2002, 000-000

논문제목
Annealing Effects On Ultra thin MOS Capacitors

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초록
Silicon oxide with thickness less than 9 nm is fabricated by tube furnace oxidation. Nitrogen is added to dilute the oxidation rate. Aluminum dots with radius of 0.05 cm are deposited on the oxide. High frequency capacitance-voltage (HF C-V), conductance-voltage (G-V) and current-voltage (I-V) characteristics are measured. Annealing under nitrogen atmosphere is carried out with different time and at different temperature. Densities of the interface states before and after annealing are compared. After annealing, a decrease in density of the interface states is found. Experiments show that 450°C annealing for 30 minutes has the lowest density of the interface states.

출처

논문제목
Effective electron mobility in Si inversion in metal-oxide-semiconductor systems with a high-k insulator: The role of remote phonon scattering
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초록
The high dielectric constant of insulators currently investigated as alternatives to SiO₂ in metal-oxide-semiconductor structures is due to their large ionic polarizability. This is usually accompanied by the presence of soft optical phonons. We show that the long-range dipole field associated with the interface excitations resulting from these modes and from their coupling with surface plasmons, while small in the case of SiO₂, for most high-k materials causes a reduction of the effective electron mobility in the inversion layer of the Si substrate. We study the dispersion of the interfacial coupled phonon-plasmon modes, their electron-scattering strength, and their effect on the electron mobility for Si-gate structures employing films of SiO₂, Al₂O₃, AIN, ZrO₂, HfO₂, and ZrSiO₃ for “SiO₂-equivalent” thickness ranging from 5 to 0.5 nm.

출처
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논문제목
Epitaxial growth of yttrium-stabilized HfO₂: high-k gate dielectric thin films on Si

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초록
Epitaxial yttrium-stabilized HfO₂ thin films were deposited on p-type (100) Si substrates by pulsed laser deposition at a relatively lower substrate temperature of 550 °C. Transmission electron microscopy observation revealed a fixed orientation relationship between the epitaxial film and Si; that is, (100)Si//(100)HfO₂ and [001]Si//[001]HfO₂. The film/Si interface is not atomically flat, suggesting possible interfacial reaction and diffusion. X-ray photoelectron spectrum analysis also revealed the interfacial reaction and diffusion evidenced by Hf silicate and Hf-Si bond formation at the interface. The epitaxial growth of the yttrium stabilized HfO₂ thin film on bare Si is via a direct growth
mechanism without involving the reaction between Hf atoms and SiO$_2$ layer. High-frequency capacitance-voltage measurement on an as-grown 40-A yttrium-stabilized HfO$_2$ epitaxial film yielded an effective dielectric constant of about 14 and equivalent oxide thickness to SiO$_2$ of 12 A. The leakage current density is $7.0 \times 10^{-2}$ A/cm$^2$ at 1 V gate bias voltage.


- 논문목록
  Basic characteristics of metal-ferroelectric-insulator-semiconductor structure using a high-k PrO$_x$ insulator layer

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- 초록
  A metal-ferroelectric [SrBi$_2$Ta$_2$O$_9$ (SBT)]-high-k-insulator(PrO$_x$)-semiconductor(Si) structure has been fabricated and evaluated as a key part of metal-ferroelectric-insulator-semiconductor-field-effect-transistor MFIS-FET memory, aiming to improve the memory retention characteristics by increasing the dielectric constant in the insulator layer and suppressing the depolarization field in the SBT layer. A 20-nm PrO$_x$ film grown on Si(100) showed both a high of about 12 and a low leakage current density of less than $1 \times 10^{-8}$ A/cm$^2$ at 1.5 MV/cm. A 400-nm SBT film prepared on PrO$_x$/Si shows a preferentially oriented (105) crystalline structure, grain size of about 130 nm and surface roughness of 3.2 nm. A capacitance-voltage hysteresis is confirmed on the Pt/SBT/PrO$_x$/Si diode with a memory window of 0.3 V at a sweep voltage width of 12 V. The memory retention time was about 1104 s, comparable to the conventional Pt/SBT/SiON$_x$/(SiO$_x$)/Si. The gradual change of the capacitance indicates that some memory degradation mechanism is different from that in the Pt/SBT/SiON/Si structure.

- 논문목록
  Atomic layer chemical vapor deposition of ZrO$_2$-based dielectric films: Nanostructure and nanochemistry

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- 초록
  A 4 nm layer of ZrO$_x$ (targeted x=2) was deposited on an interfacial layer (IL) of native oxide (SiO$_x$, t=1.2 nm) surface on 200 mm Si wafers by a manufacturable atomic layer chemical vapor deposition technique at 300°C. Some as-deposited layers were subjected to post-deposition, rapid thermal annealing at 700°C for 5 min in flowing oxygen at atmospheric pressure. The experimental x-ray diffraction, x-ray photoelectron spectroscopy, high-resolution transmission electron microscopy, and high-resolution parallel electron energy loss spectroscopy results showed that a multiphase and heterogeneous structure evolved, which we call the Zr-O/IL/Si stack. The as-deposited Zr-O layer was amorphous ZrO$_2$-rich Zr silicate containing about 15% by volume of embedded ZrO$_2$ nanocrystals, which transformed to a glass nanoceramic (with over 90% by volume of predominantly tetragonal-ZrO$_2$. (t-ZrO$_2$) and monoclinic-ZrO$_2$. (m-ZrO$_2$) nanocrystals) upon annealing. The formation of disordered amorphous regions within some of the nanocrystals, as well as crystalline regions with defects, probably gave rise to lattice strains and deformations. The interfacial layer (IL) was
partitioned into an upper SiO₂-rich Zr silicate and the lower SiO. The latter was sub-toxicometric and the average oxidation state increased from SiO0.85 in SiO₆ (as-deposited) to Si₁.32 in SiO₆₉ (annealed). This high oxygen deficiency in SiO was indicative of the low mobility of oxidizing specie in the Zr-O layer. The stacks were characterized for their dielectric properties in the Pt(Zr-O/IL)/Si metal oxide-semiconductor capacitor (MOSCAP) configuration. The measured equivalent oxide thickness (EOT) was not consistant with the calculated EOT using a bilayer model of ZrO₂ and SiO₂, and the capacitance in accumulation (and therefore, EOT and kZr-O) was frequency dispersive, trends well documented in literature. This behavior is qualitatively explained in terms of the multilayer nanostructure and nanochemistry that evolves.

- 출처
  Journal of Applied Physics, Volume:93 Issue:7 April 2003 Page(s): 4144-4157

- 논문제목
  Interfacial properties of ZrO. on silicon

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- 요약
  The interface of zirconium oxide thin films on silicon is analyzed in detail for their potential applications in the microelectronics. The formation of an interfacial layer of ZrSiO, with graded Zr concentration is observed by the x-ray photoelectron spectroscopy and secondary ion mass spectrometry analysis. The as-deposited ZrO₂/ZrSiO₃/Si sample is thermally stable up to 880°C, but is less stable compared to the ZrO₂/SiO₂/Si samples. Post-deposition annealing in oxygen or ammonia improved the thermal stability of as-deposited ZrO₂/ZrSiO₃/Si to 925°C, likely due to the oxidation/nitridation of the interface. The as-deposited film had an equivalent oxide thickness of ~1.3 nm with a dielectric constant of ~21 and a leakage current of 3.2 × 10⁻⁶ A/cm² at 1.5 V. Upon oxygen or ammonia annealing, the formation of SiO, and SiH₂NO, at the interface reduced the overall dielectric constants.

- 출처

- 논문제목
  Praseodymium oxide (Pr₂O₃) thin films have been deposited on Si(100) substrates by metalorganic chemical vapor deposition using praseodymium tris-2,2,6,6-tetramethyl-3,5-heptanedionate as source material. Film structural, morphological, and compositional characterizations have been carried out. Dielectric properties have been studied as well by capacitance-voltage and current-voltage measurements on metal-oxide-semiconductor capacitors of several areas. The Pr₂O₃ films have shown a dielectric constant ~23~25 and a leakage current density of 8.8 × 10⁻⁸ A/cm² at +1 V.

- 출처

- 논문제목
  Dielectric properties of Pr₂O₃, high-k films grown by metalorganic chemical vapor deposition on silicon

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  Praseodymium oxide (Pr₂O₃) thin films have been deposited on Si(100) substrates by metalorganic chemical vapor deposition using praseodymium tris-2,2,6,6-tetramethyl-3,5-heptanedionate as source material. Film structural, morphological, and compositional characterizations have been carried out. Dielectric properties have been studied as well by capacitance-voltage and current-voltage measurements on metal-oxide-semiconductor capacitors of several areas. The Pr₂O₃ films have shown a dielectric constant ~23~25 and a leakage current density of 8.8 × 10⁻⁸ A/cm² at +1 V.