완전 광 패킷 스위칭 시스템 : 클럭 추출 핵심 기술

(All-optical packet switching system : clock extraction as a key technology)

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요 약

링 구조형 광통신망에 적합한 완전 광 패킷 스위칭 시스템을 실험적으로 검증한다. 실험적 검증을 위해, 비디오 신호는 헤더와 페이로드로 구성된 광 패킷에 실리고, 완전 광 패킷 스위칭 노드에 전달 된다. 전달 된 광 패킷은 여러가지 완전 광 프로세서에 의해 처리되는데, 그들은 완전 광 헤더 처리기, 패킷-레벨 클럭 추출기, 비트-레벨 클럭 추출기, 데이타 형태 변환기 등으로 구성되어 있다.

Abstract

We demonstrate a novel all-optical packet switching system that is suitable for optical ring networks. For the demonstration, video signals are encoded into optical packets which are composed of header and payload. The optical packets are all-optically processed at a switching node based on all-optical header processor, packet-level clock extraction, bit-level clock extraction, all-optical data format converter and so on.

Keywords : all-optical packet switching, Optical Time Division Multiplexing (OTDM), clock extraction, optical ring network, Terahertz Optical Asymmetrical Demultiplexer (TOAD)

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I. 서 론

Recently, several tera-bit transmission systems[1] have been demonstrated. However, as the transmission bit-rate increases, the required signal processing speed for switching at each network node will exceed the physical limit of electronic components. In order to overcome the speed limitations of electronics, introduction of all-optical packet switching techniques exploiting the excellent physical properties of photons is inevitable. Although optics is theoretically capable of ultra-high speed signal processing, only a few practical optical devices are realized for optical buffering, optical packet synchronization and so on. Therefore, we need to

minimize the complexity and the number of functions in the design of systems as much as we can implement with the currently available devices. Our goal has been to find an all-optical packet switch with a simple architecture for ultra-high speed networks.

In this paper we propose and develop a novel all-optical packet switching system based on Optical Time Division Multiplexing (OTDM), which is composed of several key technologies such as a packet-level clock extractor[2], a bit-level clock extractor[3], a header detector, a data format converter and a payload extractor employing a Terahertz Optical Asymmetrical Demultiplexer (TOAD)[4]. Among the key technologies, in this paper the packet-level clock extractor and the bit-level clock extractor are dealt with in detail.

II. Ring network and its node architecture

Fig. 1(a) and (b) show an example of an optical ring network and its switch node architecture for simple packet switching. If we adopt the slotted ring protocol, each slot circulating around the ring will be occupied by full or empty packets, where the empty one has an unique header as 'E'header in Fig. 1(a). And there is a single node, i.e. management node for the ring network, for controlling such an empty packet in each ring as node 'M' in Fig. 1(a). Each node must have the ability to recognize the data packets destined to itself in order to drop messages. To add a packet from a node to the ring network, an input empty header is detected. Then, an empty packet and an outgoing packet are swapped.

When a packet enters into an optical node, the acket-level clock extractor pulls out the first clock of the packet for whole switch node chronization. Then, all-optical header detection is ormed with the incoming packet and the extracted et-level clock. If the detected header contains the ss of the optical node itself, the incoming packet
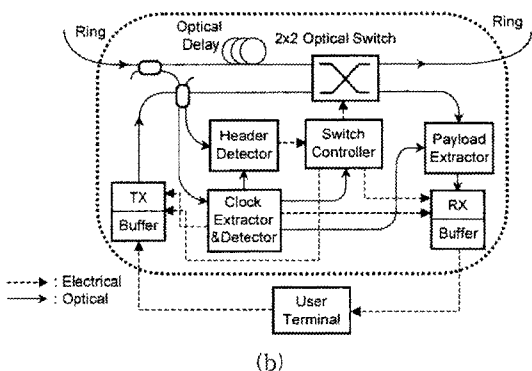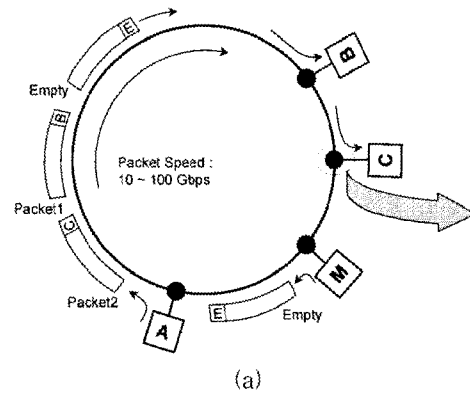

(a)

(b)

그림 1. (a) 링형 광 네트워크 (b) 스위치 노드 구조
Fig. 1. (a) Optical ring network and (b) its switch node architecture.

is switched to the packet extractor shown in Fig. 1(b). Otherwise, the incoming packet transparently passes the optical node. At the payload extractor, due to the speed limitations of electronics, the demultiplexing of an incoming high-speed packet to low speed signal is required[4]. The extracted packet-level clock is also used for synchronization of the packet generator (TX) and receiver (RX). The buffers with TX and RX in Fig. 1(b) take a role of packet-synchronizing andspeed-adapting for packets between a ring and a node.

III. Demonstration of an all-optical packet switch demonstration

An all-optical packet switching system with 1x2 switching architecture has been constructed. The system can handle the 10 Gb/s opticalpacket based
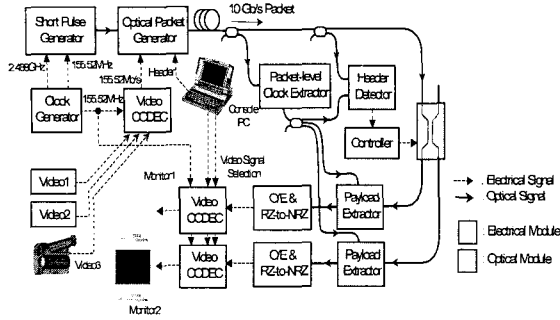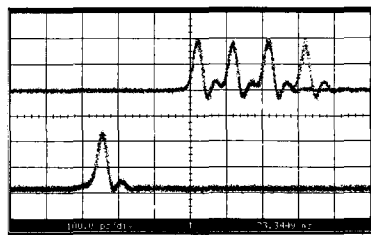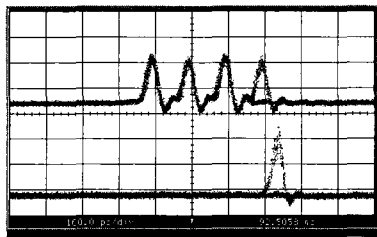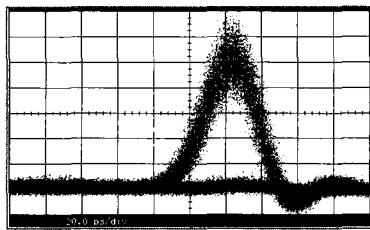
그림 2. 완전 광 패킷 스위칭 시스템의 전체 구조
Fig. 2. Overall architecture of all-optical packet switching system.

(a)

(b)

(c)

그림 3. 실험결과 (a) 패킷-레벨 클럭 추출 (b) 페이로드 추출 (c) 페이로드의 확대된 아이 모양
Fig. 3. Experimental results of (a) Packet-level clock extraction (b) Payload extraction (c) Magnified eye.

OTDM. Although only the packet dropping function is implemented, almost all the functions as an optical

node are included. Fig. 2 shows overall architecture of an all-optical packet switching system for demonstrations. Three video signals are multiplexed and then converted to a 155.52 Mb/s digital signal by the video CODEC. The digital signal inputs to the optical packet generator and modulates a payload of 10 Gb/s packet. The optical packet is generated based on time interleaving technique. The generator is composed of 1x4, 4x1 couples, optical delays, and optical modulators, which makes 4 bits optical packets. The optical packet consists of 4 bits including one synchronization bit, two header bits, and one payload bit. The upper signal of Fig. 3 (a) shows the oscilloscope trace of the optical packet when the header is "11". When the packet enters into a switching node, the packet-level clock extraction is firstly conducted. To perform such function, a simple TOAD scheme is used, which is based on pattern effect of a Semiconductor Optical Amplifier (SOA) and phase asymmetry in a fiber loop mirror. The lower signal of Fig. 3(a) shows the packet-level clock extracted from the incoming packet. More than 10dB of the contrast ratio between the extracted clock pulse and the three removed pulses can be achieved. Also, only 1~10 pJ/pulse optical energy for the operation is required. If there are long sequences of "0" bits in a packet, the contrast ratio is greatly reduced. However, the appearance of such a long quiet interval in a packet can be avoided by proper line coding techniques.

The extracted packet-level clock is used as a control signal of the header detector and two payload extractors. Such functions are implemented using an ordinary TOAD optical AND logic[4]. The control signal must have a different wavelength compared with the packet signal. So, to change the wavelength of the extracted clock, non-interferometric SOA/fiber-Bragg-gratingfilter wavelength conversion[5] is employed. In our demonstration, although the payload is only one bit, the payload with long sequences can be handled by using 1xn demultiplexing scheme with several TOADs[4]. Fig. 3(b) shows the eye diagram

for a video signal measured at the output of the payload extractor and the magnified eye diagram of the extracted payload is shown in Fig 3(c). After an electrical RZ-to-NRZ conversion, the extracted payload is converted to a 155.52 Mb/s digital signal. Then, the digital signal is changed to three video signals by two video CODECs. At the same time, one of three video signals is selected for displaying video signal by the console PC as shown in Fig. 2.

IV. Packet-level clock extraction

Fig. 4shows a packet-level clock extraction scheme using a modified TOAD. With the same scheme, K.-L. Deng et al.[6] have carried out the packet-level clock extraction from the packet composed of a strong clock pulse at the first bit position followed by weak data pulses, where the TOAD acts as an intensity discriminator. However, in this paper, TOAD extracts packet-level clock pulse from packets made of identical pulses only.

As shown in Fig. 4, the modified TOAD is constructed by connecting output ports ③ and ④ of a tunable directional coupler (TDC) through an SOA, without WDMcouplers in the loop mirror. When a
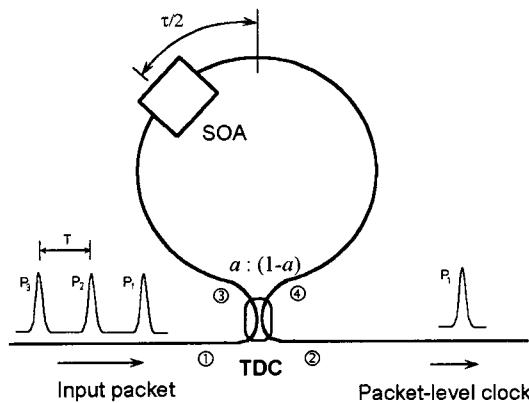
Fig. 4. Schematic of a modified TOAD for packet-level clock extraction.(SOA : semiconductor optical amplifier, TDC : tunable directional coupler).

pulse enters port ①, it is split into two pulses; the one from port ③ goes in the clockwise (CW) direction and the other from port ④ goes in the counterclockwise (CCW) direction. The SOA is placed in such a way that the CW pulse arrives at the SOA before the CCW pulse with arrival time interval t. We assume that the gain recovery time t_g of the SOA is much longer than the pulse period T (t_g >>T). The SOA-arrival time difference t between CW and CCW pulses is set to be shorter than T (τ <T).

The intensities of the transmitted and reflected signals by the TOAD are given by[6, 7]

$$I_r = I_{in}(a(1-a)(G_{cw} + G_{ccw})$$
$$+ 2a(1-a)\sqrt{G_{cw}G_{ccw}}\cos\theta_{diff}),\qquad(1)$$
$$I_t = I_{in}(a^2 G_{cw} + (1-a)^2 G_{ccw}$$
$$- 2a(1-a)\sqrt{G_{cw}G_{ccw}}\cos\theta_{diff}),\qquad(2)$$

where Iin is input intensity, Ir is reflected intensity, It is transmitted intensity, and ais the coupling coefficient of the TDC. Gcw and Gccw denote gains of the SOA for the CW and the CCW pulses, respectively, and qdiff is the phase difference between them. They are coupled by[7]

$$\theta_{diff} = \theta_{cw} - \theta_{ccw} = -\frac{\alpha}{2}\ln(G_{cw}/G_{ccw}),\qquad(3)$$

where a is the linewidth enhancement factor.

The Operation schematic of the modified TOAD is shown in Fig. 5. The pulse P1,cw arrives earlier than P1,ccw at the SOA and then saturates the SOA with large pulse gain G1,cw, where the gain falling time of the SOA is very much shorter than the gain recovery time t_g. Because t << t_g, the pulse P1,ccw enters the gain saturated SOA and has much small gain G1,ccw as shown in Fig. 5. Due to such an asymmetric gain and the following phase difference, as expected from Eqs. (1)-(3), the first pulse can be transmitted.
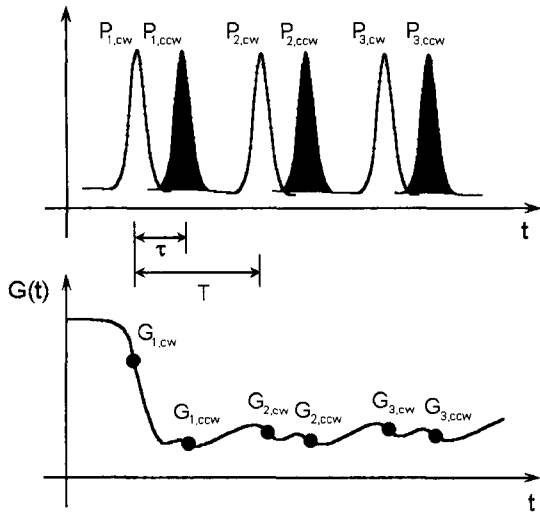
그림 5. 변형된 TOAD 에서 SOA 의 게인 다이어그램
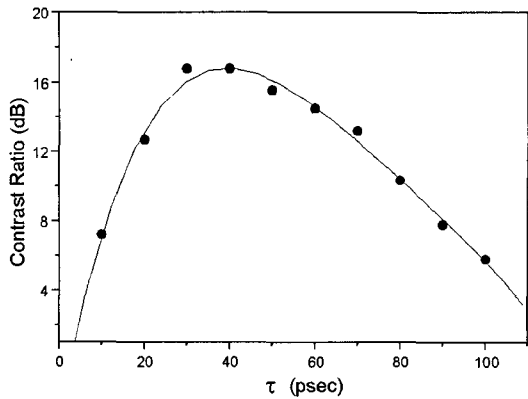Fig. 5. Gain diagram of the SOA in the modified TOAD.

그림 6. SOA-도착시간차이 t 에 대한 소광비
Fig. 6. Contrast ratio corresponding to the SOA-arrival time difference, t.

Since $T \ll t_g$, the SOA gain remains saturated for the second pulse P2 so that the CW and CCW pulses, P2,cw and P2,ccw, experience nearly same pulse gain. From Eqs. (1)-(3), it becomes I2,r I2,inG2,cw and I2,t 0 for a=0.5and the TOAD acts as an ordinary fiber loop mirror. Therefore, as far as the pulse intervals in a packet are much shorter than tgand the guard time between packets is longer than t_g, the scheme shown in Fig. 4 will generate packet-level clock pulses.

Optical pulses at 2.48832 GHz with ~90 psec

FWHM was generated by gain switching of a DFB-LD and then compressed to ~20 psec FWHM by simply passing through a ~3km-long dispersion-compensated fiber (DCF). An optical modulator generated 155.52 MHz optical pulse train (pulse interval ~6.43nsec) by gating one every sixteen pulses. Each pulse was converted into an equal intensity optical pulse pair by an asymmetric Mach-Zehnder interferometer. Fig. 6shows contrast ratio, or the intensity ratio between the two pulses in each pair after passing through the TOAD, as a function of the SOA-arrival time difference, t. The SOA used in this experiment was 1000 mm-long and polarization insensitive type (~0.6 dB). The SOA current was set to 80 mA, a of TDC was adjusted to 0.43, and the input optical power was -4 dBm (~1.3 pJ/pulse). As shown in Fig. 6, contrast ratio of ~ 17dB was obtained when t was? 30~40 psec. The rising time in Fig. 6 corresponds to the pulsewidth and the pulse travelling time in the SOA. Fig. 7 shows the contrast ratio as a function of the optical power when t was set to 30 psec. The contrast ratio exceeded 15 dB when the input power was -4 ~ 0 dBm (~1.3-~3.3 pJ/pulse). If one optical pulse does not have enough energy to saturate the SOA, the next pulse will get a partial gain. The contrast ratio increases as the input power grows until the SOA gain is fully saturated by an optical pulse. Beyond
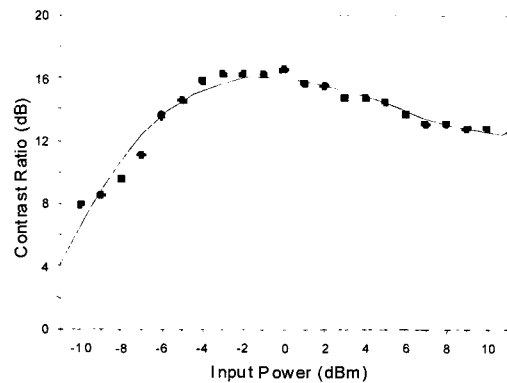

그림 7. 입력 전력 대 소광비
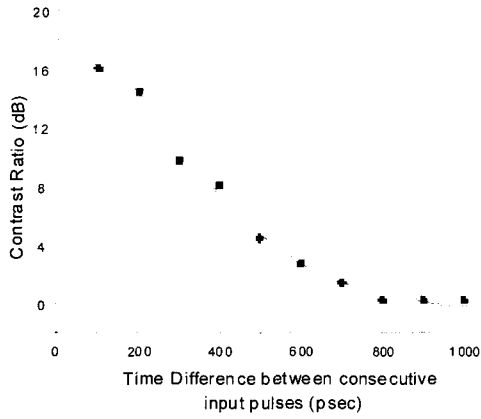Fig. 7. Contrast ratio corresponding to the input power.

그림 8. 두 펄스 사이의 시간 대 소광비
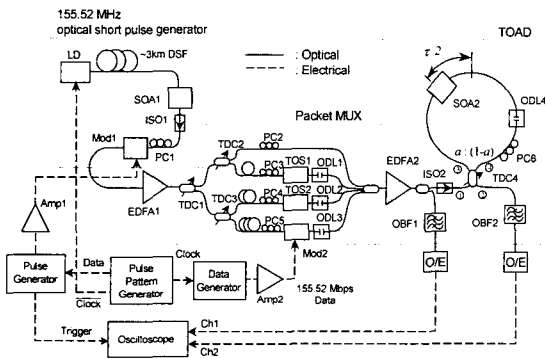Fig. 8. Contrast ratio corresponding to the time interval between two pulses.

그림 9. 완전 광 패킷-레벨 클럭 추출을 위한 실험 장치
Fig. 9. Experimental setup for all-optical packet-level clock extraction.
SOA : semiconductor optical amplifier,
TDC : tunable directional coupler,
PC : polarization controller,
Mod : optical modulator,
TOS : thermo-optic switch,
ISO : optical isolator,
DSF : dispersion-shifted fiber,
ODL : optical delay line,
EDFA : erbium-doped fiber amplifier,
OBF : optical bandpass filte

that input power, due to the big difference between G1,cw and G1,ccw, the phase difference becomes gradually less than -πand then the transmittance of the first pulse is reduced. Therefore, the contrast ratio slowly wanes. To check the effect of SOA gain recovery time to the scheme, we varied the time interval between the two optical pulses in each pair

from 100 psec to 1,000 psec. The time interval between each pulse pair was ~6.43 nsec and the SOA-arrival time difference τin the loop of the modified TOAD was kept to be 30 psec. The result is shown in Fig. 8.

From Figs. 6 and 8, it is easily seen that the lower packet speed limit is set by the SOA gain recovery time, while the upper limit is set by the width of the employed optical pulse.

Fig. 9 shows an experimental setup to demonstrate the operation of all-optical packet-level clock extraction using a modified TOAD. 155.52 MHz optical pulse with ~20 psec FWHM was generated and converted to a 10 Gbps 4-bit packet which consists of one packet-level clock bit, two header bits, and one payload bit by the Packet MUX optical circuit shown in Fig. 9. The two header bits can be manipulated by polymeric thermo-optic switches
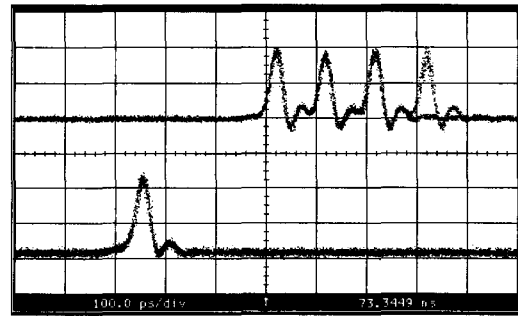
(a)
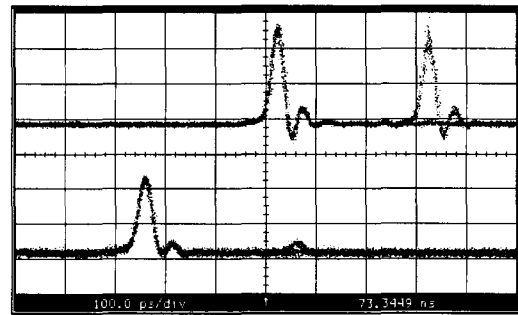
(b)

그림 10. 헤더가 (a) "11" 과 (b) "00" 일때 4 비트 패킷 데이타에 대한 오실로스코프 데이타
Fig. 10. Oscilloscope traces of the 4-bit packet data when the header is (a) "11" and (b) "00".

(TOS1 and TOS2). Figs. 10(a) and 10(b) show oscilloscope traces of the 4-bit packet data and the packet-level clock extracted from the packet when the headers are "11" and "00", respectively. As expected in Fig. 8, Fig. 10(b) shows about contrast ratio of ~ 10 dB between the clock pulse and the payload pulse.

The packet-level clock extraction is ensured as far as the guard time between packets is longer than the SOA gain recovery time, ~1 nsec. From Fig. 7, the contrast ratio was 15dB when pulse energy was between ~1.3 pJ and ~3.3 pJ. Within the range, from Fig. 8, the first bit of the packet or the synchronization bit will be 10dB larger than the rest bits of the packet, as far as there are no sequence of "0" bits longer than 300 psec. It will be two "0"bits for 10 Gbps and twenty-nine "0" bits for 100 Gbps. The appearance of such a long quiet interval in a packet can be avoided by proper line coding techniques[8]. Furthermore, the proposed scheme works better when the speed goes up, suitable for the future OTDM packet systems.

V. Bit-level clock extraction

Fig. 11 shows the experimental set-up of all-optical bit-level clock extractor proposed in this paper. The wavelength converter (dashed box in Fig. 11) for RZ data has been proposed by P.S. Cho et al.[5]. After the input signal (λ_{sig}) enters into the port 1 of the OC, the output signal from the port 2 passes through the SOA. On the other hand, a continuous wave (CW) beam (λ_{cw}) generated from the T-LD propagates the opposite direction of the input signal (λ_{sig}) through the Iso2, and then enters into the port 2 and comes out from the port 3 of the OC. At this time, the wavelength lcwof the CW beam near to the leading-edge of RZ input data is red-chirped to $\lambda'_{cw} = \lambda_{cw} + D[$[5,9].The wavelength-shifted component is selected by the narrow bandwidth grating-filter (OBF1) of which the center wavelength is set to λ'_{cw}. With such a mechanism, the wavelength lsigof the input data can be changed to λ'_{cw}[5]. For thebit-level clock extraction,
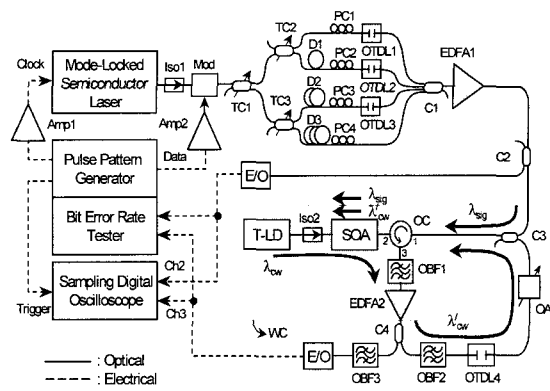

그림 11. 실험 장치
Fig. 11. Experimental set-up.
Iso : optical isolator,
Mod : optical modulator,
TC : tunable coupler,
D : optical delay line,
PC : polarization controller,
OTDL : optical tunable delay line,
C : coupler,
EDFA : Erbium-doped fiber amplifier,
OC : optical circulator,
SOA : semiconductor optical amplifier,
T-LD : tunable laser diode,
OBF : optical band pass filter,
OA : optical attenuator

the wavelength-converted signal is fedback to the port 1 of the OC through EDFA2, C4, OBF2, OTDL4, OA, and C3. And then, the input signal is combined with the wavelength- converted feedback signal at the port 1 of the OC by the C3. Here, the OTDL4 is tuned to align the bit timing between the input signal (λ_{sig}) and the wavelength-converted feedback signal (λ'_{cw}). A feedback time is to be little greater than or equal to nT, where n is any integer and T is a bit interval time of the input signal (λ_{sig}). By the combined signals, the CW beam (λ_{cw}) from T-LD is frequency-chirped. After these operations repeat over and over again, the frequency chirping is found at every bit position. Then, the stable clock signal can be obtained from the output of the OBF1, where the intensity of each pulse is matched in the time domain. Unlike the mode-locked fiber ring laser, the feedback signal (λ'_{cw}) is circulated through the fiber loop only one time. Because the proposed bit-level

clock extractionmethod is based on repetitive pulse intensity matching in the time domain, it does not require the stabilization circuit for exact phase matching compared to the mode-locked fiber ring laser. Using the similar method we have successfully applied to the all-optical circulating shift register[10] and clock division[11].

For 10 Gbps RZ data generation, firstly the 2.5 GHz optical short pulse train with lsig = 1550nm, FWHM = ~25psec is generated using a short pulse source (Santec, TSL-200). 2.5 Gbps RZ data sequence is generated by modulating the pulse train with a LiNbO$_3$ electro-optic modulator driven by a pulse pattern generator (PPG). The length of the pseudorandom binary sequence of the input signal is 2^{23}-1 at 2.5 Gbps. The 2.5 Gbps RZ data become 10 Gbps RZ data by simply passing through 1:4 optical fiber MUX as shown in Fig. 11. The 10 Gbps RZ data enters into the SOA through coupler C2, C3, and OC. The SOA (a carrier lifetime of ~320ps, Alcatel 1901) in this experiment is a polarization insensitive type (~0.6dB) based on low tensile bulk GaInAsP and is driven at an operating bias current of 185 mA. 4 dBm, λ_{cw} = 1545nm CW beam from T-LD (HP8168F) reversely enters into the SOA through Iso2. At this time, the frequency chirping in the CW beam is occurred by the input 10Gbps signal counter-propagating. The chirping components are extracted by the grating filter (OBF1, which has a bandwidth of 0.25nm at 3dB, JDS FITEL TB9226), with the center wavelength set to 1/cw = 1545.5nm. The extracted signal makes intensity sum with the input signal and is fedback to the SOA. Here, the wavelength-converted feedback signal with wavelength λ'_{cw} circulates only once and disappears.

The experimental result of the optical clock extractionis shown in Fig. 12. Fig. 12 (b) shows oscilloscope trace of 10 Gbps RZ data generated by 1:4 bit-interleaving 2.5 Gbps RZ data. Fig. 12(a) shows oscilloscope trace of the clock extraction result obtained by the proposed method. The inlet graphs in Fig. 12 are eye diagrams of each data.
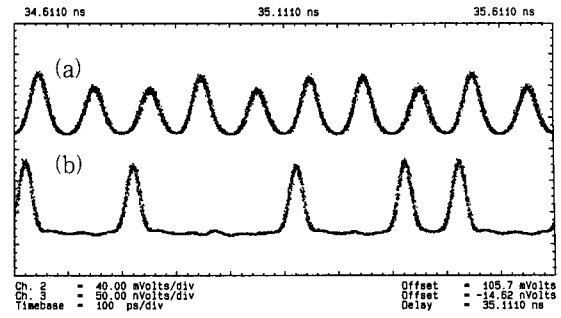

그림 12. 측정된 오실로스코프 데이터 (a) 재생된 클럭 펄스 (b) 10 Gbps RZ 입력 데이타

Fig. 12. Measured oscilloscope traces. (a) Recovered clock pulse (b) 10 Gbps RZ input data
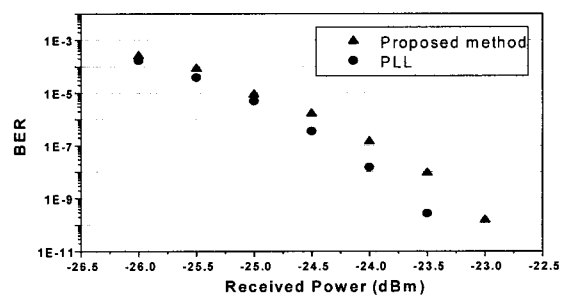

그림 13. 전기 PLL 과 제안된 클럭 재생의 성능 비교를 위한 BER 측정

Fig. 13. BER measurements for the proposed CR to compare with an electrical PLL.

To experiment the polarization dependency, even we changed the polarization arbitrarily by stirring the PC1, 2, 3, 4, the output clock was still stable. Also, to investigate the sensitivity of the feedback fiber loop length, we adjusted the OTDL4 within the range of 0~10 psec. But, there was no variation on the extracted clock. Fig. 13 shows bit-error-ratio (BER) measurements for the proposed bit-level clock extractor to compare with electrical phase-locked loop (PLL) method. The 10 Gbps data and the extracted clock were 4:1 demultiplexed and then BER was measured. We have noticed that the proposed bit-level clock extractoris nearly comparable to the conventional PLL (power penalty = ~0.5 dB @ 10^{-9} BER).

VI. Conclusions

We have successfully developed the all-optical packet switching system for the videosignal switching demonstration in TELECOM exhibition. Although the demonstration has been conducted for a 10 Gb/s optical packet consisting of only 4 bits, the proposed system can be extended to take care of a long packet with ~100Gb/s using an ultra-short pulse generator.

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