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전류-제어 인덕터 및 FDNR 시뮬레이션을 위한 능동-RC 회로 합성

(Active-RC Circuit Synthesis for the Simulation of Current-Controllable Inductors and FDNRs)

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요 약

OTA를 이용한 전류-제어 인덕터를 시뮬레이션하기 위한 체계적인 합성 과정을 기술했다. 그 합성 과정을 통해 세 개의 시뮬레이티드 인덕터를 설계했고, 그 중에서 두 개는 새롭게 설계된 것이다. 또한, 이 합성 과정을 전류-제어 FDNR 설계에 적용했다. 설계된 회로들의 동작 원리를 제시했고, 실험을 통해 설계 이론의 타당성을 증명했다. FDNR을 전류-제어 대역-통과 여파기에 응용한 예도 제시했다.

Abstract

Abstract----A systematic synthesis process is described for the simulation of current-controllable inductors using operational transconductance amplifiers (OTAs). The process is used to obtain three circuits; two are believed to be novel. The process is also applied to design current-controllable frequency-dependent negative resistances (FDNRs). Operation principles of designed circuits arepresented and experimental results are used to verify theoretical predictions. The results show close agreement between predicted behavior and experimental performance. The application of a FDNR to a current-controllable band-pass filter is also presented.

Keyword : Active circuit, Inductance simulation, FDNR, Operational transconductance amplifier, Transadmittance amplifier

I. Introduction

Current-controllable simulated inductors are useful building blocks in the design of electrically tunable filters and oscillators[1-3]. In addition, such inductors are used comprehensively in integrated continuous-time filters. In these filters, automatic tuning via current-controllable inductors is necessary to maintain precise filtering characteristics against process variations, temperature drift, aging, etc[4]. Several configurations have appeared in the literature for the realization of current-controllable inductors [5-8]. These are usually introduced simply as

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terminated gyrators implemented with operational transconductance amplifiers (OTAs). Since the transconductances of OTAs are proportional to an external dc bias current, the simulated inductance implemented with these devices is current variable.A major disadvantage of this technique is that it requires three or four identical differential-in single-ended-out OTAs for realizing a floating inductor. This results in a number of undesirable characteristics for IC design including high power, large chip area, and careful layout in such applications that accurate series inductances are important.

In this paper a new approach is presented for the systematic design of active-RCcircuits which simulate the branch relation of a current-controllable inductor. In this approach, an OTA is used as a feedback element in active-RCcircuits for the simulation of inductance. This makesit possible to synthesize several inductor circuits and two of them are new configurations which can not be derived by the terminated gyrators. A main advantage of this approach is the realization of the floating inductor with two differential-in differential-out OTAs. It features simple configuration and higher quality factor than those of the previous works mentioned above. The other advantage of the approach is that it can be directly applied to design current controllable frequency-dependent negative resistances (FDNRs). The design processes for synthesizing inductors and FDNRs are described in Section II and Section III, respectively. The experimental results and an application are presented in Section IV.

II. Design Principles of Current-Controllable Inductors

A. Grounded Inductors

Two block diagrams for synthesizing current-controllable grounded inductors are shown in Fig. 1(a) and (b). In these structures, the OTA marked G_m is used as a feedback element and the active

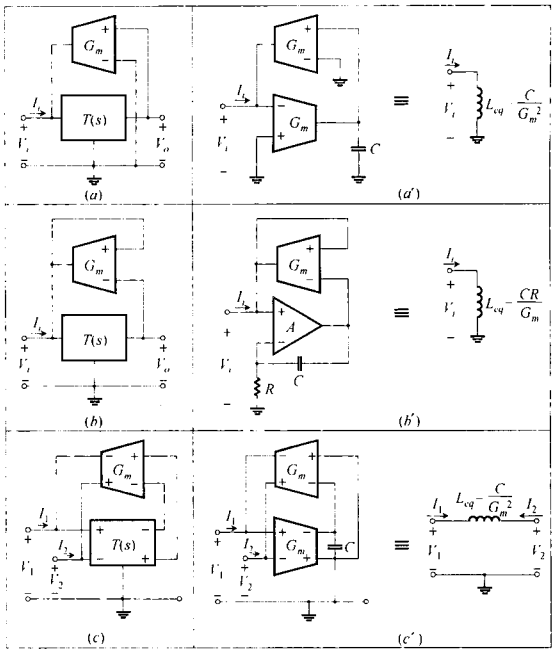

그림 1. 전류-제어 인덕터를 시뮬레이션하기 위한 블록도

Fig. 1. Block diagrams of circuit for simulating a current-controllable inductor.

two port marked $T(s)$ is assumed to have an infinite input impedance and a transfer function

$$T(s)=\frac{V_o(s)}{V_i(s)} \tag{1}$$

In Fig. 1(a), the input current is

$$I_i(s)=-G_m V_o(s)=-G_m T(s)V_i(s) \tag{2}$$

where G_m is the transconductance of the OTA. The input impedance of the circuit will be that of an inductor if

$$\frac{V_i(s)}{I_i(s)}=\frac{1}{-G_m T(s)}=sL_{eq} \tag{3}$$

Equation (3) gives

$$T(s)=-\frac{1}{G_m sL_{eq}} \tag{4}$$

Equation (4) indicates that $T(s)$ can be obtained

using an inverting integrator. Several circuits can be designed for the inductance simulation, since the inverting integration can be accomplished with active-RCcircuits in several ways. One of them, which is believed to be the most simple, is shown in Fig. 1(a)[5, 6]. In this realization, the lower OTA in conjunction with the grounded capacitor C forms the inverting integrator. For simplicity, assuming that two OTAs are identical and ideal, the circuit presents the simulated inductance L_{eq} given by

$$L_{eq}=\frac{C}{G_m^2} \tag{5}$$

Since G_m is proportional to the dc bias current of the OTA[9, 10], the simulated inductance will be inversely proportional to the square of the bias current.

Consider the second block diagram of Fig. 1(b). The input current is

$$I_i(s)=-G_m[V_i(s)-V_o(s)]=-G_m[1-T(s)]V_i(s) \tag{6}$$

The input impedance of the circuit will be inductive, if

$$\frac{V_i(s)}{I_i(s)}=\frac{-1}{G_m[1-T(s)]}=sL_{eq} \tag{7}$$

Equation (7) gives

$$T(s)=1+\frac{1}{G_m sL_{eq}} \tag{8}$$

Thus, $T(s)$ can be obtained using a noninverting integrator and an adder. The noninverting integration and addition can simply be accomplished using an op amp-RC circuit. The resulting circuit is shown in Fig. 1(b), which gives the simulated inductance of

$$L_{eq}=\frac{CR}{G_m} \tag{9}$$

It is noticeable that the inductance is inversely proportional to the transconductance of the OTA.

B. Floating Inductors

Floating inductors can be realized by replacing both the feedback element and the active two-port circuit of Fig. 1(a) with differential-in differential-out devices, as shown in Fig. 1(c). The input currents at the floating ports are

$$I_1(s)=G_mT(s)[V_1(s)-V_2(s)] \tag{10}$$

$$I_2(s)=-G_mT(s)[V_1(s)-V_2(s)] \tag{11}$$

Equations (10) and (11) lead to the admittance matrix given by

$$\begin{bmatrix}I_1(s)\\I_2(s)\end{bmatrix}=G_mT(s)\begin{bmatrix}1&-1\\-1&1\end{bmatrix}\begin{bmatrix}V_1(s)\\V_2(s)\end{bmatrix} \tag{12}$$

The input impedances at the floating ports of the circuit will be inductive, if $G_mT(s)=1/sL_{eq}$. Therefore, floating inductors are obtainable with $T(s)=1/G_m sL_{eq}$. $T(s)$ can be realized using a noninverting integrator. The most simple configuration is shown in Fig. 1(c), which gives at the floating ports the simulated inductance of

$$L_{eq}=\frac{C}{G_m^2} \tag{13}$$

C. OTA Implementation

A simple implementation of the differential-in single-ended-out OTA block for the grounded inductors is shown in Fig. 2[10]. It consists of a linear transconductor formed by transistors Q_1-Q_2 and an emitter-degeneration resistor R_E, a trans-linear current gain cell Q_3-Q_6, and three Wilson current mirrors. For simplicity, assume that all the transistors are ideal and identical. The transconductor converts the differential input voltage V_{in} to its corresponding differential output currents,

$$I_{c1}\cong I_X+\frac{V_{in}}{R_E} \tag{14a}$$

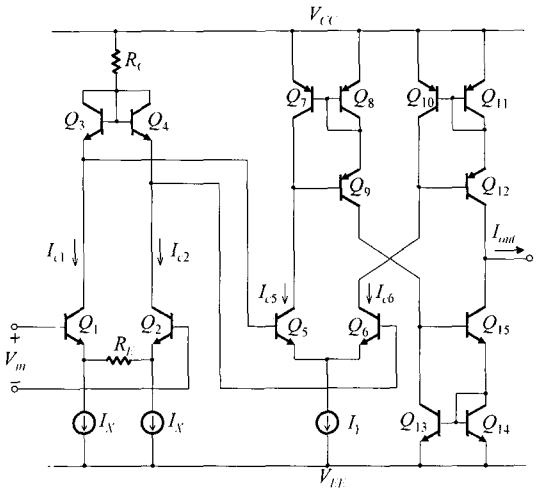

그림 2. 접지된 인덕터를 구현하기 위한 차동 입력-단일 출력 OTA 회로

Fig. 2. Differential-in single-ended-out OTA circuit for implementing grounded inductors.

$$I_{c2} \cong I_X - \frac{V_{in}}{R_E} \tag{14b}$$

where I_X is the dc current for biasing the input stage transistors Q_1 and Q_2. These differential output currents of the transconductor drive the diode-connected transistor pair Q_3 and Q_4 of the translinear current gain cell. The current gain cell makes the current partitioning of the transistor pair Q_3 and Q_4 to be the mirror image of the current partitioning of the transistor pair Q_5 and Q_6. Therefore, we can write the following relation:

$$\frac{I_{c1}}{I_{c2}} = \frac{I_{c6}}{I_{c5}} \tag{15}$$

The output currents I_{c5} and I_{c6} of the current gain cell are differenced by three current mirrors formed by Q_7-Q_9, Q_{10}-Q_{12}, and Q_{13}-Q_{15}, respectively. Since the sum of I_{c5} and I_{c6} is I_Y and the difference is I_{out}, which denotes the single-ended output current of the OTA, currents I_{c5} and I_{c6} can be written as follows:

$$I_{c5} = \frac{I_Y}{2} - \frac{I_{out}}{2} \tag{16a}$$

$$I_{c6} = \frac{I_Y}{2} + \frac{I_{out}}{2} \tag{16b}$$

Combining (14a), (14b) and (16a), (16b) into (15), one can obtain the transfer function of the OTA expressed as follows:

$$I_{out} = \frac{I_Y}{I_X}\frac{1}{R_E}V_{in} \tag{17}$$

The transconductance G_m is given by $(I_Y/I_X)(1/R_E)$. It should be noted that the tansconductance of the OTA is determined by the ratio of the dc bias currents I_Y and I_X.

It can be shown from (14a) and (14b) that the input linear range of the OTA is

$$|V_{in}| \le R_E I_X \tag{18}$$

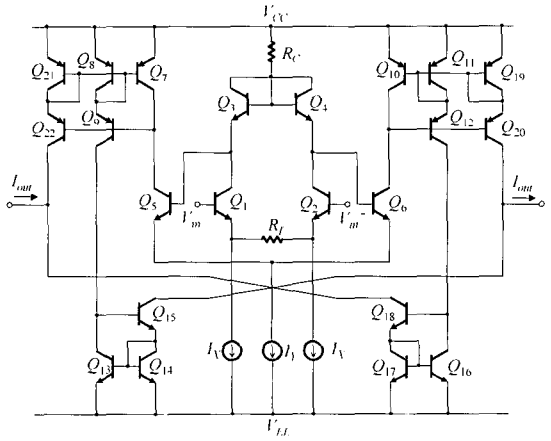

그림 3. 플로팅 인덕터를 구현하기 위한 차동 입력-단일 출력 OTA 회로

Fig. 3. Differential-in differential-out OTA circuit for the floating inductor simulation.

Fig. 3 shows a differential-in differential-out OTA circuit for the floating inductor simulation. Three current mirrors formed by Q_{16}-Q_{18}, Q_{19}-Q_{20}, and Q_{21}-Q_{22} are added in the differential-in single-ended-out OTA of Fig. 2 in order to obtain the differential output currents I_{out}^+ and I_{out}^-. The transfer function of the OTA is expressed as follows:

$$I_{out}^{+} = I_{out}^{-} = \frac{I_Y}{I_X}\frac{1}{R_E}(V_{in}^{+} - V_{in}^{-}) \tag{19}$$

The transconductance G_m is given by $(I_Y/I_X)(1/R_E)$. If the floating inductor of Fig. 1(c)is implemented with this OTA, we can obtain from (13) and (19) its equivalent inductance,

$$L_{eq} = \frac{CR_E^2}{(I_Y/I_X)^2} \tag{20}$$

It should be mentioned that the equivalent inductance is inversely proportional to the square of the dc current ratio (I_Y/I_X).

Ⅲ. Current-Controllable FDNRs Design

The design principles for simulating current-controllable inductors described in previous section can be directly applied to realize current-controllable FDNRs via element substitutions. The resulting circuits are shown in Fig. 4. Comparing this figure with Fig. 1, it can be observed that the circuit elements are substituted as follows: transconductance amplifier marked G_m transadmittance amplifier marked Y_m

capacitor C resistor R

resistor R capacitor C

The circuit in Fig. 4(a) can be also found in[11], but the circuits in Fig. 4(b) and 4(c) are new ones.

The transadmittance amplifier produces a current output which is the product of the input voltage by the transadmittance Y_m of the amplifier. A differential-in single-ended-out transadmittance amplifier can be simply implemented by replacing the degeneration resistor R_E of the differential-in single-ended-out transconductance amplifier shown in Fig. 2 with a degeneration capacitor C_E. Similarly, a differential-in differential-out transadmittance amplifier can be implemented by replacing the

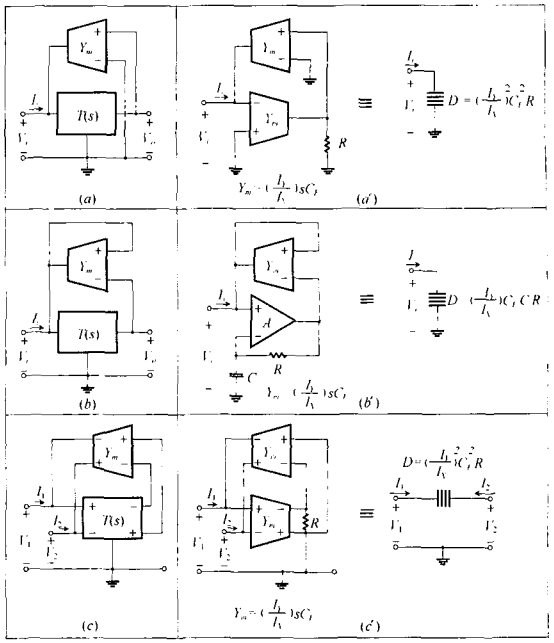

그림 4. 전류-제어 FDNR을 실현하기 위한 회로도
Fig. 4. Block diagramsof circuit for realizing a current-controllable FDNR.

degeneration resistor R_E of the differential-in differential-out transconductance amplifier shown in Fig. 3 with a degeneration capacitor C_E. The resulting transadmittances for both amplifiers are given by

$$Y_m = \frac{I_Y}{I_X} sC_E \tag{21}$$

and their input linear ranges are

$$|V_{in}| = \frac{I_X}{\omega C_E} \tag{22}$$

If the FDNRs of Fig. 4 areimplemented with these transadmittance amplifers, we can obtain their equivalent representations also shown in Fig. 4. It should be noted that the FDNR D can be tuned by varying the dc current ratio (I_Y/I_X).

Ⅳ. Experimental Results and Application

The simulated floating inductor shown in Fig. 1(c)was built using differential-in differential-out OTAs shown in Fig. 3 and a capacitor C = 500 pF. The transistor arrays used for OTAs were MPQ 2222 (npn) and MPQ 2907 (pnp). The resistors used were R_1 = 20 k and R_2 = 8 k. The bias current I_Y was set to 125 Afor convenience. All measurements were performed at supply voltages of V_{CC} = 5 V and V_{EE} = −5 V. The relation between the simulated inductance $\sqrt{L_{eq}}$ and the bias current I_Y was measured by a series resonance method. The series capacitor used was 30 nF. The results are plotted in Fig. 5, which shows that the experimental results are in good agreement with the theoretical values over the inductance range of 10-5000 $\sqrt{mH}$ (2.5 decades).

The nonidealities of the OTA such as the cutoff frequency and the stray capacitances at the input and output nodes introduce a lossy component, and thus a finite quality factor Q_L, into the simulated

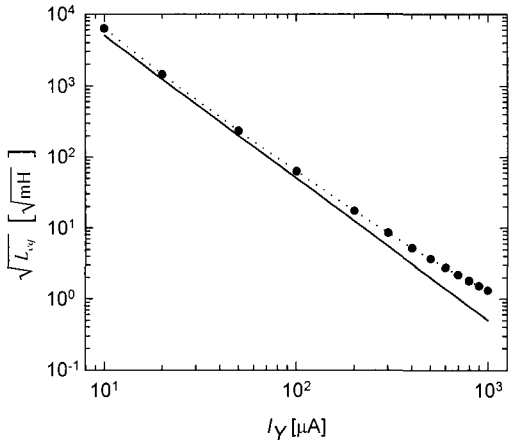

그림 5. <그림 1(c')>에 나타낸 시뮬레이터드 인덕터의 바이어스 전류 I_Y에 대한 인덕턴스

Fig. 5. Measured inductance against bias current I_Y of the simulated floating inductor shown in Fig. 1(c').
●-●-● experimental values
——— theoretical values

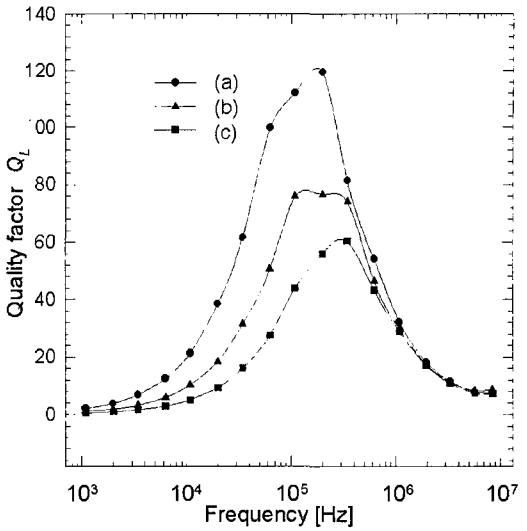

그림 6. 인덕턴스의 Q_L 특성 (a) <그림 1(c')>에 나타낸 제안된 프로팅 인덕터 (b) 참고문헌[5]의 프로팅 인덕터 (c) 참고문헌[6]의 프로팅 인덕터

Fig. 6. Q_L characteristics of the inductors: (a) Proposed floating inductor shown in Fig. 1(c'). (b) Floating inductor in [5]. (c) Floating inductor in [6].

inductor. The Q_L-factor was also measured by the series resonance method. The results are plotted in Fig. 6. For comparison, the floating inductors described in[6, 7] were also built using OTAs in Fig. 2 and their Q_L factors were measured. The results are also shown in Fig. 6, which indicate that the Q_L-factor of the proposed inductor is about 2 times higher than those of the previous works.

The floating FDNR shown in Fig. 4(c) was also built using differential-in differential-out transadmittance amplifiers with a degeneration capacitor C_E = 1 nF and a grounded resistor R = 500 k. The relation between the FDNR D and the bias current I_Y was measured by a series resonance method. The series capacitor used was 800 pF. The results are plotted in Fig. 7, which shows that the experimental results are in good agreement with the theoretical values over the D range of 10^{16} - 10^{12} farad-second (4 decades). As in the simulated inductor, the nonideal transadmittance amplifiers cause the D value to be in the error and the quality-factor Q_D to be finite. The Q_D factor was also measured by

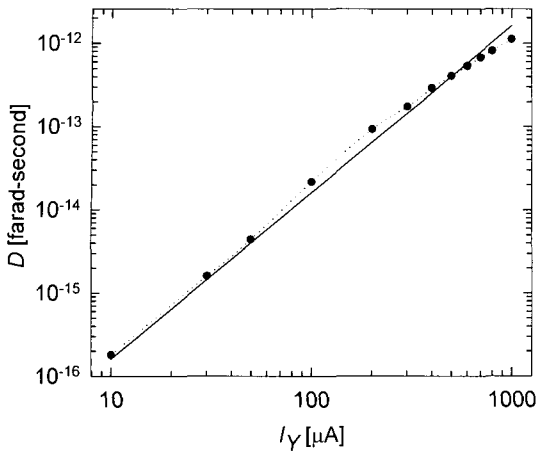

그림 7. <그림 4(c')>에 나타낸 플로팅 FDNR의 바이어스 전류 I_Y에 대한 D.

Fig. 7. Measured D against bias current of the floating FDNR shown in Fig. 4(c').
●●● experimental values
——— theoretical values

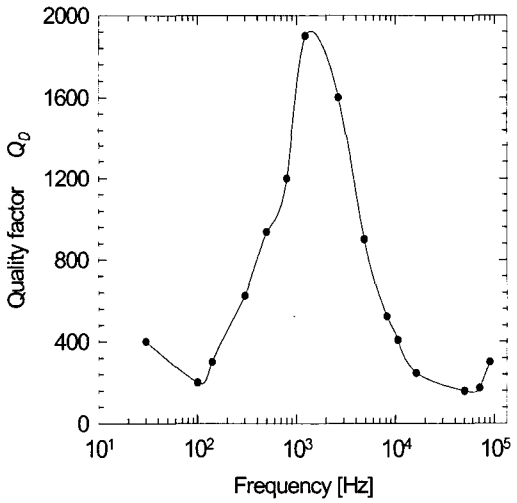

그림 8. <그림 4(c')>에 나타낸 플로팅 FDNR의 Q_D 특성

Fig. 8. Q_D characteristics of the floating FDNR shown in Fig. 4(c').

the series resonance method. The results are plotted in Fig. 8.

This prototype FDNR was applied to the design of a current-controllable band-pass filter. Fig. 9 shows the circuit diagram of the band-pass filter. Here, D represents the floating FDNR shown in Fig 4(c). The frequency response of the band-pass is shown in

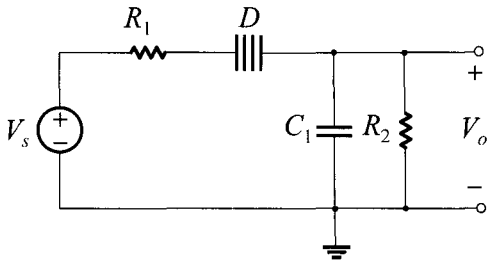

그림 9. <그림 4(c')>에 나타낸 FDNR을 이용한 전류-제어 대역-통과 여파기

Fig. 9. Current-controllable band-pass filter using the FDNR shown in Fig. 4(c'); R_1= 10k, R_2 = 50 k, C_i = 30 nF.

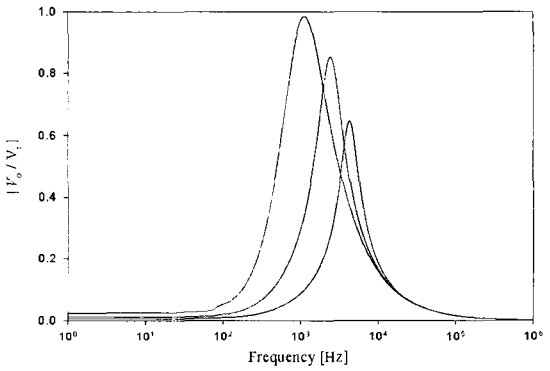

그림 10. 전류 I_Y를 250 μA까지 감소시키므로 중심 주파수가 1.1 kHz에서 4.1 kHz까지 동조하는 대역-통과 여파기의 주파수 응답

Fig. 10. Frequency response of the band-pass with the center frequency tuned from 1.1 kHz to 4.1 kHz by decreasing the current I_Y progressively from 250 μA to 70 μA.

Fig. 10, which demonstrates the tuning of the center frequency via bias current I_Y. The center frequency is tuned from 1.1 kHz to 4.1 kHz by decreasing the current I_Y from 250 A to 70 A progressively while keeping I_X constant (125 A).

V. Conclusions

A systematic synthesis process to design current-controllable inductors using OTAs has been presented. The process has been used to obtain three circuits; two are ground inductors and the other is floating one. The floating inductor circuit has been

implemented using differential-in differential-out OTAs. It features a high Q-factor and simple configuration. Because of these properties, the proposed floating inductor is expected to find wide applications in communication and instrumentation systems. The process to design current-controllable inductors has been also applied to realize current-controllable FDNRs, thereby obtaining three circuits. One of the obtained FDNRs has been applied to design a current-controllable band-pass filter.

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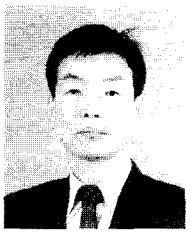

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