Improved Breakdown Voltage Characteristics of $In_{0.5}Ga_{0.5}P/In_{0.22}Ga_{0.78}As/GaAs$ p-HEMT with an Oxidized GaAs Gate

I-H. Kang, J-W. Lee, S-J. Kang, S-J. Jo, S-K. In, H-J. Song, J-H. Kim, and J-I. Song

Abstract— **The DC and RF characteristics of $In_{0.5}Ga_{0.5}P/In_{0.22}Ga_{0.78}As/GaAs$ p-HEMTs with a gate oxide layer of various thicknesses (50 Å, 300 Å) were investigated and compared with those of a Schottky-gate p-HEMT without the gate oxide layer. A prominent improvement in the breakdown voltage characteristics were observed for a p-HEMT having a gate oxide layer, which was implemented by using a liquid phase oxidation technique. The on-state breakdown voltage of the p-HEMT having the oxide layer of 50 Å was ~2.3 times greater than that of a Schottky-gate p-HEMT. However, the p-HEMT having the gate oxide layer of 300 Å suffered from a poor gate-control capability due to the drain induced barrier lowering (DIBL) resulting from the thick gate oxide inspite of the lower gate leakage current and the higher on-state breakdown voltage. The results for a primitive p-HEMT having the gate oxide layer without any optimization of the structure and the process indicate the potential of p-HEMT having the gate oxide layer for high-power applications.**

Index Terms— **InGaP/InGaAs p-HEMT, Oxidation, Breakdowm voltage**

I. INTRODUCTION

Pseudomorphic High Electron Mobility Transistors (p-HEMTs) with InGaAs channel layer have shown superior high-frequency and low-noise performance. However, compared with HEMTs having a GaAs channel, application of p-HEMTs to high power transistors was known to be limited by the enhanced impact-ionization effects, which occur in the narrow band-gap InGaAs channel [1]. The breakdown in p-HEMT having InGaAs channel is attributed to multiplication of electrons which are injected from the gate edge into the high-field drain-gate region of insulator, accelerated by the field and finally injected into the channel with a high energy (hot electron) [2]. Moreover, such multiplication generates holes along with electrons in the vicinity of gate-drain region. The holes are injected back into the gate and source electrodes, leading to a catastrophic increase in drain current. These phenomena can be suppressed by increasing the gate barrier height [3]. There have been many approaches to improve the on-state and the off-state breakdown characteristics of p-HEMTs by using optimized channel structures (e. g., an InGaAs/InP composite channel [1], an InGaAs/InP double channel [4], and a narrow InGaAs channel leading to a larger effective bandgap due to the increase of quantized energy [5]) or by decreasing the electric field in the gate-drain region through a double gate recess process [6] and an optimization of the gate-drain distance [7]. There also have been efforts to implement a metal-oxide-semiconductor (MOS) type gate for compound semiconductor FETs in order to reduce the gate leakage current and thus to improve the breakdown voltage characteristics [8]. The use of a gate oxide layer, which forms a high energy barrier at the gate interface, can prevent injection of electrons caused by thermionic-field

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Department of Information and Communications, Kwangju Institute of Science and Technology (K-JIST), 1 Oryong-dong, Buk-gu, Kwangju, Korea 500-712, e-mail: jisong@kjist.ac.kr.

emission or tunneling at high drain-source voltage. Recently stable operations of GaAs CMOS FETs and depletion-mode GaAs MOS FETs by using Ga_2O_3 (Gd_2O_3) deposited in an ultra-high vacuum chamber connected to MBE growth chamber [9] and a liquid phase oxidized GaAs [10], respectively, were demonstrated.

In this paper, we report characteristics (gate leakage current, breakdown voltage, and microwave characteristics) of p-HEMTs having different gate oxide thicknesses (0Å, 50Å, and 300Å) implemented by the liquid phase oxidation technique.

II. DEVICE STRUCTURE AND FABRICATION

Schematic cross section of $In_{0.5}Ga_{0.5}As/In_{0.22}Ga_{0.78}As/$ GaAs p-HEMTs with the gate oxide layer is shown in Fig. 1. Epitaxial layer structure of the p-HEMTs was grown on a GaAs (100) substrate using a compound-source MBE. The epitaxial layers consist of a 9000 Å undoped GaAs buffer layer, a 100 Å undoped $In_{0.22}Ga_{0.78}$ As channel layer and a 60 Å undoped $Al_{0.25}Ga_{0.75}As$ space layer, a 200 Å $In_{0.5}Ga_{0.5}P$ barrier layer with a Si δ -doping density of 3.4×10^{12} cm^{-2}, and a 300 Å GaAs cap layer.

Three different 1.5x50 μm^2 gate p-HEMTs having the gate oxide layer thickness of 0, 50, and 300 Å were fabricated by using a conventional optical lithography. First, a mesa etching for device isolation was performed by subsequently etching GaAs cap, InGaP barrier, InGaAs channel and GaAs buffer layers using wet etching solutions, and then ohmic contacts were realized by an e-beam evaporation of Ni/Au/Ge/Ni/Au, followed by a rapid thermal annealing for 20 s at 405 ℃. After gate photolithography, selective liquid phase oxidations of GaAs ohmic/oxidation layers were performed for p-HEMTs having a GaAs oxide gate using the gate photoresist pattern as a mask. The liquid phase oxidation was carried out selectively only in the gate region by using a photoresist mask in order to prevent degradation of source and drain ohmic characteristics. A gallium-ion-contained nitric acid solution was prepared by dissolving 5 g of gallium (Ga) in 45 ml of nitric acid at 60 ℃. After dilution of the solution with a de-ionized water

GaAs	Ohmic/Oxidation	300Å	$5 \times 10^{18}/cm^3$
$In_{0.5}Ga_{0.5}P$	Barrier	200 Å	$5 \times 10^{17}/cm^3$
$In_{0.5}Ga_{0.5}P$	Delta-doping	-	$3.4 \times 10^{12}/cm^2$
$Al_{0.25}Ga_{0.75}As$	Spacer	60 Å	undoped
$In_{0.22}Ga_{0.78}As$	Channel	100 Å	undoped
GaAs	Buffer	9000 Å	undoped
(100) Semi-insulating GaAs Substrate			

Fig. 1. Schematic cross section of the $In_{0.5}Ga_{0.5}P/In_{0.22}Ga_{0.79}$ As/GaAs p-HEMT with a gate oxide layer.

(10:1), the pH of the solution was controlled by adding a diluted NH_4OH solution. The oxidation system consists of a temperature-controlled water bath and a pH-meter to monitor the temperature and the pH of the solution during the oxidation process. The GaAs cap layer was oxidized by using the gallium-ion-contained nitric acid solution at the solution temperature of 70℃ and the pH of 4.7. The InGaP barrier layer also served as an oxide stop layer since it had a much lower oxidation rate compared with that of the GaAs ohmic/oxidation layer, resulting in a uniform GaAs oxide layer. After the liquied phase oxidation, a thickness monitoring system (NanoSpec/AFT2100) was used to characterize the thickness of the oxide layers on control samples that underwent identical processing steps. For p-HEMTs having a Schottky-type gate, the GaAs ohmic/oxidation layer was etched to expose the InGaP barrier layer by using a selective wet GaAs etchant ($H_3PO_4/H_2O_2/H_2O$). Finally, Schottky metallization of Ti/Pt/Au was performed by an e-beam evaporation.

III. RESULT AND DISCUSSION

The DC characteristics of $In_{0.5}Ga_{0.5}P/In_{0.22}Ga_{0.78}As/$ GaAs p-HEMTs having the gate oxide layer of 0, 50, and 300 Å were measured by using an HP4155A semiconductor parameter analyzer. Fig. 2 shows the drain current (I_D) and gate current (I_G) as a function of drain voltage for different gate bias voltages of InGaP/InGaAs p-HEMTs having the gate oxide layer of 0 Å, 50 Å, and 300 Å, respectively. The gate leakage current characteristics of p-HEMTs show the dependence of the on-state and off-state breakdown voltage on the

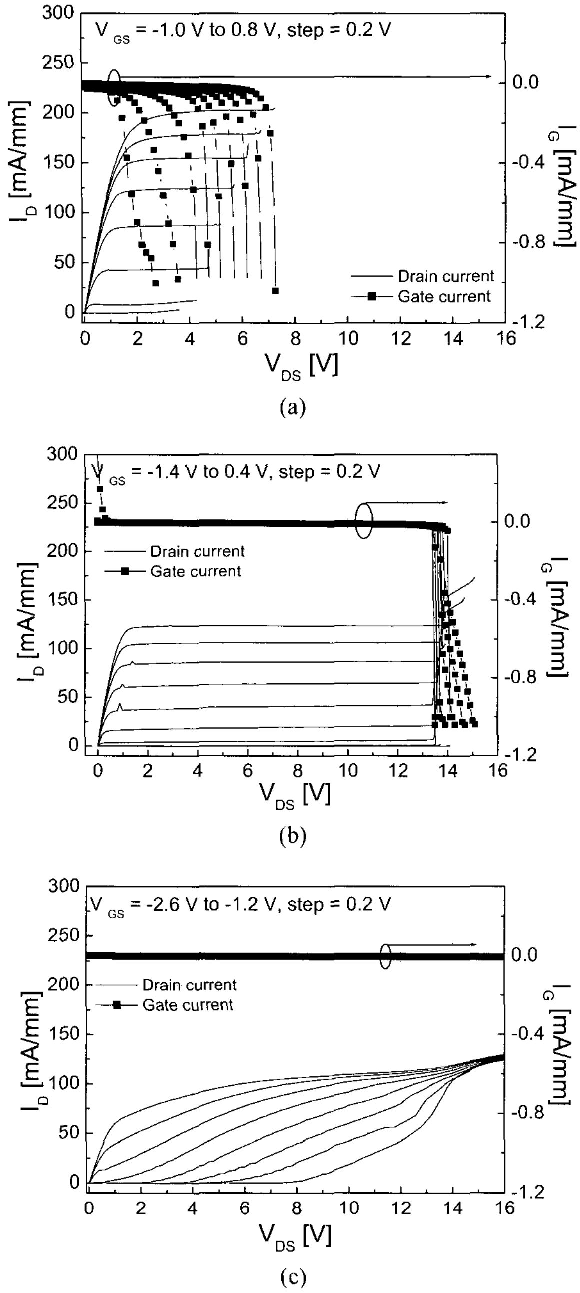

Fig. 2. Drain current (I_D) versus drain bias (V_{DS}) for different gate-source bias voltage (V_{GS}) of $In_{0.5}Ga_{0.5}P/In_{0.22}Ga_{0.79}As$ /GaAs p-HEMTs having the gate oxide layer of (a) 0 Å (Schottky-gate p-HEMT), (b) 50 Å, and (c) 300 Å.

oxide layer thickness. The on-state and the off-state breakdown voltages were defined using a simple, unambiguous, nondestructive gate current extraction technique [11]. The estimated on-state breakdown voltages of the p-HEMTs having the gate oxide layer of 0 Å, 50 Å, and 300 Å were 5.2 V, 13.2 V, and >16 V, respectively. As shown in Fig. 2, the Schottky-gate p-

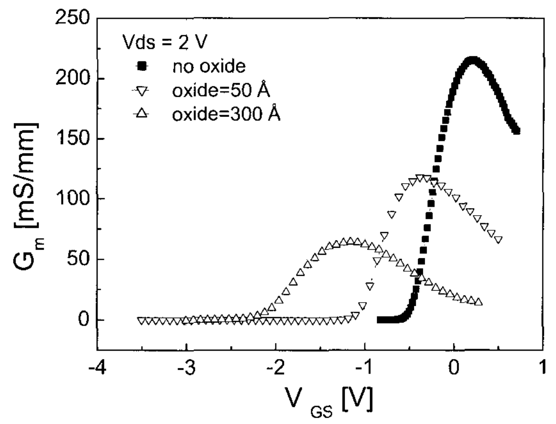

Fig. 3. Transconductance (g_m) as a function of the gate-source bias (V_{GS}) for $In_{0.5}Ga_{0.5}P/In_{0.22}Ga_{0.79}As$/GaAs p-HEMTs p-HEMTs having the gate oxide layer of 0, 50, and 300 Å.

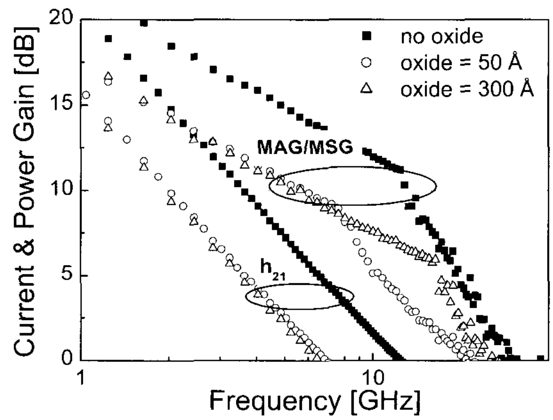

Fig. 4. Current gain (h_{21}) and power gains (MSG/ MAG) for $In_{0.5}Ga_{0.5}P/In_{0.22}Ga_{0.79}As$/GaAs p-HEMTs p-HEMTs having the gate oxide layer of 0, 50, and 300 Å.

HEMT has very low values of the on-state (5.2 V) and the off-state (3.5 V) breakdown voltages, while the p-HEMTs having the gate oxide layer have larger on-state and off-state breakdown voltages. It means the oxide layer induced a substantial improvement in the breakdown voltage by serving a potential barrier for the electrons injected from the gate. However, the HEMT having the gate oxide layer of 300Å suffered from the drain induced barrier lowering (DIBL) [12] at a relatively low drain-source bias voltage of 3.6V due to the presence of the thick gate oxide layer which gives a poorer gate-channel control. The increase in the oxide thickness causes a reduction in the sheet carrier concentration and a vertical electric field under the gate electrode, and finally produces DIBL at lower longitudinal electric field. Fig. 3 shows the normalized transconductance (g_m) of p-HEMTs having different gate oxide thicknesses as a function of the gate-source bias voltage measured at the drain-source bias voltage of 2.0V. The maximum normalized transconductances of p-HEMTs having the gate oxide thickness of 0, 50, and 300 Å were 220, 150, and 75 mS/mm, respectively. The extrinsic transconductance and RF performances of the p-HEMTs having the gate oxide layer were degraded due to the increased distance between the gate and the channel. These performances can be improved by optimization of the epitaxial layer structure of p-HEMTs having the oxide gate layer. The S-parameter measurements of p-HEMTs were performed for frequencies between 1 and 40 GHz using an HP8510C Network Analyzer and an HP4142B DC source. Fig. 4 shows the common-source current gains (h_{21}) and the power gains (*MAG/MSG*) of p-HEMT having different gate oxide thickness measured at the gate-source bias for maximum g_m and the drain-source voltage of 3 V. The cut-off frequencies (f_T) of p-HEMTs having the gate oxide thickness of 0, 50, and 300 Å were 12.4, 7, and 6.8 GHz respectively. Fig. 5 shows the gate-source capacitances of p-HEMTs having the gate oxide thickness of 0, 50, and 300 Å extracted from the measured S-parameters with respect to an effective gate-source bias (V_{GS}-V_T) where V_T is a threshold voltage of p-HEMTs. As shown in Fig. 3 and 5, the degradation of the cut-off frequency for p-HEMTs having the gate oxide layer is attributed primarily to reduction in the ratio of the transconductance to the gate-source capacitance (g_m/C_{GS}). However, the maximum oscillation frequencies

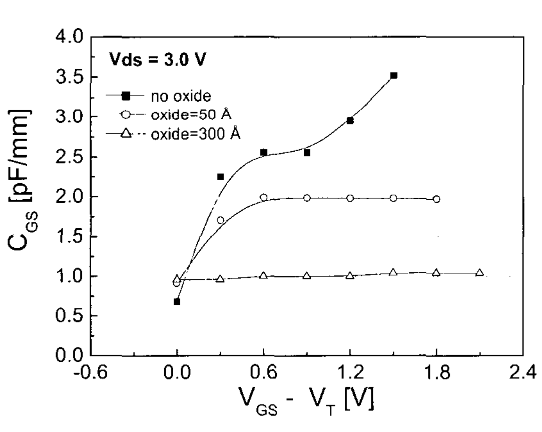

Fig. 5. Normalized gate-source capacitance (C_{GS}) of $In_{0.5}Ga_{0.5}P/In_{0.22}Ga_{0.79}As$ /GaAs p-HEMTs having the gate oxide layer of 0, 50, 300 Å as a function of the effective gate-source bias (V_{GS}-V_T).

(f_{max}) of p-HEMTs having the gate oxide layer were not much degraded compared with that of the Schottky-gate p-HEMT because the feedback capacitance (C_{GD}) decreased with increasing gate oxide thickness.

IV. Conclusion

We first report, to our knowledge, the enhanced on-state and off-state breakdown characteristics of $In_{0.5}Ga_{0.5}P/In_{0.22}Ga_{0.78}As$/ GaAs p-HEMTs having the gate oxide layer of 0, 50, and 300 Å, implemented by the liquid phase oxidation of GaAs. Further improvements in the performance of p-HEMTs having the gate oxide layer can be expected through optimization of the structure of p-HEMTs including the gate oxide layer.

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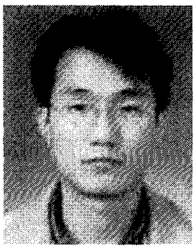
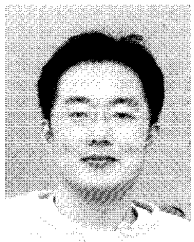


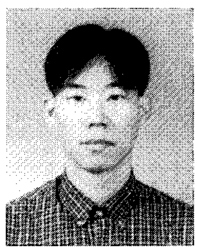
In-Ho Kang He received the B.S. degree from Gyeongsang National University in electronics engineering in 1995 and the M.S. degree from Kwangju Institute of Science and Technology (K-JIST) in Information and Communication in 1998 and currently is taking the doctral course in the same institute. His main concerning is to model HEMT using numerical methods including the Monte Carlo technique and the hydrodynamic model, and to design an MMIC using HEMT.

Jong-In Song He received the B.S. degree from Seoul National University in electronics engineering in 1980 and the M.S. degree from Korea Advanced Institute of Science and Technology in electronics engineering in 1982 and the Ph. D. degree from Columbia University, NY, in electrical and electronics engineering in 1990. From 1986 to 1990 he worked as a graduate research assistant at the Center for Telecommunications Research, where he pioneered high-performance GaAs/AlGaAs two-dimensional-electron-gas (2DEG) charge coupled device research for microwave and infrared imaging applications. He joined the Electronics Science and Technology division at Bellcore, where he worked primary on the development of microwave transistors including GaInP/GaAs, InAlAs/InGaAs, InP/InGaAs HBTs and their application to MMICs from 1990 to 1994. He was also involved in the research on the MMICs for phase arrayed antenna T/R modules that incorporate InP/InGaAs HBTs for SSPA and InAlAs/InGaAs HEMTs for LNA monolithically. He joined Kwangju Institute of Science and Technology (K-JIST) in 1994 and is currently a professor in the department of Information and communications, His current research interests include growth of InP and GaAs-based epi structures for millimeter-wave device applications using chemical beam epitaxy and molecular beam epitaxy systems, design, fabrication, and characterization of millimeter-wave devices (HEMT's and HBT's) and MMICs for broadband wireless multimedia services. He is also interested in the development of O-E and E-O tranceivers for millimeter-wave over fiber system.

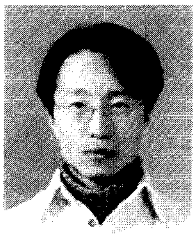


Jae-Woo Lee(J-W. Lee) He received the B.S. degree in electrical engineering from Korea University, Seoul, Korea, in 2000, and the M.S. degree in information and communication engineering from Kwang-Ju Institute of Science and Technology (KJIST), Gwangju, Korea, in 2002. In September 2002, he joined the Electronics and Telecommunications Research Institute as a member of engineering staff, where he worked with the Basic Research Lab, focusing on RF MEMS devices. Currently, his research interests include the design, fabrication, and characterization of microelectromechanical devices, especially RF MEMS switches, and systems for applications to telecommunications devices.

Shin-Jae Kang(S-J. Kang) He received the B.S. degree in semiconductor science from Chungpook National University, Chungju, Korea, in 1997 and and M.S. degree in information and communication engineering from KJIST, Gwang-ju, Korea, in 1999. He is pursuing the Ph. D. degree in the Department of Information and Communications in KJIST.

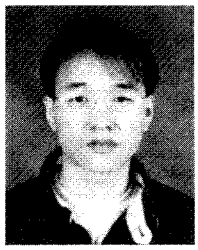


Seong June Jo(S-J. Jo) He received the B.S. degree in electronics engineering from Gyeongsan National University, Jinju, Korea, in 1997, and the M.S. degree in Information and Communications from Kwangju Institute of Science and Technology(KJIST), Kwangju, Korea, in 1999, where he is currently pursuing the Ph. D. degree in the Department of Information and Communications. His research interest include growth of InP and GaAs-based epi structures for millimeter-wave device and optoelectronics applications using a molecular beam epitaxy.



Soo-Kang In(S-K. In) He was born in Deagu, Korea, in 1973. He received the B.S. degree in electronic engineering from Kyungpook National University, Deagu, Korea, in 1999 and and M.S. degree in information and communication engineering from KJIST, Gwang-ju, Korea, in 2001. He is pursuing the Ph. D. degree in the Department of Information and Communications in KJIST. His research interest includes growth of InP and GaAs-based heterostructures for millimeter-wave device and optoelectronic device applications using MBE.

Ho-Jin Song(H-J. Song) He received the B.S. degree in electronic engineering from Kyungpook National University, Deagu, Korea, in 1999 and and M.S. degree in information and communication engineering from KJIST, Gwang-ju, Korea, in 2001. He is pursuing the Ph. D. degree in the Department of Information and Communications in KJIST.



Jeong-Hoon Kim(J-H. Kim) He received the B.S. degree from Hongik University, in electronic engineering in 1998 and the M.S. degree from Kwangju Institute of Science and Technology (K-JIST) in information and communications in 2000. He is currently pursuing a Ph.D. degree in the department of Information and Communications, Kwangju Institute of Science and Technology. His research areas include characterization of millimeter-wave device (HEMTs and HBTs), design, fabrication, and characterization of MMICs for broadband wireless communication system.