CCD Image Sensor with Variable Reset Operation

Sangsik Park and Hyung Soo Uh

Abstract— **The reset operation of a CCD image sensor was improved using charge trapping of a MOS structure to realize a loe voltage driving. A DC bias generating circuit was added to the reset structure which sets reference voltage and holds the signal charge to be detected. The generated DC bias is added to the reset pulse to give an optimized voltage margin to the reset operation, and is controlled by adjustment of the threshold voltage of a MOS transistor in the circuit. By the pulse-type stress voltage applied to the gate, the electrons and holes were injected to the gate dielectrics, and the threshold voltage could be adjusted ranging from 0.2V to 5.5V, which is suitable for controlling the incomplete reset operation due to the process variation. The charges trapped in the silicon nitride lead to the positive and negative shift of the threshold voltage, and this phenomenon is explained by Poole-Frenkel conduction and Fowler-Nordheim conduction. A CCD image sensor with 492(H) × 510(V) pixels adopting this structure showed complete reset operation with the driving voltage of 3.0V. The resolution chart taken with the image sensor shows no image flow to the illumination of 30 lux, even in the driving voltage of 3.0 V.**

Index Terms— **CCD, image sensor, reset, capability, potential, hot electron, charge injection, threshold voltage, MOS transistor**

I. Introduction

CCD image sensors are widely used as a solid-state imaging component for camera and broadcasting video camera systems because of their high signal to noise ratio [1]. CCD image sensor handles electrons as an image signal, so it is insensible to the noise of voltage. The trend of the image sensor development has been focused on low driving voltage, however, low driving voltage causes narrow voltage margin. The narrow swing of the pulse can lead to incomplete operation of switching transistor.

The reset operation which sets reference voltage and holds the signal charge to be detected is the most sensitive to the voltage margin. This operation can be optimized by a DC bias added to the driving pulse, and the bias is generated internally in the chip. Conventional method generating the bias is to use the electrical fuses, which generates discrete DC values only. The adjustment of the threshold voltage by the gate current of a MOS transistor[2] for reset operation is the precise method to guarantee the complete reset operation.

The holes and electrons injected to the gate of MOS structure make traps in the insulator or are trapped in the interface states of the insulator layer.[3, 4] A great deal of effort has been spent on the studies of electron and hole injection for MOS devices under stress, and the involved threshold shift mechanisms are well understood. [5, 6] At low gate voltage, the holes injected from the gate create the electron traps which form positively charged centers.[5-9]. At high gate voltages, injected electrons from the silicon to the oxide are trapped in the interface states, and these electrons form negative charge[8, 10-13]. The injected holes and electrons induce the threshold shift which controls the output voltage of the DC bias generating circuit. This output voltage is added to the driving pulse of the output structure, and controls the potential barrier of the potential well for the signal charges to be detected.

We introduce the limitation of the reset operation and DC controlling method with analysis of charge trapping. The result of applying the new structure is verified by

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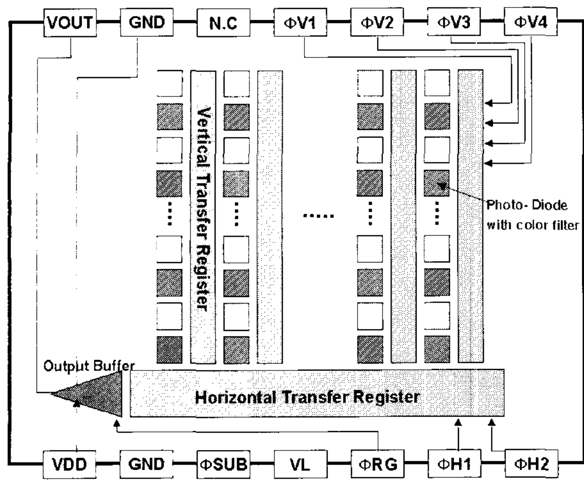


Fig. 1. Block diagram of a CCD image sensor.

the image which has no distortion at the bright illumination.

II. LIMITATION OF THE RESET OPERATION

Fig. 1 shows a block diagram of a CCD image sensor. The signal electrons to be detected in the output structure are generated in the pixels by the incident light and transferred to the CCD channel. A pixel is consists of micro-lens, color filter, photodiode, and transfer gate. The incident light is filtered by the R, G, B color filter, and focused on the photodiode by the micro-lens. The light generates the electron-hole pairs in the photodiode, and the electrons are integrated in the n-type of the photodiode for 1/30 second. The holes are swept out to the grounded p-type of the photodiode. The integrated electrons are transferred to the CCD channel by the pulse applied to the transfer gate every 1/30 second. These signal electrons are conveyed to the output amplifier through the vertical and horizontal CCD channel.

Fig. 2(a) shows the electron-voltage conversion part of the CCD image sensor. The signal electrons transferred from the pixels by the clock φ1, φ2 of the horizontal CCD are injected to the floating diffusion(n+) over the output gate(OG). The potential of the floating diffusion is modulated in proportion to the number of the electron injected. The potential change of the floating diffusion is detected by the source follower as a unit of voltage. After the detection of the voltage, the injected electrons in the floating diffusion are removed by the operation of

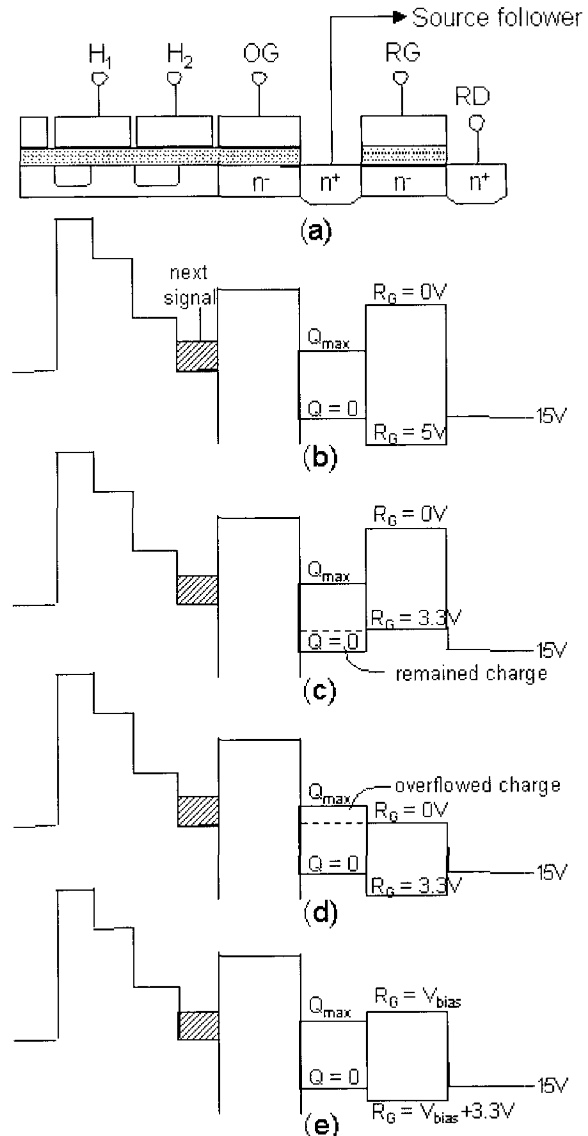


Fig. 2. Electron-voltage conversion part of the CCD image sensor. (a) Cross section of reset structure, potential diagram of the output structure with the reset voltage (b) of 0-5V, (c) of 0-3.3V causing overflow, (d) of 0-3.3V remaining charge and (e) of 0-3.3V added DC bias.

the reset gate(RS) and reset drain(RD), and the voltage of the floating diffusion is set to be equal to the reset drain for the next signal charges[14].

Fig. 2(b) shows the potential diagram of the output structure with the reset voltage of 0-5V. When the reset voltage is 0V, the signal charge is injected from φ2 channel to FD over the OG and stayed there for detection. After the detection of the voltage of the FD, the voltage of the reset gate becomes 5V. The whole signal charge swept out completely by the reset drain voltage of 15V.

The reset voltage of 0-3.3V is used recently to reduce

the operation voltage. Fig. 2(c) shows the potential diagram of the output structure which is operated with the reset voltage of 0-3.3V. The low level of the reset voltage is 0V, which is same to (b). Therefore there is no problem in keeping the signal charge to be detected. But the high level of reset voltage became 3.3V, this causes incomplete sweep-out operation. The remained charge distorts the detection of the next signal charge.

The threshold voltage of reset transistor can be controlled to lower voltage to make complete sweep-out operation as shown in Fig. 2(d). The potential diagram shows the threshold voltage of the reset transistor was adjusted too low. Too low threshold voltage leads to overflow of the signal charge before the detection.

In conclusion, the reset voltage of 0-3.3V has very narrow voltage margin, which can cause incomplete sweep-out or overflow of signal charge. The fixed DC bias can not solve this problem since the threshold voltage of the image sensors fabricated by one process are not uniform because of the process variation. The DC bias(V_{bias}) must be tuned for each device to insure the optimized reset operation as shown in Fig. 2(e). The DC bias added to the reset pulse brings the optimized margin in the reset operation.

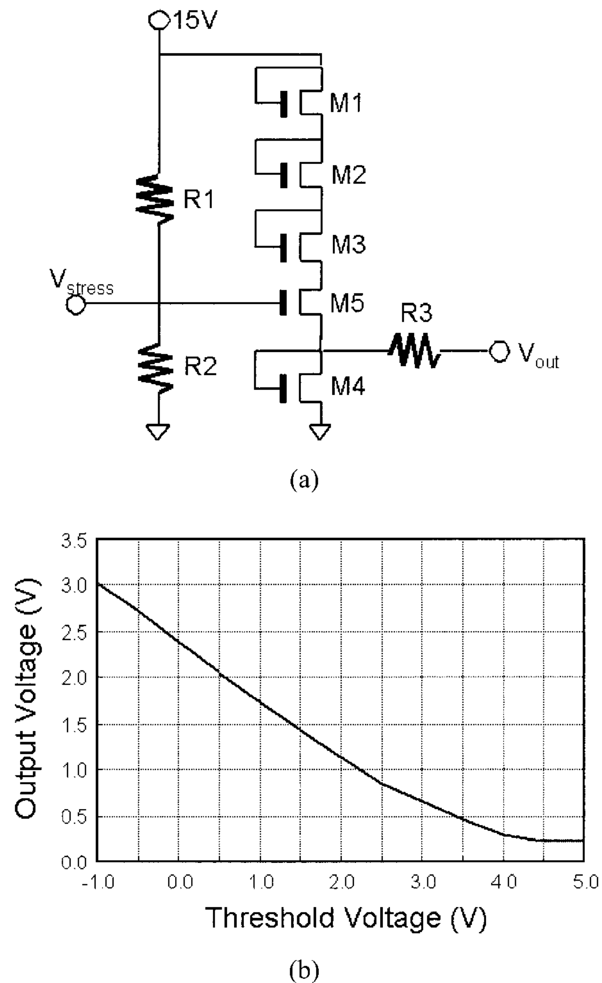


Fig. 3. (a) DC generating circuit and (b) relation between threshold voltage and output voltage. The output voltage is determined by adjusting the threshold voltage of transistor M5.

III. EXPERIMENTAL

Fig. 3(a) shows the circuit generating the DC bias for reset gate. V_{stress} node is for adjusting the threshold voltage of the transistor M5. Transistors M1-M4 is to control the DC level of the voltage of V_{out}, and resistors R1 and R2 is to give the gate voltage of the transistor M5, and R3 is inserted for AC voltage of φ_{RG} to be applied to the gate of RG.

Fig. 3(b) shows the relation between the threshold voltage of M5 and V_{out} node. Appropriate center value of DC level is 1.2V, and we assume the process can make 0.5V variation of the threshold voltage of reset transistor. Therefore, the output range of 0.2-3V is suitable to this structure.

The n-channel MOSFET's were fabricated on p-type well which was formed by boron diffusion on n-type 10Ω.cm substrate using conventional CCD process. The gate insulator of the MOS transistor used in this study is composed of 300Å silicon oxide and 300Å nitride on it[15]. The gate oxides were grown to 300Å by dry oxidation at 1000°C, and gate nitrides were deposited to 400Å by LPCVD on it. An LPCVD polysilicon gate of 400Å was deposited on it and doped with $POCl_3$ gas. The S/D n+ region was formed by arsenic implantation with a dosage of $5\times10^{15}/cm^2$ at 70 keV and the resulting junction depth is 0.12 μm.

The stress was carried out with all the terminals grounded except the stress terminal(V_{stress}) in fig. 3(a) at room temperature. The pulse duration was 300 ms for each voltage and the rise and fall time for the gate pulses were 1 ms. These stresses were all followed by a measurement of threshold voltage of M5 transistor and output voltage in Fig. 3(a). The threshold voltage was estimated by maximum slope extrapolation to zero drain current.

IV. Results And Discussion

Fig. 4 shows the threshold voltage of M5 and output voltage of the circuit as a function of stress voltage applied during 300 ms for each point. The threshold voltage decreases by the stress voltage below 32V. This is explained by the Poole-Frenkel conduction[16] which is based on the capture and emission of carriers from trap levels in the bulk of the dielectric. Silicon nitride contains a high density of structural defects, and these defects cause additional energy states close to the bandedge which permits the carriers to move in the nitride. Electrons are absorbed to the gate, and holes are drifted to the interface of nitride and oxide. These holes are recombined or captured on the interface traps. All of these movements result in the decrease of the threshold voltage[14].

The increase of the threshold voltage under the stress voltage over 32V can be explained by the Fowler-Nordheim tunneling[18]. The electrons are tunneled to the silicon oxide from bulk silicon, and moved to the oxide-nitride interface. Some electrons are recombined with the holes trapped in the oxide, and others are injected to the nitride and captured in the deep trap level in the nitride. The emission of the electrons is very hard even in the large field since these levels are very deep. This causes a fixed charge in the silicon nitride which remains even when the applied bias is removed.

At the stress voltage of 36V, the electric field in oxide is 8 MV/cm, and the F-N tunneling current is about 5× 10^{-7} A/cm^2[19]. If all the charge supplied by the current is trapped in the oxide-nitride interface, the shift of threshold voltage by a pulse(300ms) is calculated as following:

$$\Delta V_{TH} = \frac{I_{FN} \cdot A \cdot T_d}{\varepsilon_{ox} \cdot A / t_{ox}} \quad (1)$$

where I_{FN} is the F-N current, A is the area of the gate, T_d is the pulse duration, ε_{OX} is the permittivity of the silicon dioxide and t_{OX} is the thickness of the oxide. In this experiment, the thickness of the oxide is 300Å, and the pulse duration is 300ms. The equation gives 1.3V of threshold voltage shift, on the other hand the graph of Fig. shows 0.4V of threshold voltage shift. About 30% of supplied charge is effectively trapped in the interface of oxide-nitride.

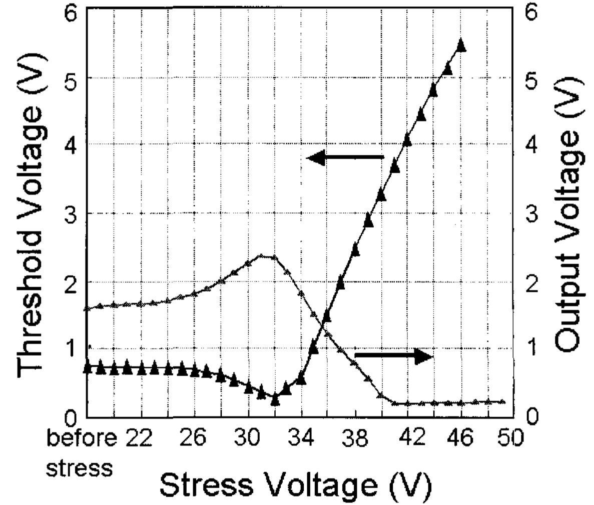


Fig. 4. Threshold voltage of M5 and output voltage of the circuit as a function of stress voltage applied during 300 ms for each point.

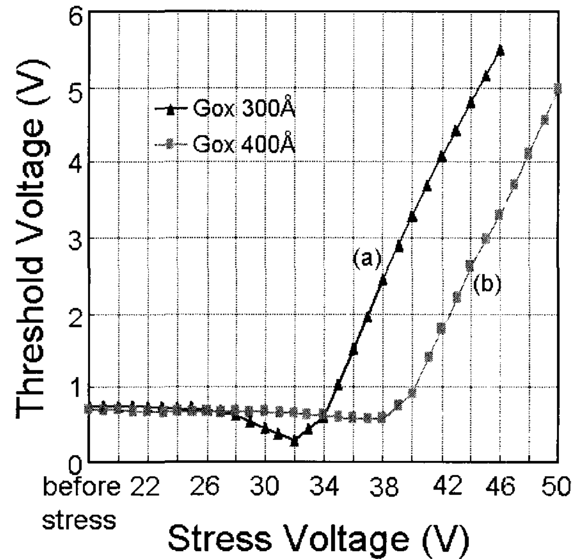


Fig. 5. Threshold voltage of MOS structure with nitride/oxide thickness of (a) 300/300Å and of (b) 300/ 400 Å as a function of stress voltage.

Fig. 5 shows the shift of the threshold voltage by the gate stress for the nitride/oxide thickness of 300/300Å (a) and 300/400Å (b). One point is corresponding to the pulse of 300ms duration. For the oxide thickness of 300Å, stress voltage of 40V induces the electric field of 8.8MV/cm in the oxide layer. For the oxide thickness of 400Å, the stress voltage which induces the oxide electric field of 8.8MV/cm is 48V, and it makes the threshold

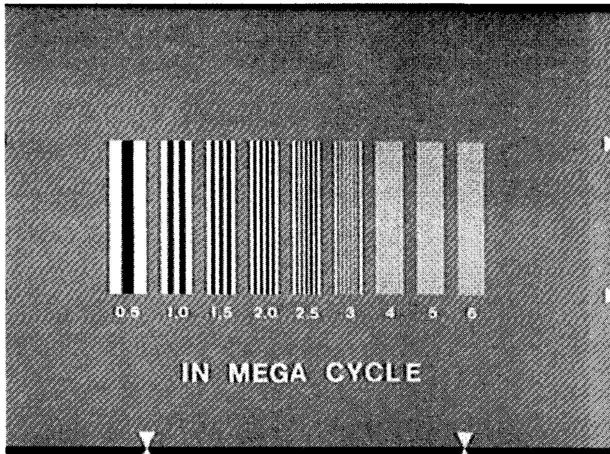


Fig. 6. Reproduced image of resolution chart taken with the image sensor with the driving voltage of 3.0V. The shallow black and white pattern was not mixed by the remained charge in the output structure, since the signal charge was swept out completely.

shift of 4V, which is larger than the case of the oxide thickness of 300Å. That difference of the shift is due to the difference of the stress time, that is, the time for the stress voltage to reach 48V in the case of the oxide thickness of 400Å is longer by 2.4 sec than the time for the stress voltage to reach 40V in the case of the oxide thickness of 300Å. The threshold shift is increased by the electric field of the oxide and the stress time.

To verify the effect of the oxide electric field to the threshold shift, we compared the threshold shift by the pulse of equal duration and electric field in the different oxide thickness. For the oxide thickness of 300Å, the threshold shift is 2.5V in the stress voltage ranging from 36V to 42V, which is correspond to the oxide electric field ranging from 7.9 MV/cm to 9.2 MV/cm. For the oxide thickness of 400Å, the oxide electric field ranging from 7.9 MV/cm to 9.2 MV/cm is corresponding to the stress voltage ranging from 44V to 50V. The stress time is equally 1.8 sec.

The threshold shift is 2.4V for the oxide thickness of 400Å, which is similar to the case of the oxide thickness of 300Å. That is, the same electric field induces similar threshold shift in the same stress time even in the different oxide thickness. Therefore, the increase of the threshold voltage by the high voltage stress is due to the Fowler-Nordheim tunneling.

The 1/4"-optical size CCD image sensors with 492×510 pixels were fabricated using the optimized output structure. The color was green, cyan, magenta and yellow, and microlenses were formed on it. The frame rate is 60 frames/sec which corresponds to NTSC system.

Fig. 6 shows a resolution chart taken with this image sensor with the horizontal driving voltage of 3.0V. The shallow black and white pattern can be mixed by the remained charge of the output structure if the reset operation is incomplete. This image shows no mixed-signal since the signal charge was swept out completely.

V. CONCLUSION

The threshold voltage of a transistor in the CCD image sensor was adjusted by the gate stress to add a optimized DC bias to the pulse of reset operation of output structure. The purpose of this DC bias is to handle the large amount of the signal electrons in low voltage CCD image sensor. The stress voltage ranging from 32V to 50V resulted in the injection of holes and electrons to the gate dielectrics, and the threshold voltage was shifted ranging from 0.2V to 5.5V, which is suitable for the stable 3V-operation of reset structure. The shift of threshold voltage was explained by the Poole-Frenkel conduction and Fowler-Nordheim conduction. The image sensor utilizing the adjusted DC bias was operated with the driving voltage of 3.0V without image distortion. The shallow black and white pattern was not mixed by the remained charge in the output structure since the signal charge was swept out completely.

REFERENCES

[1] E. R. Fossum, "CMOS image sensor: electronic camera-on-a-chip", IEEE Trans. Electron Dev., **44**, 1689 (1997).

[2] Y. Lee, S. Sung, J. Sim, C. Lee, T. Kim, J. Lee, B. Park, D. Lee and Y. Kim, "Multi-level Vertical Channel SONOS Nonvolatile Memory using a Standard SOI Logic Process", J. Korean Phys. Soc., **41**, 908 (2002).

[3] C. Hu, "Hot-Electron affects in MOSFET's", IEDM Tech. Dig. 176 (1983).

[4] F. Driussi, D. Esseni, L. Selmi and F. Piazza, "Damage Generation and Location in n- and p-MOSFETs Biased in the Substrate-Enhanced Gate Current Regime", IEEE Trans. Electron Dev., **49**, 787 (2002).

[5] Z. Ma, P. Lai, Z. Liu, P. Koand Y. Cheng, "Mechanisms

for Hot Carrier Induced Degradation in Reoxidized Nitrided Oxide n-MOSFET's under Combined AC/DC Stressing", IEEE Trans. Electron Dev., **40**, 1112 (1993).

[6] C. Hu, S. Tam, F. Hsu, P. Ko, T. Chan and K. Terrill, Hot Electron induced MOSFET Degradation – Model, monitor, and improvement", IEEE Trans. Electron Dev., **32**, 375 (1985).

[7] K. Mistry and B. Doyle, "The Role of Electron Trap Creation in Enhanced Hot Carrier Degradation During AC Stress", IEEE Electron Dev. Lett., **11**, 267 (1990).

[8] B. Doyle, M. Bourcerie, C. Bergonzoni, R. Benecci, A. Bravis, K. Mistry and A. Boudou, "The Generation and Characterization of Electron and Hole Traps Created by Hole Injection During Low Gate Voltage Hot-Carrier Stressing of n-MOS Transistors", IEEE Trans. Electron Dev., **37**, 1869 (1990).

[9] P. Bellens, P. Heremans, G. Groeneseneken, and H. Maes, "Hot carrier effects in n-channel MOS transistors under alternate stress conditions", IEEE Electron Dev. Lett., **9**, 232 (1988).

[10] S. Wang, J. Sung and S. Lyon, "Relationship between hole trapping and interface state generation in metal-oxide silicon structures", Appl. Phys. Lett., **52**, 1431 (1988).

[11] W. Weber, "Dynamic Stress experiments for understanding hot carrier degradation phenomena", IEEE Trans. Electron Dev., **35**, 1476 (1988).

[12] J. Choi, P. Ko and C. Hu, "Hot carrier induced MOSFET Degradation under AC Stress", IEEE Electron Dev. Lett., **8**, 333 (1987).

[13] B. Doyle, M. Bourcerie, J. Marchetaux and A. Boudou, "Dynamic Channel Hot carrier degradation of NMOS transistors by enhanced electron-hole injection into the oxide", IEEE Electron Dev. Lett., **8**, 237 (1987).

[14] S. Park, H. Uh, S. Choi and J. Nam, "High Sensitivity CCD Image Sensor using Capacitive Inverted Feedback Source Follower Circuit", J. Korean Phys. Soc., **41**, 547 (2002).

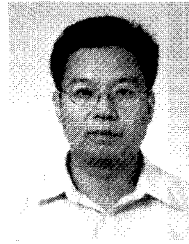
[15] J. Kim, Y. Moon, J. Choi, B. Shin, I. Choi and K. Park, "Charge Loss Mechanisms in a Stacked Gate Flash EEPROM Cell with a ONO Inter-Poly Dielectric", J. Korean Phys. Soc., **39**, 1103 (2001).

[16] M. Aminzadeh, S. Nozaki and R. Giridhar, "Conduct ion and Charge Trapping in Polysilicon-Silicon Nitride-Oxide-Silicon Structures Under Positive Gate Bias", IEEE Trans. Electron Dev., **35**, 459 (1988).

[17] W. Zhu, T. Ma, T. Tamagawa, J. Kim and Y. Di, "Current transport in metal/hafnium oxide/silicon structure", IEEE Trans. Electron Dev. Lett., **23**, 97 (2002).

[18] W. Brown and J. Brewer, "Nonvolatile Semiconductor Memory Technology", Chap. 1

[19] Yuan Taur and Tak H. Ning, "Fundamentals of Modern VLSI Devices", Cambridge Univ. Press, (U.K. 1998), Chap. 2.4, pp. 95-96.



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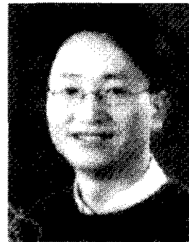

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