A design of 16-bit adiabatic Microprocessor core

Youngjoon Shin, Hanseung Lee, Yong Moon, and Chanho Lee

Abstract— **A 16-bit adiabatic low-power Microprocessor core is designed. The processor consists of control block, multi-port register file and ALU. A simplified four-phase clock generator is designed to provide supply clocks for adiabatic processor. All the clock line charge on the capacitive interconnections is recovered to recycle the energy. Adiabatic circuits are designed based on ECRL(efficient charge recovery logic) and 0.35㎛ CMOS technology is used. Simulation results show that the power consumption of the adiabatic Microprocessor core is reduced by a factor of 2.9~3.1 compared to that of conventional CMOS Microprocessor**

Index Terms— **adiabatic circuits, microprocessor, ECRL**

I. Introduction

In recent years, studies on adiabatic computing have been grown for low power systems and several adiabatic logic families are proposed [1-7]. This is very useful such as hand held computers and PDAs. In order to realize a complete system such as a Microprocessor, large macro blocks are necessary as a building block.

Most adiabatic circuits need AC-type supply to recycle the energy. A method based on adiabatic technique uses an AC power supply for the recovery of energy and an efficient supply clock generator is essential to show the feasibility of adiabatic circuits.

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A Microprocessor core for a 16-bit RISC Microprocessor is designed based on the adiabatic concept and an efficient clock generator with the controllable driving capability for adiabatic circuits is also designed.

II. Adiabatic Microprocessor Macroblocks

ECRL(Efficient Charge Recovery Logic) [8] type adiabatic logic families are used in this paper and AC-type supply clocks are needed to supply power. Adiabatic circuits require four-phase sinusoidal clocks for cascading logic stages. ECRL adiabatic circuits use a differential signal scheme.

The designed Microprocessor consists of a Control Unit, Register File, Shifter and ALU.The block diagram of the Microprocessor is shown in Figure 1.

The ALU executes addition, subtraction and logic operation. The subtraction operation needs a carry input signal and inversion gates so the subtraction result is obtained in seven phases. The gate count optimization is performed to reduce the power consumption. The total gate number of the proposed adder is reduced by a factor of 10% compared to the previous adiabatic adder[8]. The

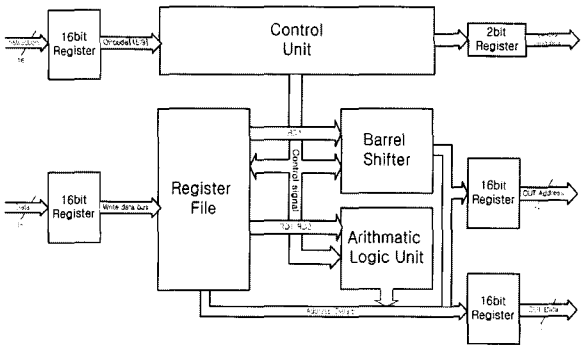

Fig. 1. The structure of Microprocessor

Shifter executes shift and rotate operation and Control Unit takes the charge of the phase matching and supply selection signals.

The ALU consists of 16-bit CLA with subtraction logic, 16-bit logical unit and MUX. Figure 2 shows the block diagram of ALU [10].

The 16-bit Barrel Shifter is designed suitable for pipelining structure. The block diagram of 16-bit Barrel Shifter is shown in figure 3. This structure is effective to reduce phases.

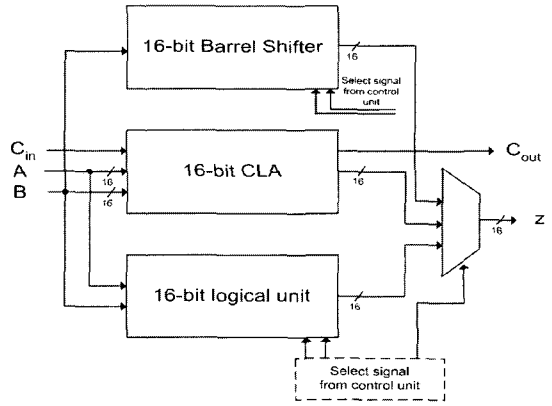

Fig. 2. The structure of Shifter and ALU

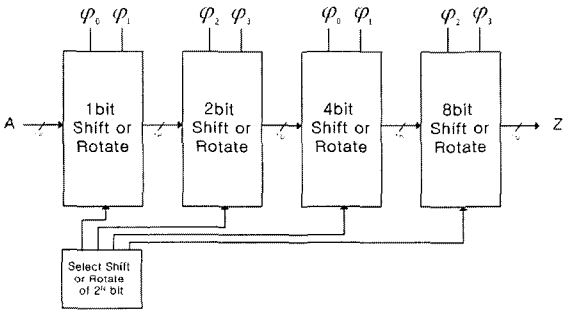

Fig. 3. The structure of 16-bit barrel shifter

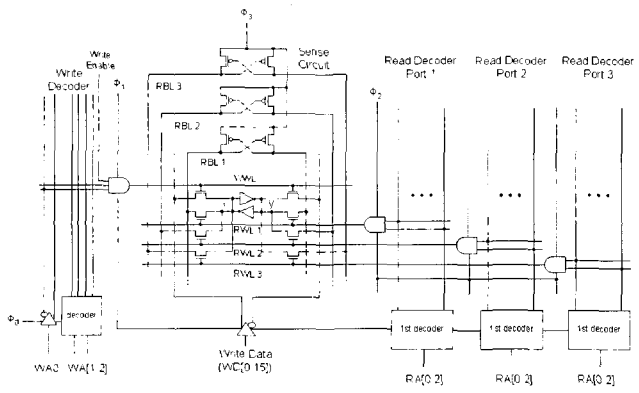

Fig. 4. The structure of adiabatic register file

The 3-read and 1-wirte multi-port register file is designed in adiabatic manner to reduce energy. The cell structure of multi-port register file is shown in Figure 4. A 3-bit is used for register addressing and cross-coupled PMOS is used as a sense circuit to recover the charges in bit-lines. The write operation needs 2 phases and the read operation is composed of 3 phases. The read operation has an one-phase delay from the beginning of the write operation, so reading the updated data in the same cycle is possible in this register file.

III. Supply Clock Generator

The AC supply is needed to return the delivered energy back to the supply efficiently. The LC resonant circuit is used to supply 4-phase supply clocks. Figure 5 shows the block diagram of supply clock generator.

It consists of one inductor, two capacitors and MOS

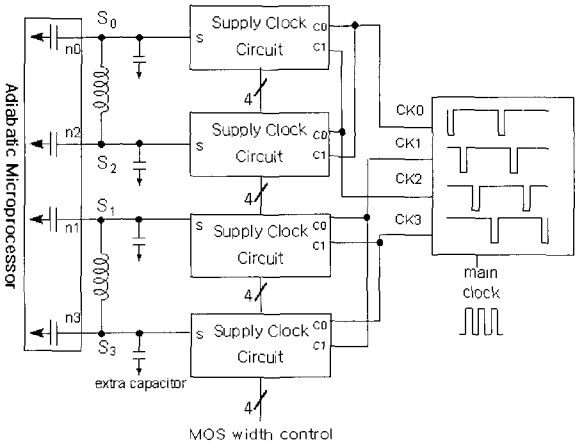

Fig. 5. The block diagram of supply clock generator

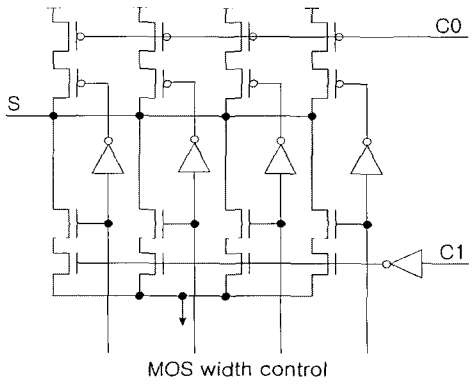

Fig. 6. The schematic of supply clock circuit

switches. The switch transistors shown in Figure 6 are connected to the supply and are used to maintain the swing of supply clocks by compensating the energy loss.

The operating frequency of Microprocessor core is determined by the resonant frequency calculated from the external inductance and the equivalent capacitance of the supply clock node. The equivalent capacitance of the supply clock node is calculated using the equation $f=1/RC_{eq}$. Table 1 shows the calculated equivalent capacitances of supply clock nodes for adiabatic Microprocessor core.

Since the equivalent capacitances of the supply clock nodes are different, small external capacitors are added to match the capacitances of the supply clock nodes. The amplitude of the supply clock grows as the DC power supplies energy through the MOS switches.

IV. Simulation Results

The energy dissipation of ECRL inverter circuit is shown in Figure 7. The energy graph shows that energy is recovered as the voltage of the supply clock goes down. The energy consumption calculated by integrating the product of voltage and current .

The 16-bit adiabatic Microprocessor core is fabricated by 0.35μm CMOS MPW program of IDEC, and SPICE simulation is carried out using the layout extracted net-list. A conventional CMOS processor with the single-ended signal scheme is also designed to compare the power consumption. The CMOS Microprocessor core for the energy comparison is designed by removing the latches and adding flip flops.

Table 1. The equivalent capacitance of supply clock node

node	S0	S1	S2	S3
C_{eq} [pF]	1.67	2.80	1.16	2.26

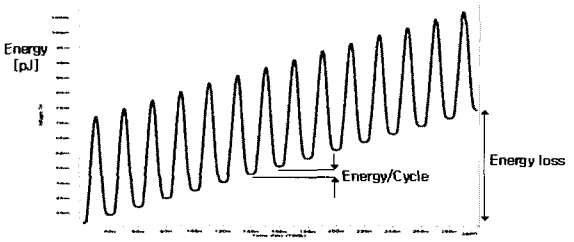

Fig. 7. Energy recovery plot of ECRL inverter

The efficiency of the supply clock generator is varied according to the size of switching transistors, and is simulated by changing the combination of the switching transistors. The size of the switching transistor increases as the operation frequency goes up. This trend shows that the larger current is needed for the higher frequency operation.

In this paper, several NMOS sizes are tested for high energy efficiency in 50Mhz. When the width of NMOS is 40μm, the optimal efficiency is obtained.

The operation of register file is shown in Figure 8. Reading operations are carried out for each read port, after writing '10100110' to the register sequentially.

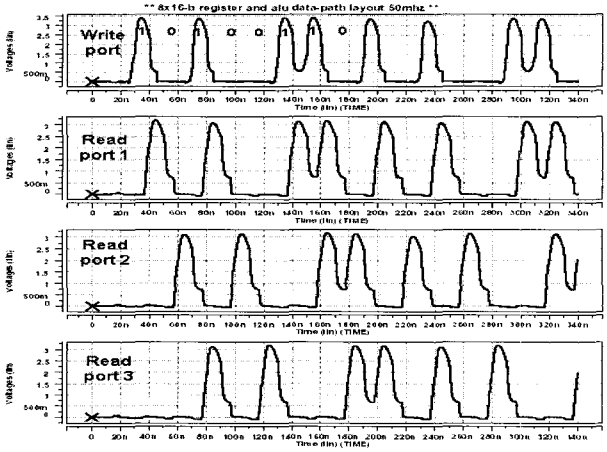

Fig. 8. The simulation result of adiabatic register file

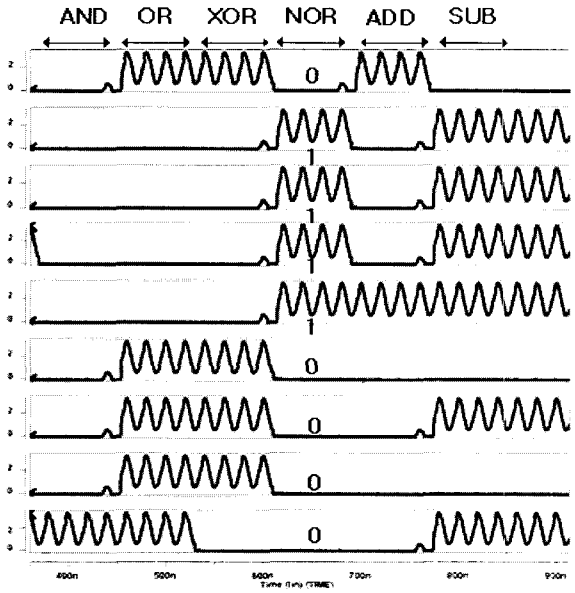

Fig. 9. The simulation result of Microprocessor core

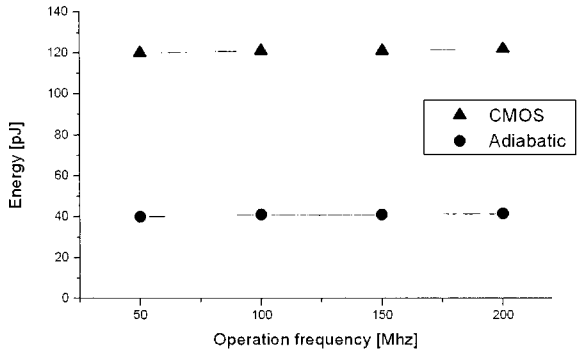

Fig. 10. Energy versus operation frequency for CMOS and adiabatic Microprocessor core

The operation of arithmetic and logic is shown in Figure 9.

According the test instruction codes, figure 9 shows the lower 9-bit operation results of two registers (R1, R2).

Register "R1" equal '0000010000000011', and register "R2" equal '0000000100001101'. The result of NOR operation is displayed in figure 9.

The energy consumption of the ECRL and the conventional CMOS Microprocessor core is compared in Figure 10. The core energy comparison is carried out with varying the operation frequency. The energy consumption of the adiabatic Microprocessor core is about 39%~41% of that of CMOS Microprocessor core.

V. Chip Implementation And Test Result

A 16-bit adiabatic Microprocessor core is designed by full-custom method. The chip layout is shown Figure 11. The size of chip is 4mm x 4mm and the package type is used 100-pin QFP. A 0.35㎛ CMOS 1-poly and 3-metal process is used.

The test setup of the fabricated chip comprises Pattern Generator for input data, function generator for four-phases clock, oscilloscope, Logic Analyzer and DC power supply. Figure 12 shows the block diagram of chip test environment. The several test steps are performed to analyze the fabricated IC. Some blocks show the operation of chip, but the operation of full chip is not verified. The more experiment time is needed to evaluate the chip and find the cause of this failure.

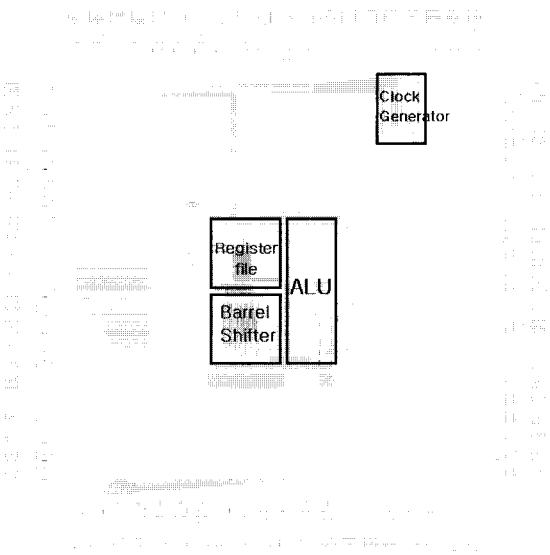

Fig. 11. The chip layout of 16-bit Microprocessor

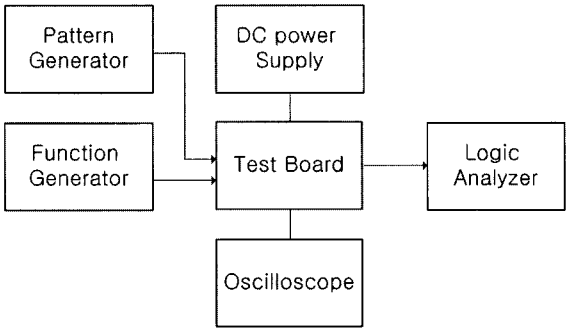

Fig. 12. The block diagram of chip test environment

VI. Conclusions

An adiabatic Microprocessor core and a supply clock generator are designed using 0.35㎛ CMOS technology. The energy and functional simulation is performed using the net-list extracted from the layout. The energy consumption of the adiabatic Microprocessor is improved by a factor of 2.9~3.1 compared to that of the conventional CMOS. The proposed design methodology of adiabatic circuits is applicable and feasible to low power system or other digital circuit. Designing blocks such as cache memory and multiplier is helpful improving the performance of Microprocessor

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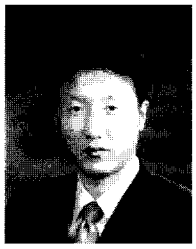

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