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MVL Data Converters Using Neuron MOS Down Literal Circuit

뉴런모스 다운리터럴 회로를 이용한 다치논리용 데이터 변환기

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Abstract

This paper describes the design techniques of the data converters for Multiple-Valued Logic(MVL). A 3.3V low power 4 digit CMOS analog to quaternary converter (AQC) and quaternary to analog converter (QAC) mainly designed with the neuron MOS down literal circuit block has been introduced. The neuron MOS down literal architecture allows the designed AQC and QAC to accept analog and 4 level voltage inputs, and enables the proposed circuits to have the multi-threshold properity. Low power consumption of the AQC and QAC are achieved by utilizing the proposed architecture.

Key -Word : MVL, AQC, QAC, DLC, Neuron MOS, Data Converter

요 약

본 논문에서는 다치논리(Multiple-Valued Logic : MVL)를 위한 데이터 변환기의 설계방법에 대해서 논의한다. 3.3 v의 단일 전원의 4 디지트의 CMOS 아날로그 4치 변환기(Analog to Quaternary Converter : AQC)와 4치 아날로그 변환기(Quaternary to Analog Converter)를 뉴런모스를 사용한 다운리터럴회로(Down-Literal Circuit : DLC)를 사용하여 설계하였다. 뉴런모스 다운리터럴회로는 제안된 AQC와 QAQ가 4개의 전압 레벨값을 출력과 입력으로 사용하게 하며, 소자의 다중 문턱전압 특성을 갖게한다. 제안된 AQC -QAC 회로는 구조면에서 전전력 소모의 특성을 갖는다.

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I. Introduction

Data converters play an important role in an ever-increasing digital world. As more products perform calculations in the digital of discrete time domain, more sophisticated data converters must translate the digital data to and from our inherent analog world. A/D converters translate from analog measurements, which are characteristic of

most phenomena in the real world, to digital language, used in information processing, computing, data transmission, and control systems. D/A converters are used in transforming transmitted of stored data, of the results of digital processing, back to real world variables for control, information display, or further analog processing. [1-3] In this paper, concentrating on the recent trend that many mixed signal integrated circuits have been implemented on a single chip, including data conversion circuit such as analog to digital converter and digital to analog converter, a analog to quaternary, quaternary to analog converter circuit has been proposed.

Multiple-valued logic(MVL) circuits have been developed for decades and the data converters for MVL circuits are remarkable for their advantages that are expected to reduce the limitation of wire connections and power dissipation density, which are the main design constrains of future ULSI system.

A functional MOS device has been proposed by Shibata and Ohmi in 1992[4], which is a switch with multi-valued voltage inputs. The device is composed of a floating-gate and multiple input gates that capacitively interact with the floating-gate. And neuron MOS down literal circuit(DLC) which has multiple threshold voltages with two bias voltages and DLC comparator which consists of one DLC inverter and DLC have been proposed[5-7] and it works in the high speed as the input control element for current switches. To implement the MVL circuits, the data conversion circuits using the DLC will be expected to be used as the analog input output devices.

The purpose of this paper is to present the circuit design of AQC and QAC and its simulation results. This paper also describes the previously proposed works for the quaternary converters and the A/D technique for MVL circuits including neuron MOS and Resonant Tunneling Diode(RTD).

II. Data conversion circuits

2.1 Quaternary based circuits[8-9]

Over the past 30 years, a substantial amount of paper has been published on data conversion circuits for MVL. Especially, the quaternary signal converter, which has the convenience of converting from or to binary signal, had been proposed in many works by K. W. Current. He concentrated on the advantages of using quaternary logic over binary logic which are its significantly grater functional density.

In analog to quaternary converter, the voltage output equation has been defined as Eq. (1) and the quantization error as Eq. (2).

$$Q_{out} = \frac{V_I}{V_{FS}} = q_1 \cdot 4^{-1} + q_2 \cdot 4^{-2} + \cdots q_n \cdot 4^{-n} \quad (1)$$

$$0 \le |\triangle V_I| \le V_{FS} \cdot 4^{-(n+\frac{1}{2})} \quad (2)$$

where V_I and V_{FS} are the input voltage and full-scale voltages and qi are the quaternary value and n is the number of digits, respectively.

In quaternary to analog converter, the analog current output in case of using weighted current source has been defined as Eq. (3).

$$I_{out} = (A_n \cdot 4^n + \cdots + A_2 \cdot 4^2 + A_1 \cdot 4^1 + A_0 \cdot 4^0) I_{ref} \quad (3)$$

where A_i are the quaternary logic current output from the quaternary threshold logic gates.

Quaternary encoder-decoder had been designed using voltage divider and logic gates and pass transistors with standard CMOS technology.

2.2 Data converter using neuron MOS[10-13]

With the standard double-polysilicon CMOS process, a highly-functional device called neuron MOS transistor has been proposed. In [17-18], the comparison of the number of transistors necessary for designing an ADC shows the dramatic reduction. In the case of flash ADC design, 16 transistors were needed for 3-b ADC as compared to 174 transistors by conventional CMOS design. It had been shown that the reduction of circuit complexity in the low-bit A/D converters using the weighted capacitance gate input of neuron MOS were available. The ADC with low DC power dissipation had been proposed in [19]. The dynamic latch in the comparator and the reference voltage generated by the capacitive voltage divider configuration combined with the ADC and the low power ADC had been introduced. To increase the accuracy of the neuron MOS structure, calibration techniques had been proposed in [20]. With the scheme, calibrated 6-bit ADC using neuron MOS had been presented.

2.3 Data converter using RTD[14-15]

A/D converters using RTDs show the reduced complexity of the circuit and the high speed in sampling rate. Some very fast and simple ADC circuits had been proposed by the unique folding characteristics of the vertically integrated RTD [14]. And multiple-valued quantizer using RTDs had been applied for 4-bit flash ADC, which operates in the speed of several GHz [15].

III. The AQC using DLC comparator

The DLC comparator had been proposed by [7]. The first stage of the comparator is the analog inverter and the second stage is the DLC. In such structure, the threshold voltage of the DLC is determined by Eq. (4)

$$V_{TH,DLC2} = V_{dd} - \frac{(V_{dd} - V_y) + (V_{dd} - V_y)}{2} = V_y \quad (4)$$

To show the transient output of the DLC comparator, the clock signal is adopted. The circuit diagram of basic clocked DLC comparator is shown in Fig. 1. When the clock signal is high, the output of the DLC comparator is pass through to the output buffer.

The layout of the DLC comparator has been shown in Fig.2. The double poly in the 0.35um process enables the gate capacitance and the floating capacitance. Fig.2 shows the simple structure of the DLC comparator and the capacitance of each capacitor is 0.2[pF].

The total block diagram of proposed AQC is shown in Fig. 3. AQC has four main blocks, reference voltage block, DLC comparator block, thermometer code encoding block and quaternary signal encoding block.

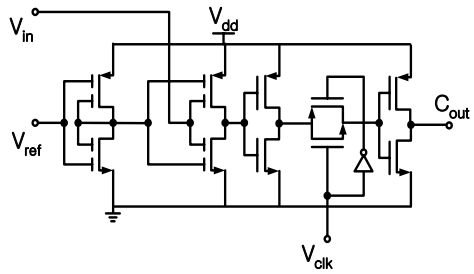

그림 1. 클록신호를 인가한 DLC 비교기

Fig. 1. Circuit diagram of clocked DLC comparator

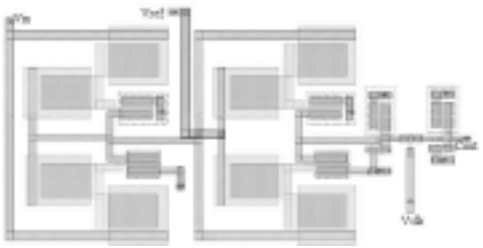

그림 2. DLC 비교기의 레이아웃
Fig. 2. The layout of the DLC comparator

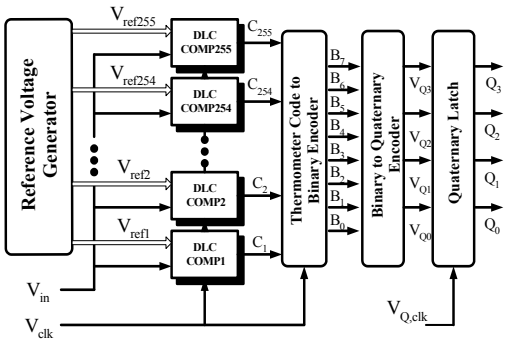

그림 3. AQC의 전체 블록도
Fig. 3. The total block diagram of AQC

Reference voltage block generates 255 different reference voltage signals and the size of registers is determined by the number of the sheet resistance. The resistance and sheet resistance are achieved by Eq. (5)

$$R = \rho L / A = \rho L / X_j W \ [\Omega]$$
$$R_S = \rho / X_j \ [\Omega/square] \quad (5)$$

where, ρ, X_j, L and W are resistivity, depth of cross connection, conductor length and conductor width, respectively.

The size of the 255 different resistors is too large to be designed in one device. And it is hard to get the exact value of the resistance. To overcome this problem, the 64 external bias voltages are used and the signals are divided by four same internal resistors.

In the Hynix 0.35um process, the poly resistor has the sheet resistance of 90 ± 15 $[\Omega/square]$. We use the 900Ω poly resistor as a unit resistor in the resistor string.

The reference voltage is divided into 2^N values by the reference voltage block, each of which is fed into the DLC comparator. The input voltage is compared with each reference value and results in a thermometer code at the output of the comparator. A thermometer code exhibits all zeros for each resistor level, if the voltage level of V_{in} is less than that of the resistor string, and ones if the voltage level of V_{in} is greater than that of the resistor string.

The thermometer code to binary code encoding block consists of Ex-OR gates. A simple 2^N-1 : N digital thermometer decoder circuit converts the compared data into an N-bit digital word.

The quaternary signal encoding block encodes the 4-digit quaternary signals from 8-bit binary signals. B_0 and B_1 are fed into the BQE 0 which generates the Q_0 signal. B_2 and B_3, B_4 and B_5, B_6 and B_7 are fed into the BQE 1, BQE 2 and BQE3, respectively. The circuit diagram of proposed BQE block has been shown in Fig. 4.

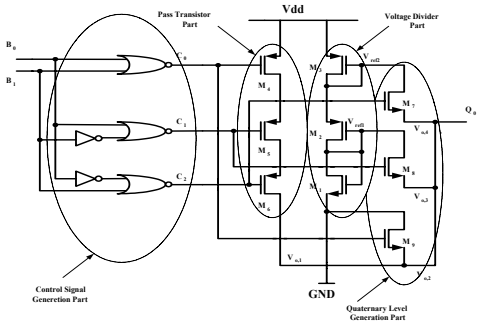

그림 4. 제안된 BQE 회로의 블록도
Fig. 4. The block diagram of proposed BQE

The layout of the total AQC block has been shown in Fig. 5. The 255 DLC comparator block occupied the 60% of the total size in the 3.8m by 3.4m core size. Reducing the size of the DLC comparator and the number of the capacitors has been remained for the further study.

IV. Quaternary to analog converter

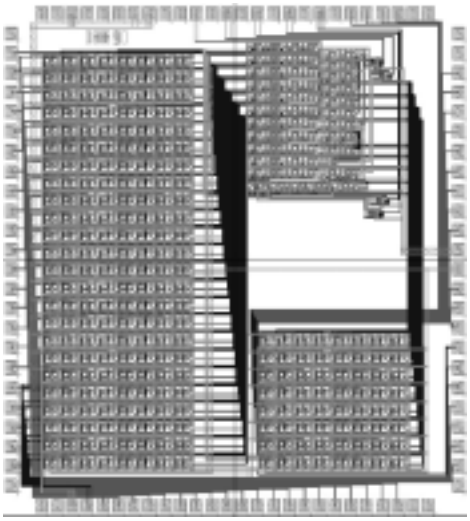

그림 5. 제안된 AQC의 전체 레이아웃
Fig. 5. The total layout of AQC

As we previously proposed[16], the proposed QAC has four input digits and one output voltage signal. Four input digits are the quaternary values and output voltage represents analog signal. The sampling rate of the LSB(Q0) is 120ns. It represents the four-valued signal from 0 to 3. The QAC has the same resolution of the 8 bit DAC but only 4 digits are needed in the QAC circuit. The output total current is determined by Eq. (5) and it has the base-4 digit summation property.

$$I_{out} = \sum_{i=0}^{3} 4^{i} \cdot V_{input} \cdot I_{ref} \qquad (5)$$

where, i is the input digit and

$$V_{input} = \begin{cases} 0 & \text{if } 0 \le V_{input} < 0.5 \\ 1 & \text{if } 0.5 \le V_{input} < 1.5 \\ 2 & \text{if } 1.5 \le V_{input} < 2.5 \\ 3 & \text{if } 2.5 \le V_{input} \end{cases}$$

QAC has the three basic blocks, the down literal circuit block, the quaternary weighted current type switch block, and the current source and output load block. The functional block diagram is shown in Fig. 6. QAC has four input digits and one output voltage signal. The quaternary input is ranged from 0000 to 3333.

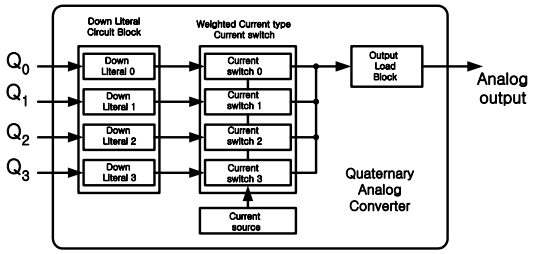

그림 6. QAC 회로의 기능 블록도
Fig. 6. The functional block diagram of QAC

Because of the output stability, the structure of multiple common gate mirror is adopted and as many as common gate mirrors are needed to generate the summed output current I_{out}.

It is needed to fit the current driving capacity of the differential switch MOS. The channel size of differential switch MOS in B0, B1, B2 and B3 is multiplied by 4, 16 and 64, respectively.

Table 1 represents the input condition of each digit and the output loaded output signal of QAC. There are four blocks for each digit and they are composed with a down literal block and a current switch block. And each down literal block has four different reference voltages and three down literal circuit blocks.

The layout of DLC which is the main element of the QAC is shown in Fig. 7. The gate capacitances are implemented by double poly and the floating gate has been implemented by the gate oxide between the two gate inputs and the gate poly. And the layout of the total QAC block has been shown in Fig. 8.

표 1. QAC의 4치 입력에 대한 출력신호
Table 1. The output signal of QAC with input condition

V_{in}	Down0	Down1	Down2	I_{out}
0	Low	Low	Low	0
1	High	Low	Low	$\sum_{i=0}^{3} 4^{i} V_{input} I_{ref}$
2	High	High	Low	
3	High	High	High	

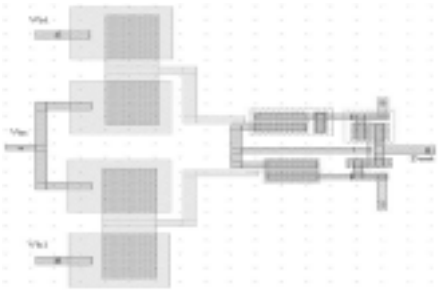

그림 7. DLC의 레이아웃
Fig. 7. The layout of DLC

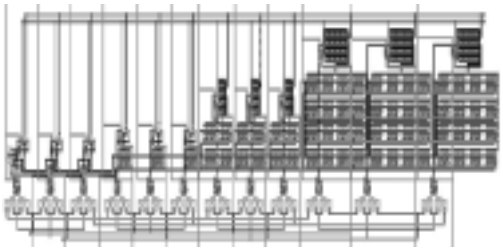

그림 8. 제안된 QAC의 전체 레이아웃
Fig. 8. The total layout of QAC

V. Simulation results

5.1 Simulation results of AQC

The simulated circuit performances of the 4 digit AQC are summarized in Table 2. Logical levels of the quaternary output voltage are induced as 0, 1, 2, 3V and the differences between two adjacent reference voltages are assigned as 10mV.

Fig. 9 shows the simulation results of the proposed AQC, and 4-digit 256 levels are shown as 3MS/s sampling rate at Q_0, with 22.49mW power consumption.

It is known that the area and power requirements of the 2^N-1 comparators are the disadvantages of the flash ADC. And the doubling of area with each bit of increased resolution is caused by the number of increased comparators. In AQC case, the number of transistors of the clocked DLC comparator is smaller than the conventional one and so does the power consumption. The simulation results of one clocked DLC comparator shows the 50 % reduced number of MOS transistors and reduced power consumption(0.1 mW). As results, the limitation of resolution over 8-bit in flash ADC could be overcome by the proposed AQC architecture.

표 2. 제안된 AQC 회로의 동작 특성
Table 2. Circuit performances of the AQC

Technology	CMOS n-well 0.35 um
Resolution	4 digit 256 level
Rise/Fall Time	0.1 ns
Settling Time	20 ns
Sampling Rate	> 3 MSample/s
Power Supply	3.3 V
Power Consumption	22.49 mW

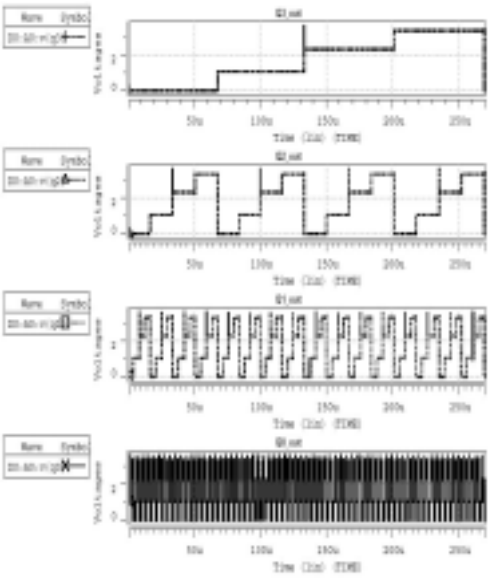

그림 9. 제안된 AQC 회로의 출력 특성
Fig. 9. The simulation results of the AQC

5.2 Simulation results of QAC

The simulated circuit performances of the 4 digit QAC are summarized in Table 3. And the total output plot of the AQC has been shown in Fig. 10.

The input signals of the QAC are 4-digit quaternary signals and the output signal shows the analog voltage output signal with 256 levels.

The result shows the fast conversion rate at Q_0 as 6.25MHz and low power consumption as 3.129mW.

The load resister is 1 [k] in this simulation and the rising and falling time is 10ns and the settling time is 30ns. Logical levels of the quaternary input voltage are assigned as 0, 1, 2, 3V and the reference current of current source block is 1uA. The reference voltages of the down literal circuit block are assigned as 0V, 1/3Vdd = 1V, 2/3Vdd = 2V, Vdd = 3V, respectively.

The maximum glitch energy is approximately equal to 0.4mV·s during the transition between 0333 and 1000. To reduce the glitch energy of the output signal, we use a capacitor at the output node. And it is parallel to the output load resistor.

표 3. 제안된 QAC 회로의 동작 특성
Table 3. Circuit performances of the QAC

Technology	CMOS n-well 0.35μm
Resolution	4-digit 256 level
Rise/Fall Time	10nsec
INL	< ±1.0 LSD
DNL	< ±1.0 LSD
Settling Time	30nsec
Output Swing	0.26V
Conversion Time	6.25MHz (LSD)
Glitch Energy	0.4mV·s
Power Supply	3.3V
Power Consumption	3.129 mW

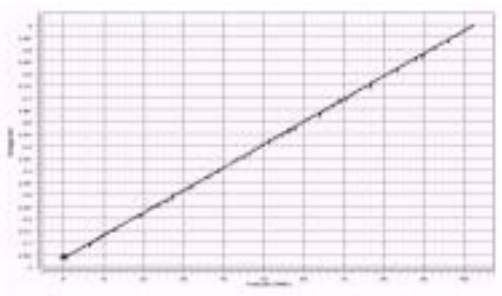

그림 10. 제안된 QAC 회로의 출력 특성
Fig. 10. The simulation results of the QAC

Terms	Type	Sampling Rate (MS/s)	Resolution	Power Consumption (mW)	Power Supply (V)	DNL/INL	Ref.
Neuron MOS	ADC	20	8bit	68	5	-	[19]
	DAC	200	8bit	1	5	0.5/2.0	[20]
RTD	ADC	5 (GS/s)	4bit	300	3	-	[25]
MVL	AQC	200 (kHz)	4digit	400	5	-	[8]
	QAC	-	3digit	-	-	-	[9]
This Paper	AQC	3	4digit	22.49	3.3	0.5/0.3	-
	QAC	6.25 (MHz)	4digit	3.129	3.3	1.0/1.0	

VI. Comparisons and Conclusions

6.1 Comparisons

In Comparison, we compared the proposed circuit with three types of data converters. Table 4 shows the comparisons in terms of resolution, sampling rate, power consumption, power supply and errors.

Firstly, the AQC and QAC of K. W. Current are focused on the realization of data converter for MVL.

Secondly, the data converters with neuron MOS show the drastic reduction of the number of transistors. But the exact size of input gate capacitors is hardly achieved.

Lastly, the data converter with RTD shows the sampling rate as several GHz but it is hard to design the RTD with standard CMOS process.

In this paper, AQC and QAC show low power consumption with 3.3V power supply and quaternary digits have the double information processing ability compared with binary bits.

표 4. 데이터 변환기의 성능 비교
Table 4. Performance comparison of converters

6.2 Conclusions

In conclusions, a 3.3V-3MS/s low power 4 digit CMOS AQC is designed by the flash ADC architecture with clocked DLC comparator and a 3.3V-6.25MHz low power 4 digit CMOS QAC is designed with the quaternary-weighted current mirror switches and neuron MOS down literal circuits with a single power supply of 3.3V for a double poly four metal standard CMOS 0.35um n-well technology. It is expected that the reduced die area and complexity of the circuitry and power dissipation could be acquired by using the quaternary logic in data conversion.

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