직렬형 멀티레벨 인버터를 사용한 대용량 무효전력 보상장치의 파라메타 설계

論 文
52P-4-6

Design of Parameters for High Power Static Var Compensator Used Cascade Multilevel Inverter

閔 完 基*·崔 載 昊**
(Wan-Ki Min·Jae-Ho Choi)

Abstract - This paper examines the application of high voltage static var compensator(SVC) with cascade multilevel inverter which employs H-bridge inverter(HBI). This method has the primary advantage that the number of voltage levels can be increased for a given number of semiconductor devices when compared to the conventional control methods. The SVC system is modeled using the d-q transform which calculates the instantaneous reactive power. This model is used to design a controller and analyze the SVC system. From the mathematical model of the system, the design procedures of the circuit parameters L and C are presented in this thesis. To meet the specific total harmonic distortion(THD) and ripple factor of the capacitor voltage, the circuit parameters L and C are designed. Simulated and experimental results are also presented and discussed to validate the proposed schemes.

Key Words : SVC, Cascade Multilevel Inverter, THD, Parameter Design, High Power Application

1. INTRODUCTION

In the large power system network, the active control of reactive power is indispensable to stabilize the power systems and to maintain the supply voltage. A static var compensator(SVC) using the voltage source inverters (VSIs) have been widely accepted as the next generation of the reactive power controllers of power system. Several SVCs based on GTOs and a special zig-zag transformer have been developed and put into operation in recent years[1-2]. It has been recognized that these SVCs have advantages over the conventional SVCs of generating less harmonic current to the system and requiring a much smaller reactor. However, zig-zag transformers used in these SVCs are bulky, expensive and unreliable. SVCs based on multilevel voltage source inverter have been widely studied due to its capability of eliminating the zig-zag transformer. In this multilevel VSI based SVC category, there are mainly three different system configurations. They are 1) diode-clamped converter configuration[3-4], 2) flying-capacitor converter configuration[5] and 3) cascading converter configuration [6]. The first and second configurations require a very large number of clamping diodes or flying capacitors, respectively. But the third one has the advantages of using small number of diodes and capacitors. It is constructed by cascading several voltage source HBIs. Although the above merits, it suffers the disadvantages.[6]

In this paper to solve these problems above, the main objective was to improve the unbalanced DC voltages of the SVC based cascade type multilevel inverter[8,9]. and analyze the performance of the designed prototype. One of the major limitations of the multilevel inverters was the DC voltage unbalancing between each HBI cell. To solve this problem, the novel fundamental rotated switching scheme of fundamental frequency was newly developed. From the model of the system, the design procedures of the circuit parameters L and C are developed. The circuit parameters L and C are designed so as to meet the specific THD and ripple factor of the capacitor voltage(RF). In the simulation and experiment, the proposed SVC system is verified on the transient response such as unit step change, most severe var commend.

2. CONFIGURATION OF POWER CIRCUIT

The simplified block diagram of the SVC system presented in this paper is shown in Fig.1. This system consists of a 7-level inverter, a set of linked reactors and series connected DC capacitors, DSP control board and

* 正 會 員 : 朝鮮理工大學 電氣科 副敎授·工博
** 正 會 員 : 忠北大學校 電氣電子工學部 敎授·工博
接受日字 : 2003年 7月 30日
最終完了 : 2003年 9月 2日

the ac source mains. In this system, the three phase source voltages mean v_{sa}, v_{sb} and v_{sc}, and the three inverter

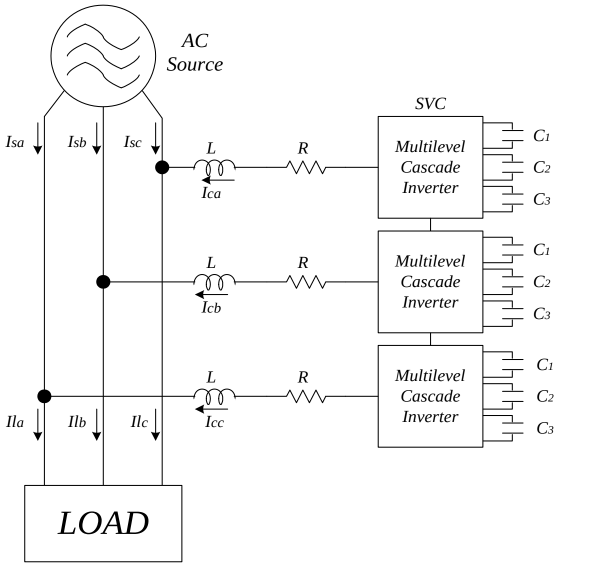

Fig.1 Structure of the SVC with cascade multilevel inverter.

output voltages of SVC, v_{ca}, v_{cb} and v_{cc}, respectively. Fig. 2(a) shows the three phase unit structure of HBIs constructed IGBT devices. It consists ofthe connection diagram for a wye connection 7-level inverter. Fig. 2(b) shows one module(cell) of the HBI with IGBT. Each HBI can generate three level outputs, $+V_{dc}$, 0 and $-V_{dc}$. The operating principles of the SVC system can be explained by considering the single fundamental equivalent circuit. An equivalent voltage source

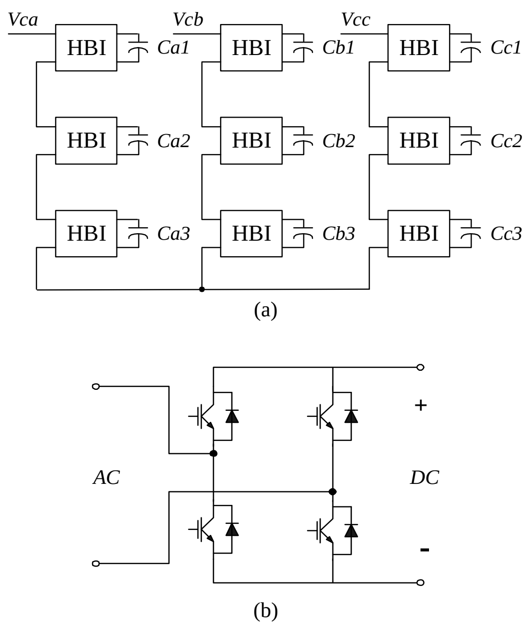

Fig. 2 Three phase cascade multilevel inverter.
(a) Main circuit of cascaded 7-level inverter,
(b) H-bridge inverter(HBI) with IGBT.

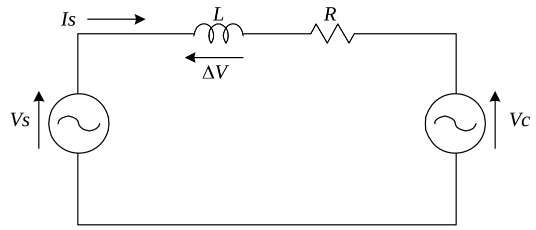

Fig. 3 Single phase equivalent circuit

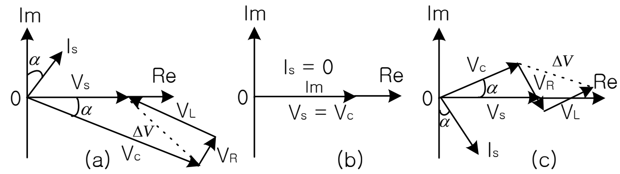

Fig. 4 Phasor diagram of the SVC.
(a) Leading current (b) Zero currnet (c) Lagging current

V_s is connected to the AC mains through a linked reactor, L and a resistor R representing the total losses in the transmission line, including inverter, as shown in Fig. 3. By controlling the phase angle, α of the inverter output voltage with respect to the phase of source voltage, the DC capacitor voltage V_{dc} can be changed. Thus, the amplitude of the inverter output voltage, V_c can be controlled. Fig. 4(a), (b) and (c) show the phasor diagram for leading(capacitive), zero and lagging (inductive) var generation, respectively.

When the inverter output voltage, V_c is higher than the ac system voltage V_s, leading reactive current is drawn from the system(var is generated). When the inverter output voltage V_c is equal to the ac system voltage V_s, reactive power exchange is zero. When the inverter output voltage V_c is lower than the ac system voltage V_s, lagging reactive current is drawn from the system (vars are absorbed). Accordingly, a large amount of reactive power drawn by the SVC can be controlled by adjusting the phase angle α by the small amount. Fig. 5 shows the synthesized phase voltage waveform of a 7-level cascaded inverter with three HBIs. For each phase of the compensators, the power circuit consists of a cascade multilevel voltage inverter of independent HBI modules.

3. SYSTEM ANALYSES

3.1 Steady state analysis

Therefore, the real power P and the reactive power Q drawn by the inverter system are expressed as[8-9]

$$P = V_{sq}I_q + V_{sd}I_d = \frac{V_s^2}{2R}\{1-\cos(2\alpha)\} \quad (1)$$

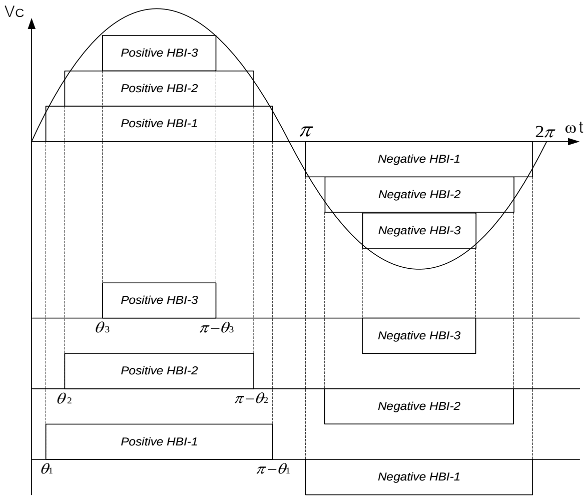

Fig. 5 Waveforms of the 7-level cascade inverter.

$$Q = V_{sq}I_d - V_{sd}I_q = \frac{V_s^2}{2R}\sin(2\alpha) \qquad (2)$$

Fig. 6 shows the magnitude of P and Q as a function of the specific circuit parameters given in Table 1. The real power P corresponds to the total losses in the inverter. Note that in the range of small α, i.e., |α| < 5°, the amount of reactive power is almost proportional to α. In addition, V_{dc}, is dependent on the M of switching pattern and the value of L, but independent of the value of C. Based on the DC analysis, the effective resistance R and the maximum phase difference α_{max} for the rated var can be obtained theoretically.

3.2 Design of inductance L

The inductance of the reactor L has a major effect on the THD_i of the line current and the maximum value of dc capacitor voltage. THD_i of the line current is one of the important specification. Therefore, the inductance L, is

Table 1 Circuit components for parameter design.

Meaning	Symbol	Value
Rated power	VA	1[MVA]
rms line to line voltage	V_s	3300[V]
Resistance	R	0.5[Ω]
Linked reactor	L	5[mH]
DC capacitor	C	2200[μF]
Fundamental frequency	f	60[Hz]
Modulation index	M	0.8

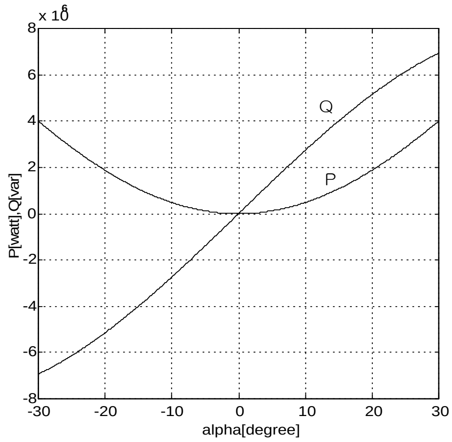

Fig. 6 Plot of Q and P drawn by the cascade inverter vs. α.

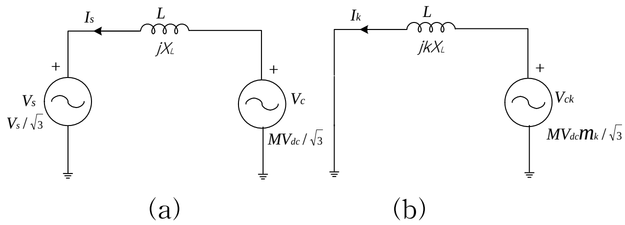

Fig. 7 Per phase equivalent circuit: (a) for fundamental (b) for k-th harmonic component.

to be designed so as to meet the requirement of the specific THD_i. To solve the THD_i, per phase equivalent circuit is considered under the assumption that R is negligible because it is much smaller than the impedance ωL and DC capacitor voltage V_{dc} is ripple free. The inverter phase voltage(v_{ca}) consists of the fundamental and its harmonic components.

$$v_{ca} = S_a^{12}(\omega t) M V_{dc} = \sqrt{2/3}\, M V_{dc} \sum_{k=1}^{\infty} m_k \sin(k\omega t + \phi_k) \qquad (3)$$

where S_a^{12} is the switching function in a phase and $m_1 = 1$, m_k is the amplitude of k-th harmonic component normalized by the fundamental component. Hence the per-phase equivalent circuit can be separately for fundamental and for k-th harmonics shown in Fig. 7. Therefore, for the rated capacitive var operation, rms value of output voltage of SVC V_c can be written in the following form:

$$V_c = M V_{dc} \qquad (4)$$

$$V_{ck} = M V_{dc} m_k \qquad (5)$$

The fundamental current component can be expressed by:

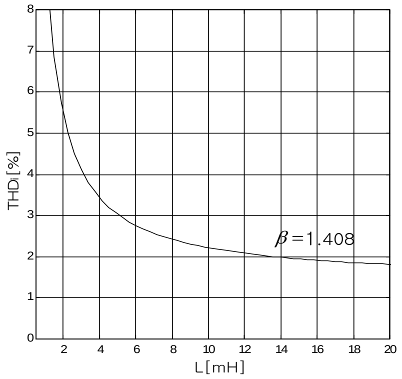

Fig. 8 THD_i curve of line current.

$$I_{s1} \cong \frac{|V_{c1} - V_{s1}|}{\omega L} \quad (6)$$

The k-th harmonic current is given by:

$$I_{sk} \cong \frac{V_{ck}}{k\omega L} \quad (7)$$

THD_i of the ac line current becomes:

$$\begin{aligned} THD_i &= \frac{\left[\sum_{k=2}^{\infty} I^2_{sk}\right]^{1/2}}{I_s} \\ &= \frac{MV_{dc}\left[\sum_{k=2}^{\infty}\left(\frac{m_k}{k}\right)^2\right]^{1/2}}{|MV_{dc} - V_s|} \\ &= \beta \frac{MV_{dc}/V_s}{MV_{dc}/V_s - 1} \end{aligned} \quad (8)$$

where

$$\beta = \left\{\sum_{k=2}^{\infty}\left[\frac{m_k}{k}\right]^2\right\}^{1/2}$$

From this equation, THD_i curve is shown in Fig. 8 and thus the inductance designed so as to meet the specific THD_i for a β determined by the switching pattern used in inverter.

3.3 Design of Capacitance C

The capacitance C determines the ripple factor(RF) of the DC capacitor voltage. The RF has an effect on the THD of the line current and thus it is to design in order to satisfy the specific RF. The RF of the capacitor voltage(RF_v) is completely determined by the input DC current i_{dc} for the rated capacitive var operation. Assuming that the three phase line currents are balanced and sinusoidal, i_d can be expressed by:

$$i_{dc} = \sum_{k=1}^{\infty} \sqrt{2} I_{dc,k} \cos(k\omega t + \Theta_k) \quad (9)$$

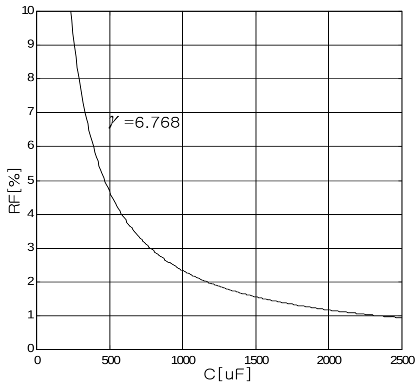

Fig. 9 RF_v curve vs. capacitance C.

I_{dck} is the rms value of the k-th harmonic component. By definition, the RF of the voltage V_{dc} is given by:

$$\begin{aligned} RF_v &= \frac{\sum_{k=1}^{\infty}\left[V_{dck}^2\right]^{1/2}}{V_{dc}} \\ &= \frac{\frac{1}{\sqrt{2}\omega C}\sum_{k=1}^{\infty}\left\{\left(\frac{I_{dck}}{k}\right)^2\right\}^{1/2}}{V_{dc}} \\ &= \frac{1}{\sqrt{2}\omega C V_{dc}}\sum_{k=1}^{\infty}\left[\left(\frac{I_{dck}}{k}\right)^2\right]^{1/2} \\ &= \frac{X_c}{\sqrt{2}V_{dc}}\gamma \end{aligned} \quad (10)$$

$$\text{where } \gamma = \left\{\sum_{k=1}^{\infty}\left[\frac{I_{dck}}{k}\right]^2\right\}^{1/2}$$

The factor γ is completely determined by the fundamental switching pattern of the inverter. Fig. 9 shows the RF_v values for the X_c.

4. CONTROL STRATEGIES

This means that each switching devices in HBI modules is turned on and off equally. So, the DC voltage of capacitor is balanced in each HBI module. From the transfer function[7], a controller can be designed in order that the SVC system has fast dynamic characteristics. The SVC system equation(11) is modeled using the d-q transform which calculates the instantaneous reactive power.

$$\frac{\triangle Q}{\triangle \alpha} = C(sI - A)^{-1} = \frac{I(s)}{H(s)} \quad (11)$$

where $I(s) = V_s^2\left[\frac{s^2}{L} + s\frac{R}{L^2} + \frac{M^2}{L^2 C}\right]$,

$$H(s) = s^3 + 2\frac{R}{L}s^2 + s\left(\omega^2 + \frac{R^2}{L^2} + \frac{M^2}{LC}\right) + \frac{M^2 R^2}{L^2 C}$$

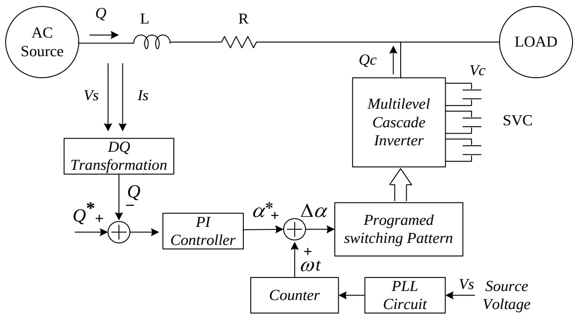

Fig. 10 Block diagram for SVC control.

This model is used to design a control strategy based on the control of the phase angle, α of the fundamental switching pattern also. Fig. 10 shows the control diagram of this system constructed by PI controller. Reactive power feedback using a PI controller makes it possible to improve the transient response of the reactive power. The calculated reactive power Q and reference reactive power Q^* are applied to the PI controller. The output of the PI controller is reference signal representing the phase angle α. The counter produces the phase information, ωt from a

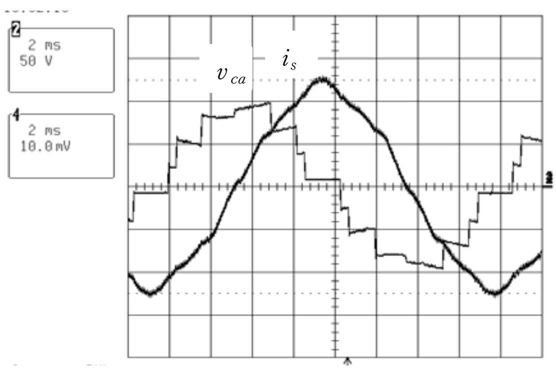

Fig. 11 Output voltage v_{ca} and current i_a of inductive var generation for Q^* = 0.8[kvar].

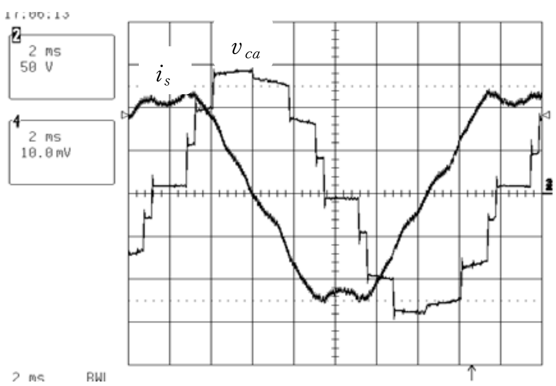

Fig. 12 Output voltage v_{ca} and current i_a of capacitive var generation for Q^* = −0.8[kvar].

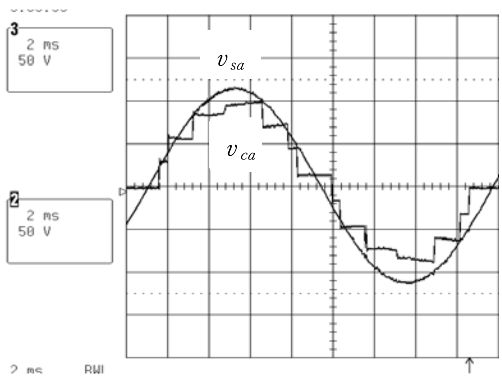

Fig. 13 Source voltage v_{sa} and output voltage v_{ca} of inductive var generation for Q^* = 0.8[kvar].

signal generated by a phase locked loop(PLL) circuit. The phase comparator compares α with ωt, and determines the times which the corresponding switching devices are turned on and off. Each time the a angle is changed the DC capacitor voltage keeping a new stable operation voltage. Because the DC voltage changes, the output voltage of cascade multilevel inverter does too, altering its amplitude. The amount of reactive power generatedor absorbed) is basically dependent on the difference of amplitude between the source voltage and output voltage of cascade multilevel inverter.

5. EXPERIMENTAL RESULTS

To confirm the validity of the proposed design methods and scheme, an experimental 5[kVA] prototype is implemented and tested also. This system consists of a 7-level inverter, a set of linked reactors and series connected DC capacitors, DSP control board(TMS320C31) and the ac source mains. This SVC system is constructed with the values given as follows: rms line to line voltage V_s=130[V], frequency f=60[Hz], other system parameters L=5[mH], R=0.2[Ω], C=2200[μF]. Fig. 11 shows output voltage v_{ca} and current i_a of inductive var generation for Q^* = 0.8[kvar]. Fig. 12 plots output voltage v_{ca} and current i_a of capacitive var generation for Q^* = −0.8[kvar]. Fig. 13 shows the ac source voltage v_{sa} and the inverter output voltage v_{ca} in inductive var generation for Q^*=0.8[kvar]. Fig. 14 shows the ac source voltage v_{sa} and the inverter output voltage v_{ca} in capacitive var generation for Q^*=−0.8[kvar]. Fig. 15 and Fig. 16 are plotted in the transient state result for inductive and capacitive var generation, respectively. In inductive var generation, Fig. 15 is plotted in the var commend Q^* and the separate DC capacitor voltages of

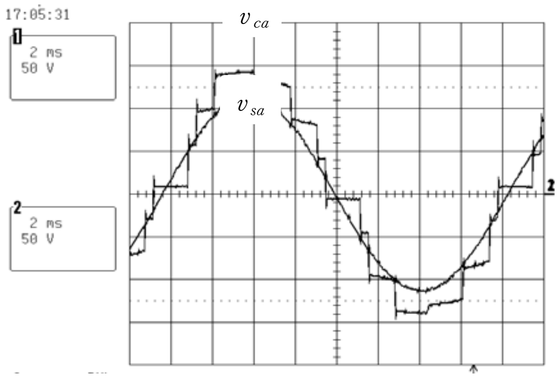

Fig. 14 Source voltage v_{sa} and output voltage v_{ca} of capacitive var generation for Q^* = −0.8[kvar].

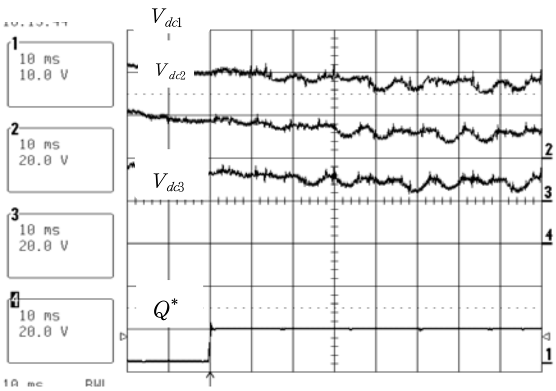

Fig. 15 HBIs DC voltages for step change of reactive var commend Q^*.(inductive var generation : from 0 to 0.8kvar)

each HBI module. In capacitive var generation, Fig. 16 is plotted in the var commend and the separate DC capacitor voltages of each HBI module. Fig. 17 is show in the harmonic spectrums of current in inductive var generation. A THD of current is 3.3[%]. In capacitive var generation in Fig. 18, THD is 4.3[%] and satisfied with the design value below 5[%].

6. CONCLUSION

This paper presents the high power application of SVC system using cascade multi-level inverter. From the mathematical model of the system, the design procedures of the circuit parameters L and C is presented. From the simulated and experimental results, the circuit parameters L and C is designed so as to meet the line current THD and ripple factor of the capacitor voltage. In the experiment, the SVC system is verified on the transient response such as unit step change, most severe var commend. This cascade multilevel inverter is also suited for transformer-less high power application such as FACTS(Flexible AC Transmission System).

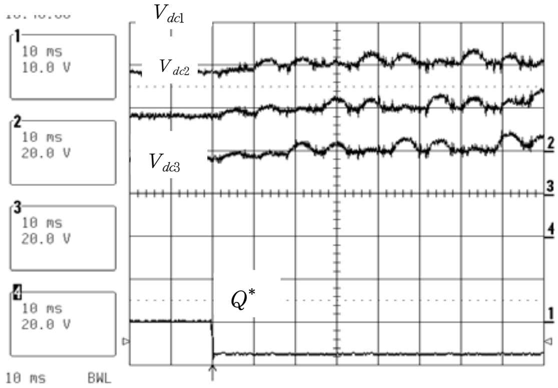

Fig. 16 HBIs DC voltages for step change of reactive var commend Q^*.(capacitive var generation : from 0 to −0.8kvar)

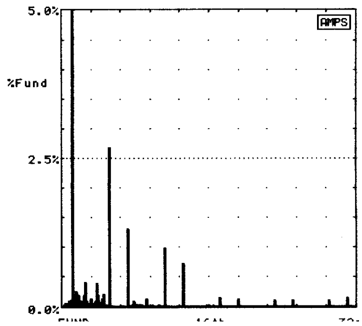

Fig. 17 Harmonic spectrums of current in inductive var generation.

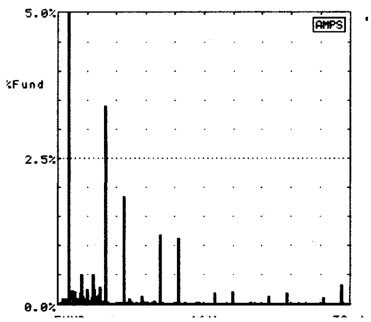

Fig. 18 Harmonic spectrums of current in capacitive var generation.

REFERENCES

[1] C. Schauder, et. al., "Development of a ±100 MVAR static con-denser for voltage control of transmission systems," *IEEE PES Summer Power Meeting*, Paper

No. 94, SM479 -6PWRD, 1994.

[2] Mori, et. al., "Development of large static var generator using selfcommutated inverters for improving power system stability", *IEEE PES Winter Power Meeting*, paper no. 92 WM165-1, 1992.

[3] L. H. Walker, et. al., "Force-commutated reactive power compensa-tor," *IEEE Trans. Ind. Appl.*, vol. IA-22, no. 6, pp. 1091-1104, Nov./Dec. 1986.

[4] Nam S. Choi, et. al., "Modeling and analysis of a static var compensator using multilevel voltage source inverter", *IEEE/IAS'94 Annual Meeting*, pp. 946-953, 1994.

[5] C. Hochgraf, et. al., "Comparison of multilevel inverters for static var compensation," in Conf. Rec. *IEEE/]AS Annual Meeting.*, 1994, pp. 921-928.

[6] F. Z. Peng, et. al., "A multilevel voltage source inverter with separate DC sources for static var generation," *IEEE Trans. on Industry Applications*, vol. 32, no. 5, September/October pp. 1130-1138, 1996.

[7] H. Akagi, et. al., "Analysis and design of a DC voltage-controlled static var compensator using quad-series voltage source inverters", *IEEE Trans. Ind. Appl.*, vol. 32, no. 4, pp. 970-977, 1996.

[8] Wan Ki Min, et. al., "Control of STATCOM using multilevel source inverter for high power application", *Prcc. IEEE PEDS*, Vol. 2, pp. 871-876, July 1999.

[9] Wan Ki Min, et. al., “Novel Switching Strategy of 1Mvar STATCON Using Cascade Multilevel Voltage Source Inverter for FACTS Application", *KIEE Trans.*, Vol. 48B, No.12 , pp. 691-700, 1999.

저 자 소 개

민 완 기 (閔 完 基)

1964년 2월 11일생. 1989년 충북대학교 전기공학과 졸업. 1993년 동 대학원 졸업(석사). 2000년 동 대학원 졸업(박사). 1988년~1991년 LG 종합연구원 및 LG 반도체 근무. 1994년~1997년 한전 전력연구원 연구원. 1997년~2003년 현재 조선이공대학 전기과 부교수, 2001년 1월~2001년 7월 일본 치토세과학기술대학 객원교수.

Tel : (062) 230-8357

E-mail : wkmin@mail.chosun-c.ac.kr

최 재 호 (崔 載 昊)

1955년 9월 27일생. 1979년 서울대학교 전기공학과 졸업. 1981년 동 대학원 졸업(석사). 1989년 동 대학원 졸업(박사). 1981년~1983년 중경공업전문대학 전자과 전임강사. 1893년~2003년 현재 충북대학교 공과대학 전기전자공학부 교수. 1993년~1994년, 1997년~1998년 University of Toronto (Visiting Professor)

Tel : (0431) 261-2425

E-mail : choi@power.chungbuk.ac.kr