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# A Novel Current-fed Energy Recovery Sustaining Driver for Plasma Display Panel (PDP)

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## ABSTRACT

A novel current-fed energy-recovery sustaining driver (CFERSD) for a PDP is proposed in this paper. Its main idea is to recover the energy stored in the PDP or to inject the input source energy to the PDP by using the current source built-up in the energy recovery inductor. This method provides zero-voltage-switching (ZVS) of all main power switches, the reduction of EMI, and more improved operational voltage margins with the aid of the discharge current compensation. In addition, since the current flowing through the energy recovery inductor can compensate the plasma discharge current flowing through the conducting power switches, the current stress through all main power switches can be considerably reduced. Furthermore, it features a low conduction loss and fast transient time. Operations, features and design considerations are presented and verified experimentally on a 1020×106mm sized PDP, 50kHz-switching frequency, and sustaining voltage 140V based prototype.

**Keywords :** Plasma display panel, energy recovery circuit, zero voltage switching

## 1. Introduction

The recent interest in flat panel display devices has made a PDP become a promising candidate for the conventional cathode ray tube (CRT) display, because a PDP is praised for its large screen size, wide viewing angle, thinness, long life time, and high contrast, etc. Therefore, it is promising that PDPs will soon become consumer preferable wall-hanging color TVs. Fig. 1 is simplified sectional view showing an example of a three-electrode-type surface-discharge AC PDP.

An AC PDP display is composed of X and Y electrodes covered by bus electrodes, a dielectric layer, and MgO layer in sequence on front glass substrate and address electrodes perpendicular to X and Y electrodes on the rear glass substrate. The MgO layer protects the dielectric layer from the plasma damage and aids the plasma in sustaining a discharge through secondary electron emission from its surface. The address electrodes are covered with three phosphors of red, green and blue (R. G. B.). The space between the two opposing substrates is filled typically with chemically stable rare gases such as Ne and Xe. An externally applied electric field between X and Y electrodes ionizes the gas to create the plasma. Then, the ultraviolet light from the plasma excites the phosphor to create red, green, and blue visible lights.

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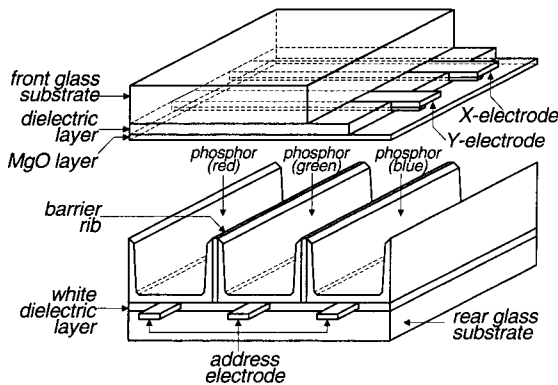
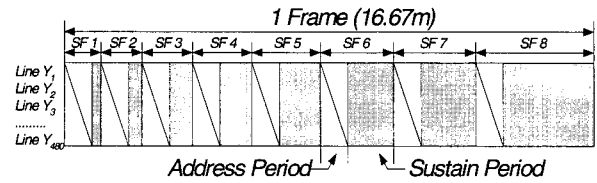


Fig. 1. Simplified structure of a three-electrode-type AC PDP.

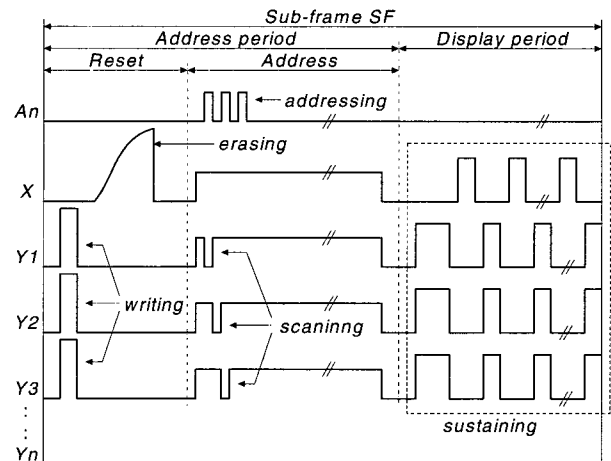
Recently, the address-display-separation (ADS) driving scheme is generally adopted to drive AC PDPs, as shown in Fig. 2 [1-2]. One frame is divided into eight sub-frames as shown in Fig. 2a. Each sub-frame has the isolated address period and display period, which are concurrent to all of display area. Fig. 2b shows the applied waveform to the PDP panel. The address period consists of a reset and address setup. The writing and erasing pulses are applied to X and Y electrodes to erase the wall charges accumulated during the previous sub-field period, which makes the same surface condition of all display cells. The writing pulses are applied between Y and address electrodes. This step is repeated from first to 480<sup>th</sup> scan line sequentially according to the display data to accumulate a wall charge on dielectric layers. Then, high voltage sustaining pulses are applied between X and Y electrodes in the display period. Therefore, the plasma discharges take place between X and Y electrodes. The high voltage pulses can be generated by using a simple full bridge driver and most of the input power is consumed during this period.

Meanwhile, since X and Y electrodes of a PDP are covered with dielectric and MgO layer, a PDP can be regarded as an equivalent inherent capacitor  $C_p$  as shown in Fig. 3. The typical value of an equivalent capacitor  $C_p$  is about 80nF for a 42-in PDP. Therefore, when applying a sustaining pulse to X and Y electrodes without an ERC, a considerable energy of  $2C_p V_s^2$  for each cycle is dissipated in the non-ideal resistance of circuits and PDP during charging or discharging interval [3-6]. Furthermore, the excessive surge charging and discharging currents will

give rise to EMI noises and increase the surge current ratings of power switches.



(a) Address display separation (ADS) scheme



(b) Applied waveform of ADS scheme

Fig. 2. Address display separation (ADS) driving scheme.

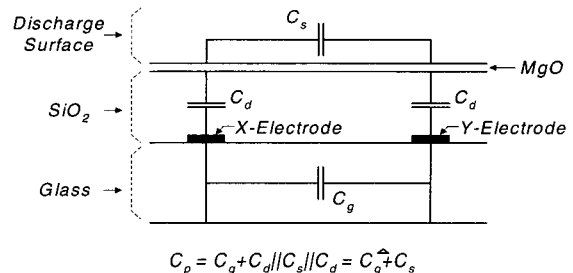


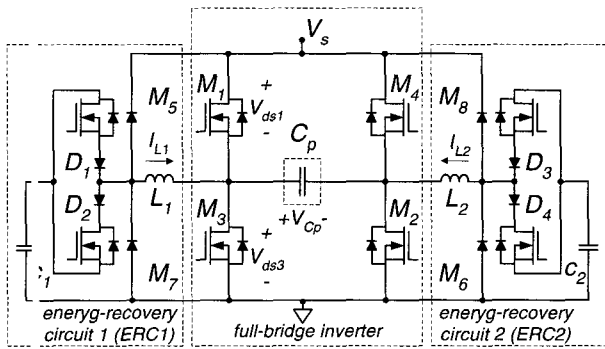
Fig. 3. Equivalent circuit for inherent capacitance of PDP cell.

To solve these problems, several energy recovery sustaining drivers (ERSD), as shown in Fig.4, have been proposed in recent years. Although these circuits can recover most of the lost energy, they still have several drawbacks. The circuit as shown in Fig. 4a features a high efficiency and good circuit flexibility. But, the most serious problem of this circuit is a large voltage drop across the parasitic resistance of the circuit during plasma discharge transients.

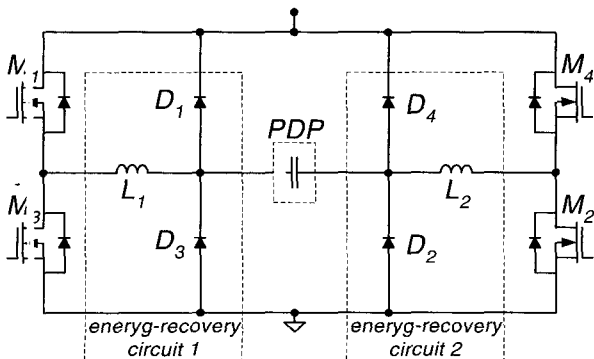
Therefore, the effective voltage applied to the PDP

decreases and so does the accumulated amount of the wall charge, which also makes the plasma discharge start voltage increased. Moreover, when the main switches are turned on, the voltage drops across the non-ideal resistance and diode causes the hard switching of the main switches, subsequent excessive surge current, serious power dissipation, EMI problem, and subsequent bad energy-recovery efficiency [3-6]. Another circuit as shown in Fig 4b is very simple and has no voltage drop as mentioned above. But its fatal problem is a very large circulating current that comes up to the value of the plasma discharge current (i.e. 150A for 42-in PDP). Therefore, its excessive conduction loss degrades the overall system efficiency and the considerable heat generated by this current would require a large cooling system [5].

To overcome these drawbacks, a novel CFERSD for a PDP as shown in Fig. 8 is proposed in this paper. It features no serious voltage drops caused by the large discharge current with the aid of the discharge current compensation.



(a) Prior circuit I



(b) Prior circuit II

Fig. 4. Schematic diagrams of prior ESRD.

Thus, its operational voltage margin is more improved. Furthermore, its circulating current is very small and the main power switches are all turned on with ZVS. Therefore, its overall system efficiency is very high, the EMI problem is very light, and the burden on the cooling system is very light. The prior circuit I shown in Fig. 4a is taken as an example to illustrate the basic operation of the prior ESRD.

## 2. Conventional Circuit

### 2.1 Mode analysis

Fig. 4(a) and Fig. 5 shows a prior ESRD and its driving waveform for a PDP, respectively [7-9]. One cycle period of a proposed circuit is divided into two half cycles,  $t_0 \sim t_4$  and  $t_4 \sim t_8$ .

Because the operation principles of two half cycles are same, only the first half cycle is explained. Considering only the left-side circuit, the intrinsic panel capacitance  $C_p$  and the energy recovery capacitor  $C_1$  ( $C_1 \gg C_p$ ) are series connected by an external inductor  $L_1$ . The driver utilizes the series resonance between  $C_p$  and  $L_1$  to charge or discharge the intrinsic panel capacitance  $C_p$ . The voltages across the capacitors  $C_1$  and  $C_2$  are assumed to be equal to  $V_s/2$  in the steady state.

Before  $t_0$ , only the switch  $M_3$  and  $M_2$  are in the on state and the others are in the off state. The voltage  $V_{Cp}$  is equal to zero.

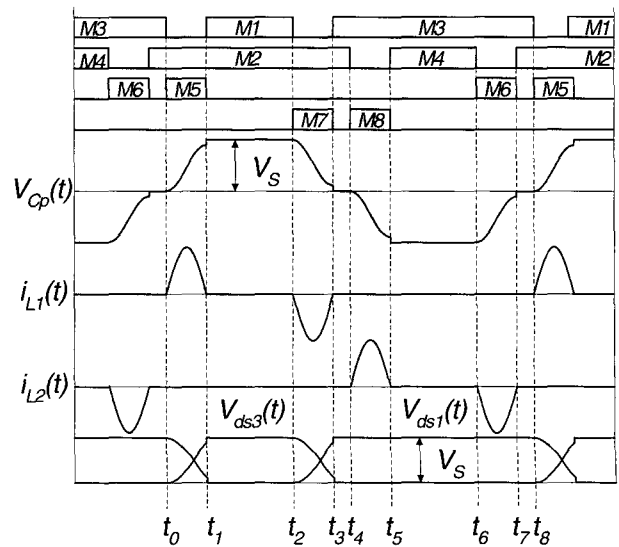


Fig. 5. Key waveforms of the prior circuit I.

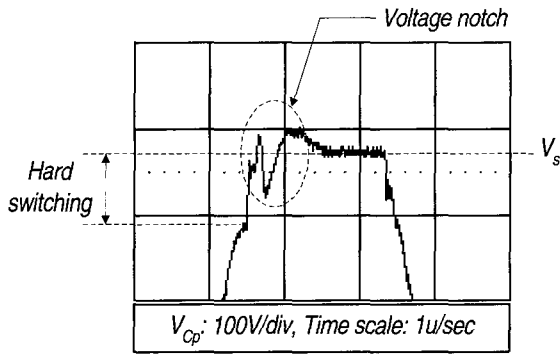


Fig. 6. Experimental waveform  $V_{Cp}$  of the conventional circuit.

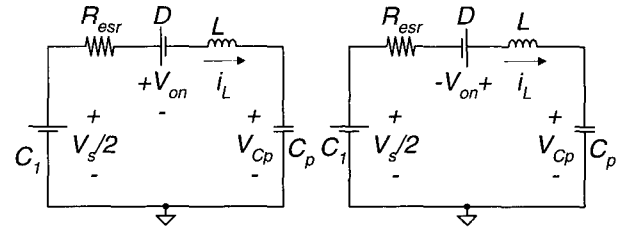
**Mode 1** ( $t_0 \sim t_1$ ): When the switch  $M_3$  is turned off and the switch  $M_5$  is turned on, this mode begins. The series resonance between  $C_p$  and  $L_1$  begins through  $M_5$ ,  $D_1$ , and  $M_2$ . Then, the panel voltage  $V_{Cp}$  will be charged to  $V_s$  at  $t_1$ .

**Mode 2** ( $t_1 \sim t_2$ ): After  $V_{Cp}$  is raised to  $V_s$ , the switch  $M_1$  is turned on and then the switch  $M_5$  is turned off at  $t_1$ . Namely, during this period,  $V_s$  is supplied from the power source to the panel through  $M_1$  and  $M_2$ . Therefore, the voltage across the panel capacitor  $C_p$  is maintained to  $V_s$  for this period.

**Mode 3** ( $t_2 \sim t_3$ ): When the switch  $M_1$  is turned off and then the switch  $M_7$  is turned on at  $t_2$ , this mode begins. The series resonance between  $C_p$  and  $L_1$  begins through  $D_2$  and switches  $M_7$  and  $M_2$ . Since the discharge current of the capacitor  $C_p$  begins to flow into the capacitor  $C_1$  through  $L_1$ ,  $D_2$ ,  $M_7$ , and  $M_2$ , the capacitor  $C_1$  is charged. The panel capacitor  $C_p$  discharges until the voltage  $V_{Cp}$  drops to zero voltage.

**Mode 4** ( $t_3 \sim t_4$ ): When the voltage  $V_{Cp}$  is reduced to zero, the switch  $M_3$  is turned on and then the switch  $M_7$  is turned off at  $t_3$ . That is, during this period, the ground potential is supplied to the panel through  $M_3$  and  $M_2$ . Therefore, the zero voltage applied to the panel capacitor  $C_p$  is sustained for this period.

As described above, the charge and discharge currents flow through the inductor  $L_1$ , the LC resonance operation appears, and thereby the energy recovery effect can be obtained.



(a) In charging  $C_p$  (b) In discharging  $C_p$   
Fig. 7. Equivalent circuit in charging and discharging.

In other words, the energy discharged from the capacitance  $C_p$  can also be temporarily stored in the capacitor  $C_1$  through  $M_7$  and  $D_2$ , and the energy discharged from the energy recovery capacitor  $C_1$  is used to charge the intrinsic panel capacitance  $C_p$  through  $M_5$  and  $D_1$ . Therefore, most energy is recovered and high efficiency is achieved.

However, although it can recover most of the lost energy, it still has several significant drawbacks. Detailed problems of the conventional circuit are described in the following section.

## 2.2 Problems of the conventional circuit

At mode 1, when the intrinsic panel capacitor is charged to exceed the firing voltage  $V_f$ , the gas in the plasma display panel would start to discharge. However, there is an interval (about 100~200 ns) between the instant  $V_{Cp}$  reaches the firing voltage  $V_f$  and the gas starts to discharge. Generally, the value of  $L_1$  or  $L_2$  is small enough, and the voltage  $V_{Cp}$  can be quickly charged to  $V_s$  before the gas starts to discharge. In such condition, although the series resonance finishes completely, the large discharge current going through the on resistance of the switches  $M_1$  and  $M_2$  or  $M_3$  and  $M_4$  would cause voltage notch across the panel as shown in Fig 6. These facts say that the increase of the voltage notch causes the amount of the wall charge to decrease and thus the discharging start voltage to increase.

Meanwhile, in charging or discharging  $C_p$ , the equivalent circuit is formed as shown in Fig. 7, where  $R_{esr}$  means the non-ideal resistance of circuits and  $V_{on}$  the forward voltage drop of the diode. From this figure, the panel voltage  $V_{Cp}(t)$  in charging transient can be obtained as follows:

$$V_{Cp}(t) = \left( \frac{V_s}{2} - V_{on} \right) \left\{ 1 - e^{-t/\tau} \left( \cos \omega t + \frac{\omega R_{esr}}{L} \sin \omega t \right) \right\} \quad (1)$$

where:  $\tau$  is time constant  $2L/R_{esr}$  and  $\omega$  is the resonant angular frequency  $\{1/LC_p - (0.5R_{esr}/L)^2\}^{0.5}$ .

After a half cycle resonance between  $L$  and  $C_p$ , the voltage across  $C_p$  becomes  $(V_s/2 - V_{on})(1 + e^{-\pi/\tau})$ . Then, to sustain  $C_p$  at  $V_{in}$ , the switch  $M_1$  is turned on. The voltage difference as high as  $V_s - (V_s/2 - V_{on})(1 + e^{-\pi/\tau})$  between  $C_p$  and input source causes the hard switching of  $M_1$  as shown in Fig. 5 and subsequent serious surge current. Similarly, the panel voltage  $V_{Cp}(t)$  in discharging transient can be obtained as follows:

$$V_{Cp}(t) = \left(\frac{V_s}{2} + V_{on}\right) + \left(\frac{V_s}{2} - V_{on}\right)e^{-t/\tau} \left(\cos \omega t + \frac{\omega R_{esr}}{L} \sin \omega t\right). \quad (2)$$

After a half cycle resonance between  $L$  and  $C_p$ , the voltage across  $C_p$  becomes  $(V_s/2 + V_{on}) - (V_s/2 - V_{on})e^{-\pi/\tau}$ . Then, to sustain  $C_p$  at  $0V$ , the switch  $M_3$  is turned on. The voltage difference as high as  $(V_s/2 - V_{on})(1 - e^{-\pi/\tau})$  between  $C_p$  and GND causes the hard switching of  $M_3$  and subsequent serious surge current.

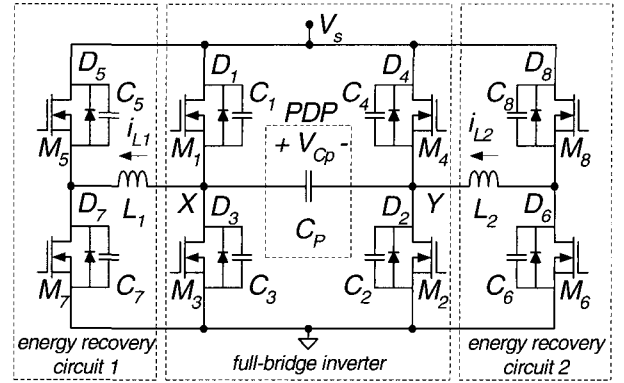
Above facts say that the increase of the parasitic resistance and forward voltage drop of the diode cause the excessive surge current, serious power dissipation, EMI problem, and subsequent bad energy-recovery efficiency. To solve these problems, it is necessary to reduce the parasitic resistance by designing the circuit board optimally as well as choosing switching devices with small on-resistance and low on-drop voltage to minimize the hard-switching stress and improve the energy recovery performance. However, since it is impossible to get rid of the parasitic components completely, abovementioned problems are inevitable. To overcome these drawbacks, a new CFERSD for a PDP is proposed in this paper.

### 3. Proposed Circuit

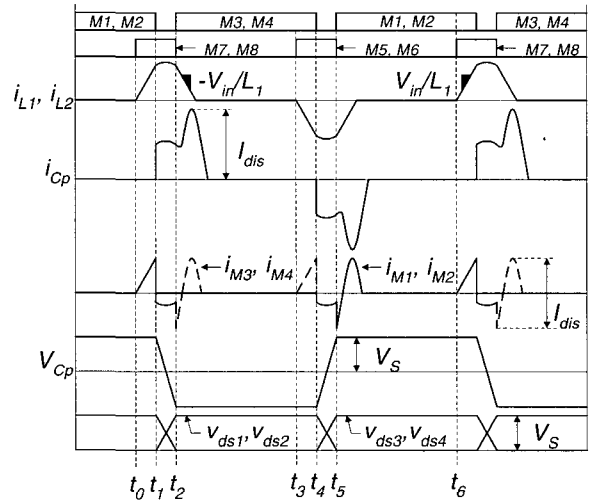
#### 3.1. Circuit operation

Fig. 8 shows the complete circuit diagram and key waveforms of the proposed circuit. One cycle period of a proposed circuit is divided into two half cycles,  $t_0 \sim t_3$  and  $t_3 \sim t_6$ .

Because the operation principles of two half cycles are symmetric, only the first half cycle is explained. Before  $t_0$ , the voltage  $v_{Cp}$  across  $C_p$  is maintained to  $V_s$  with  $M_1$  and  $M_2$  conducting.



(a) Schematic diagram of the proposed circuit



(b) Key waveforms

Fig. 8. A complete circuit diagram and its key waveforms.

**Mode 1 ( $t_0 \sim t_1$ ):** When  $M_7$  and  $M_8$  are turned on at  $t_0$ , mode 1 begins. The input voltage  $V_s$  is applied to  $L_1$  and  $L_2$  with  $M_1$ ,  $M_2$ ,  $M_7$  and  $M_8$  conducting. Thus,  $i_{L1}$  and  $i_{L2}$  increase linearly with the slope of  $V_s/L$  as  $i_{L1}(t) = i_{L2}(t) = V_s(t - t_0)/L$ , where it is assumed that the values of  $L_1$  and  $L_2$  are equal to  $L$ .

**Mode 2 ( $t_1 \sim t_2$ ):** When  $M_1$  and  $M_2$  are turned off at  $t_1$ , mode 2 begins. With the initial conditions of  $i_{L1}(t_1) = i_{L2}(t_1) = I_L = V_s(t_1 - t_0)/L$  and  $v_{Cp}(t_1) = V_s$ ,  $i_{L1}$  and  $i_{L2}$  start to charge the PDP,  $C_1$ , and  $C_2$  and discharge  $C_3$  and  $C_4$  as follows:

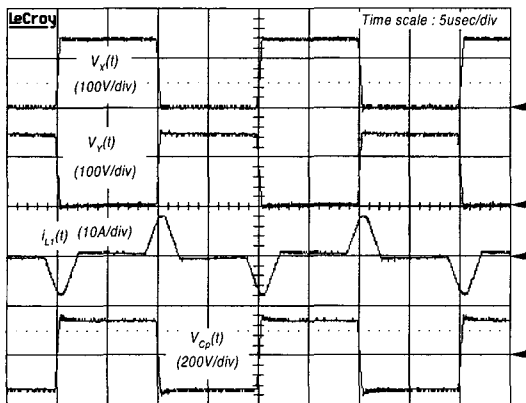
$$V_{Cp}(t) = V_s - \frac{I_L}{C_{oss} + C_p}(t - t_1) \quad (3)$$

$$V_X(t) = V_s - V_Y(t) = V_s - \frac{0.5I_L}{C_{oss} + C_p}(t - t_1) \quad (4)$$

where it is assumed that  $C_1$ ,  $C_2$ ,  $C_3$ , and  $C_4$  are equal to  $C_{oss}$  and  $L_1$  and  $L_2$  act as a current source with the value of  $I_L$ . With this arrangement, the abrupt charging and discharging operations of  $C_p$  are avoided and the voltage across  $C_p$  is decreased toward  $-V_s$ .

**Mode 3 ( $t_2 \sim t_3$ ):** When  $v_{Cp}$  is clamped at  $-V_s$ ,  $V_Y$  gets to  $V_s$ , and  $V_X$  drops to 0V at  $t_2$ , mode 3 begins. Since the voltages,  $V_{ds3}$  and  $V_{ds4}$ , across  $M_3$  and  $M_4$  are 0V,  $M_3$  and  $M_4$  can be turned on with ZVS. Moreover, since the inductor currents,  $i_{L1}$  and  $i_{L2}$ , compensate a large portion of the plasma discharge current  $I_{dis}$  during this period, the plasma discharge current through  $M_3$  and  $M_4$  are considerably reduced as shown in Fig. 8 b.

Therefore, the voltage drops across the parasitic resistances are not serious and the wall charges are well accumulated. After  $M_7$  and  $M_8$  are turned off, the inductor currents begin to decrease linearly with the slope of  $-V_s/L$  and the energy stored in the inductors is fed back to the input power source. The circuit operation of  $t_3 \sim t_6$  is similar to that of  $t_0 \sim t_3$ . Subsequently, the operation from  $t_0$  to  $t_6$  is repeated.



(a) Voltage across X, Y electrodes, and the PDP and inductor current through  $L_1$

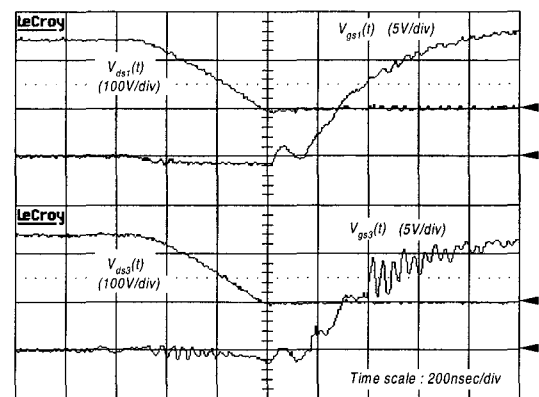
$$L_1 = L_2 = \frac{(t_2 - t_1)(t_1 - t_0)}{2(C_p + C_{oss})} \quad (5)$$

where  $L_1$  and  $L_2$  include the parasitic line inductance.

## 4. Experimental Results

The prototype CFERSD for a PDP is implemented with specifications of  $L_1 = L_2 = 24\mu\text{H}$ ,  $C_p = 13\text{nF}$  (1020×106mm sized PDP),  $M_1$ ,  $M_2$ ,  $M_3$ , and  $M_4 = 2\text{SK}2995$ , gate driver IC = IR2110, switching frequency = 50kHz, and  $V_s = 140\text{V}$ .

Fig. 9 shows the key experimental waveforms of the proposed circuit, when the white image is displayed. As can be seen in Fig. 9, the current source built-up in the inductor completely charges the panel capacitor  $C_p$  to  $V_s$  or  $-V_s$  with no serious voltage notch across the PDP. Since it compensates the large amount of plasma discharge current, the current through and the voltage drop across power switches are considerably reduced respectively, which will attract more wall charge to deposit on the dielectric layer of the electrodes. In other words, the wall



(b) Turn on transients of  $M_1$ ,  $M_3$

Fig. 9. Experimental waveforms of proposed circuit (In displaying the white image).

### 3.2 Design considerations

Since the brightness of a PDP is proportional to the operation frequency, the rising times,  $t_1 \sim t_2$  and  $t_4 \sim t_5$ , are required to be as short as possible. The interval  $t_1 \sim t_2$  (or  $t_4 \sim t_5$ ) is the desired rising time, and  $C_p$  and  $C_{oss}$  are as known values. Thus the values of  $L_1$  and  $L_2$  can be determined from equations (3) as follows:

voltage is larger, and it helps the panel maintain to light at lower voltage such as 140V compared with about 165V for prior circuit. Furthermore, the current through the inductor flows only when charging or discharging transients, and  $M_1$  and  $M_3$  are turned on after  $V_{ds1}$  and  $V_{ds3}$  drop to 0V as shown in Fig. 3b, that is, ZVS of  $M_1$  and  $M_3$  is achieved.  $M_2$  and  $M_4$  are also turned on with ZVS.

## 5. Conclusions

A novel CFERSD has been presented to overcome the drawbacks of prior circuits. Its circulating energy is very small and the main power switches are all turned on with ZVS. Therefore, it features a high efficiency and the burden on the cooling system is very light. In particular, since it compensates the plasma discharge current, it could solve the problem of the undesirable voltage drop. Thus, this enables the panel to light at lower voltage than the prior circuit. Therefore, this proposed circuit is expected to be well suited for hang-on-the-wall TVs with its thinness, lightness, high efficiency, and low price, etc.

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