Implementation of a MAC protocol in ATM-PON

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Abstract

MAC (Medium Access Control) protocol is necessary for a OLT (Optical Line Termination) to allocate bandwidth to ONUs (Optical Network Units) dynamically in ATM PON (Passive Optical Network) operated in a kind of optical subscriber network having tree topology. The OLT collect information about ONUs and provide all permission with each ONU effectively by means of MAC protocol.

Major functions of MAC protocol are composed of the algorism for distributing permission demanded by a ONU dynamically and allocation all permission used in APON properly. Sometimes MAC get to be a element of limiting the whole operation speed and occupy a most frequent operation part of the TC (Transmission Convergence) function module so it have to be designed to guarantee the best quality for each traffic. This paper introduce the way of implementation of a algorism which satisfy all of the upper conditions. This MAC algorism allocate bandwidth according to a number of working ONU and the information of the queue length dynamically and distribute permission for same interval to minimize delay variation of each ONU cell. MAC scheduler for the dynamic bandwidth allocation which is introduced in this paper has look-up table structure that makes programming possible. This structure is very suitable for implementation and operated in high speed because it require very simple and small chip size.

I. INTRODUCTION

Information super highway is composed of inter-office network and local loop network. Most of all the most important issue in building information super highway is how to cut cost of building local loop network that takes large part of cost of building information super highway. APON(ATM Passive Optical Network) offers inter-connection between subscribers within a radius of 20km in the form of FTTx(Fiber to the any) and the cost of building APON is low because maximum up to 64 subscriber. System using several fiber core divided from a fiber core by splitter can access to information super highway. APON system has very important mean as a next generation subscriber access system because it can support ultimate local network form FTTH(Fiber To Home) by means of integration FTTx in a platform.

MAC(Media Access Control) protocol mean a kind of protocol which control media access in order to allow communication between systems using media together. So it is essential to execute MAC in the communication of point-to-multipoint links if it is in wireless or wire local loop. Although MAC protocol also should be executed in APON just because ONU(Optical Network Unit) in APON use a fiber core together, the standardization is now under way [1]. Especially cell scheduling should be executed to improve performance of QOS(Quality of Service) which is given for each traffic in ATM network. But if too complicated algorism is executed, the dimension of chip have to be increased so that make impossible that something execute in the given time efficiently. So more simple and efficient algorism is more effective.

In this paper, the MAC schedule which makes possible that OLT(Optical Line Termination) provide various bandwidth for ONU in APOM

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base on G.983.1 is implemented. MAC protocol is divided GRP(Grant Request Protocol) and GDA(Grant Distribution Algorithm). And the interval of mini-slot which used to send the information about buffers in ONU can be programmed by the number of ONU from half frame at the minimum up to 4 frames at the maximum. In permission and allotment algorism(that is the algorism to distribute equitable bandwidth to each ONU by means of the information of the state of each ONU buffers). First of all OLT try to read CBR permission of the partition slot by the cycle of the half frame and then allocate bandwidth and VBR permission to ONU. The most number of the permission and allotment per one cycle of mini-slot can be programmed from 25 to 200 and the algorithm which calculate the sum of the number of the each active ONU and the queue length, is used to operate and allocate permission dynamically. The allocated istribution area of permission can be programmed from the half frame at the minimum to 4 frames at the maximum and so the permission and allotment adopt the algorism to minimize the variation by delay of cell and allocate same space [2].

The construct of this thesis will be followed. First of all the outline of operation and block diagram of MAC schedule will be introduced at the second section and at the third section the operating principle of APON and formation will be introduced in more detail. And next at the forth section we can confirm and explain the process of the operation as a whole through the trial experiment and FPGA (Field Programmable Gate Array). Finally at the fifth section we will come to conclusion and refer to the subject to be studied afterward.

II. THE OUTLINE OF THE PERMISSION AND DISTRIBUTION ALGORITHM FOR MAC

In APON system the downstream signal through one optical core connected to the OLT which is installed office is divided by splitter to 64 optical cores and transmitted to the ONU. On the contrary, the signal transmitted by several ONU is multiplexed by combiner and transmitted to the OLT through one optical core. The distance between OLT and ONU can be 20km at the maximum and OLT is deployed in the form of FTTCab(fiber to the cabinet), FTTB/C(Fiber To The Building/Curb) and FTT H according the location of the installed ONU and the capacity of handling the signal. Especially the ONU installed in home is named ONT(Optical Network Termination) [3]. The transmission speed in downstream is 155.52 or 622.04 Mbps and in upstream is 155.52 Mbps. In APON, optical transmission adopt WDM (Wavelength Division Multiplexing) as the way of modulation for bi-direction communication through one optical core and transmit signal of 1,310㎛ wavelength in upstream using burst mode but in downstream transmit signal of 1,550 ㎛ wavelength using continuous mode.

There are ranging and MAC protocol as a major technology for implementation APON. When several systems transmit cells to the upstream Ranging protocol adopt the transmission technology that virtually places same distance among several systems to prevent collision in a section of holding same medium. So to speak OLT is aware of new entries of ONUs and after measuring distance among them. It place all of the ONUs at the same location virtually by allocating equalized delay that means standby time before ONUs send cells. This theory already has comes up to standard in G.983.1.

The most important factor in request permission protocol is the structure and cycle of the mini-slot that send the information of ONU itself. So the structure of mini-slot is composed of 7 bytes like fig. 1 and just one upstream timeslot(the length of 56 byte) contain 8 mini-slot. The delimiter value of overhead is divided into 8 groups and each ONU is distinguished from itself by each group number and location of offset.

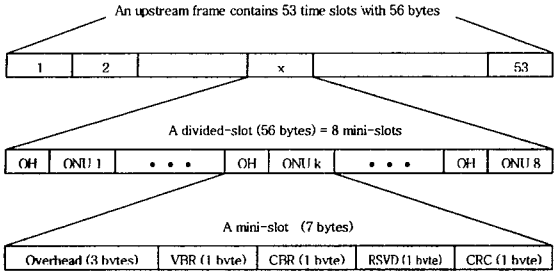


Fig. 1 Format of divided slot

Table 1 Payload content of downstream PLOAM cell.

1	IDENT	25	LCF11
2	MESSAGE_PON_ID	26	LCF12
3	MESSAGE_ID	27	LCF13
4	MESSAGE_FIELD1	28	LCF14
5	MESSAGE_FIELD2	29	LCF15
6	MESSAGE_FIELD3	30	LCF16
7	MESSAGE_FIELD4	31	LCF17
8	MESSAGE_FIELD5	32	RXCF1
9	MESSAGE_FIELD6	33	RXCF2
10	MESSAGE_FIELD7	34	RXCF3
11	MESSAGE_FIELD8	35	RXCF4
12	MESSAGE_FIELD9	36	RXCF5
13	MESSAGE_FIELD10	37	RXCF6
14	CRC	38	RXCF7
15	LCF1	39	RXCF8
16	LCF2	40	RXCF9
17	LCF3	41	RXCF10
18	LCF4	42	RXCF11
19	LCF5	43	RXCF12
20	LCF6	44	RXCF13
21	LCF7	45	RXCF14
22	LCF8	46	RXCF15
23	LCF9	47	RXCF16
24	LCF10	48	BIP

The cycle of mini-slit is changeable by the number of active ONUs from the length of the half frame to the minimum up to 4 frames to the maximum. And also OLT provides permission for such as mini-slot. The contents of mini-slot is the number of cells that is kept in buffer of ONU before transmission and if wrong number is transmitted, it has effect on performance of PON seriously. So CRC field is used to protect itll s contents.

When mini-slot has transmitted to OLT through the request permission protocol MAC schedule inside OLT try to read arrived mini-slot and distribute permission properly and then provide permission to ONUs by creating contents in permission field of downstream PLOAM cell like table 1. The downstream PLOAM cell has 27 permission fields and ONUs start to read permission number when if that number is same as that ONUs itself is the point of time that it transmits data cells to the upstream with exact synchronization.

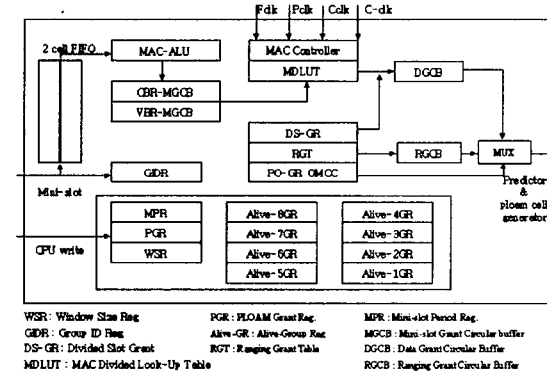


Fig. 2 Configuration of MAC processor

Mac processor have to provide a function of traffic shaping that is essential factor to distribute permission and product permission field. And for making permission field in downstream PLOAM cell per half frame it must satisfy the timing term desired completing the schedule per half frame. So we have to develop more effective algorithm for simple implementation and performing a essential function. Fig. 2 show us a whole formation of MAC processor. The input signal which is handled in MAC processor consist of data CPU asking a razing and another data arriving at mini-slot. Eventually

to provide PLOAM cell creator with the permission table gets to be output signal and this output is also offered to predictor.

MAC predictor has 3 CBs (circular Buffer) and 1 MAC distribution LUT (MAC Distribution Look-up Table, MDLT) and there are three kinds of CBs: first one is data grant CB (Data Grant Circular Buffer, DGCB), second one is ranging grant CB (Ranging Grant Circular Buffer, RGCB), and last one is MAC grant CB (Mini-slot grant circular buffer, MGBC)

The fig. 3 below show the operating point of time of the MAC scheduler, MAC scheduler start to distribute permission one cell before coming out next PLOAM clock and finish calculating all scheduler during about 1378 (53×26) byte clocks.

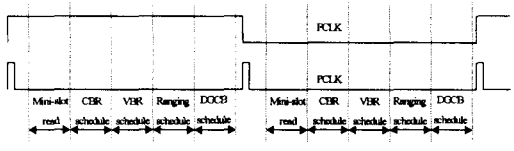


Fig. 3 Operation point of MAC scheduler

The fig. 4 show the total operating process of the MAC scheduler. As mentioned above mini-slot scheduler is operated per every half frame and window scheduler start to window scheduling when CPU enable flag bits(window Flag=on, that is MSB of WSR=1). In this case, the distributed Grant is composed of ranging, PLOAM and UA_GR(Unassigned Grant) and at that time W_PRO or W_end Grant instead of UA_GR is used in predictor.

The grant types offered in MAC layer are divided slot, PLOAM cell, OMCC cell(ONT Management and Control Channel) and data cell(CBR,VBR). In the priority order of distribution, the divided slot and PLOAM cell which are necessary for maintaining TC layer among which provide cyclic grant has the most high order. Subsequently Maintaining OMCC is essential for exchanging control information between OLT and ONU/OLT. Lastly UA_GR occupy the space left after finishing all scheduling user traffic. Consequently, Grant having high priority order propose scheduling algorithm ahead and the table 2 show the way of coding for Grant field of PLOAM cell [2].

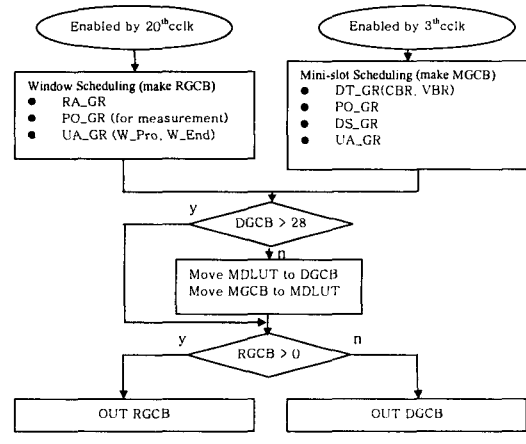


Fig. 4 Operational flowchart of MAC scheduler

Table 2 Coding scheme for the grant field of the PLOAM cell.

Type	Bit [7]	Bit [6]	Bit[5:0]	Grant	Reference
Control grant	1	1	111111	Idle	Fixed in G.983.1
			111110	Unassigned	
			111101	Ranging	
			111100-00 1000	Reserved	Future
			111011	W_Pro	Proposed
			111100	W_End	
		0	000000-00 0111	Divided slot	
Data grant	0	1	000000-11 1111	CBR cell	
		0	000000-11 1111	VBR cell	

A. THE GRANT OF PARTITION SLOT

The divided slot has to occupy the upstream channel for every half frame. So as fig. 5 shown, the grant field in each PLOAM cell has one DS_GR.

B. TNE GRANT OF PLOAM CELL

G.983.1 recommend that PLOAM grant

provide all ONU with a grant per every less than 100ms. It means that PLOAM provide one grant per about every 659.0 frames. We design that a grant will be offered per every 256 frames, which support the cycle of the PLOAM cell is about 39.08ms in this study. It means that when the maximum 64 ONU/OLT are operated, one PLOAM cell grant is offered per every 4 (256/64) frames. So as figure 4 shown, the grant of the PLOAM CELL use the 27 grant field of the first PLAOM cell in first downstream frame exclusively.

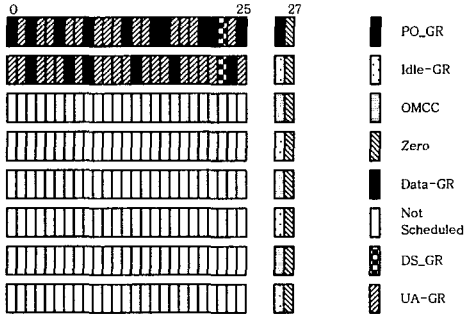


Fig. 5 Structure of grant table.

C. THE GRANT OF OMCC CELL

There is a definition about OMCC in ITU-T G.983.2. Each another VPI (Virtual Path Identifier) is assigned to each ONT as PLOAM cell. The MAC layer of OLT offers grant for upstream OMCC traffic of each OLT [4]. Even though there are several definition about several kinds of OMCC performance monitoring, the study for OMCC performance monitoring is going on. But the below thing is mentioned.

1. CLP=0 (CLP has to be 0 to be transmitted)
2. The consumed bandwidth for OMCC channel cannot go beyond (TBD)% of total PON bandwidth
3. OMCC cell has to be placed in high order of priority Q
4. The response time cannot be more than one second in case of message having high priority and three second in case of it having low priority.

So the bandwidth of OMCC cell has to be guaranteed even in case user traffic is congested and the 27th grant for the first PLOAM cell of the 2th, 3th,4th frame is used as grant for OMCC cell to guarantee the bandwidth of OMCC channel.

D. THE GRANT OF DATA

MAC scheduler receives the information of buffer status for each ONU and distributes permission by the impartial way of bandwidth allotment and CBR grant cannot has higher order than VBR grant distribution in data grant.

E. Non-allotment Grant

Mac scheduler try to distribute grant whenever allotment slot arrives, exactly for every half frame. At this time if there is no assigned grant, the grant distribution will happen by UA_GR

III. The implementation of the MAC scheduler

A. Mini-slot grant circular buffer (MGCB) scheduler

In MGCB scheduler, the grant is dynamically distributed by the number of active ONU and Q length information collected from ONUs. The fig. 5 show arithmetic operation unit. The divided slot arriving for every half frame is temporarily stored in cell buffer and the grant distribution is processed at regular point with half frame cycle and in MAC-ALU(MAC-Arithmetic Logic Unit) the distribution and operation happen after reading value of the CBR and VBR of the mini-slot. CBR grant has higher priority than VBR grant in distribution priority. First we explain the process of grant and distribution.

Table 3 Maximum number of the grant for variable MPR (Mini-slot Period Register)

MPR	1	2	3	4	5	6	7	8
Maximum number of the grant according to the cycle of mini-slot (Y)	25	50	75	100	125	150	175	200

First of all, letll s define that the length of CBRll and VBRll Q arriving from ill th ONU through mini-slot is Ci and Vi and the actual number of grant OLT offering is CBR_Gi and VBR_Gi. MGCB scheduler calculates the total sum (CBRt) of the CBR Q length of all mini-slot inter one partition slot and if this value is equal or smaller than (Y)the maximum number of the grant according to the cycle of mini-slot as figure 3 shown,

$$CBR\_Gi = Ci \quad (1)$$

The value is assigned as above. In opposition if CBRt is larger than Y the value is assigned as below,

$$CBR\_Gi = Ci * Y/CBRt \quad (2)$$

In this x is a maximum integer less than x. The VBR allotment carry out after finishing distribution of CBR permission and when the reserve of the assigned permission is leaved. The possible number of permission for VBR traffic is difference of total sum between Y and the assigned grant and the consequent number is always natural number.

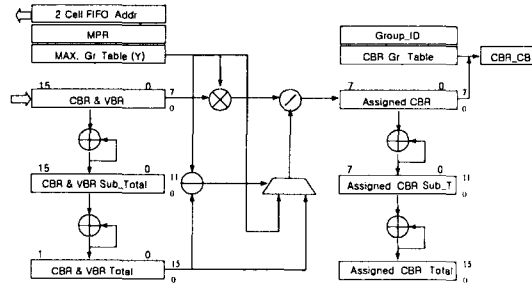
$$SUB\_Y = Y-\sum iCBR\_Gi \quad (Y \geq \sum i\ CBR\_Gi) \quad (3)$$

MGCN scheduler take a total sum(VBRt) of VBR grant of the partition slot and if this value. Is equal or smaller than SUB_Y it assign VBR grant to ONUi as much as Vi,

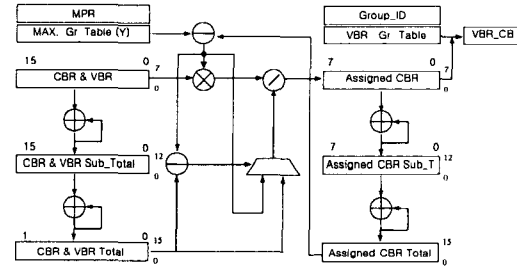
$$VBR\_Gi = Vi \quad (4)$$

In opposition when VBRt is larger than SUB_Y, the value is assigned as below,

$$VBR\_Gi = Vi \times SUB\_Y/VBRt \quad (5)$$



(a) CBR Arithmetic



(b) VBR Arithmetic
Fig. 5 MAC-ALU

The grant and distribution of data (CBR, VBR) takes the largest part of operation among TC function modules and the operator to be used take a large part of dimension of chip and also can be factor to limit operating speed. Even though a parallel multiplication and division operator produce multiplication and division item faster than a series multiplication and division operator do.

Increasing Chip dimension in proportion to square the number of bits is essential factor for paying for speed increase. So considering operating speed and chip dimension a series multiplication and division operator is suitable.

B. MAC Distribution Look Up Table(MDLUT) scheduler

In MGCB scheduler, the dynamically distributed grant is distributed at same interval. At this time, if too complicated algorism is used for minimizing cell delay variation, the dimension of chip is increased and also the situation that it cannot handle data process in given time can incur. So consequently more simple and effective algorism is asked. In MDLUT, broadband data service having various traffic quality in the whole bandwidth of transmission channel are statistically multiplexed and dynamic length formation (LUT) that is programmed for providing customer with enough transmission bandwidth and good service quality must be embodied.

Table 4 Writing address and Reading address for MPR

MPR	1000	00111	0110	0101	0100	0011	0010	0001	
Writing address									
Upper	Lower	Lower	Lower	Lower	Lower	Lower	Lower	Lower	Upper
00000	000	000	000	000	000	000	000	000	10101
00001	001	001	001	001	001	001	001		10010
00010	010	010	010	010	010	010			01111
01111	011	011	011	011	011				01100
10000	100	100	100	100					01001
10001	101	101	101						00110
00110	110	110							00011
00111	111								00000
01000									10111
10101									10100
10110									10001
10111									01110
01100									01011
01101									01000
01110									00101
00011									00010
00100									11000
00101								011	10110
10011						011	110	001	10000
10100					011	001	001	100	01101
01001				010	001	101	100	111	01010
01010			001	001	100	010	010	010	00111
01011		001	010	011	010	100	101	101	00100
11000	000	000	000	000	000	000	000	000	00001
Reading address									
	0001	0010	0011	0100	0101	0110	0111	1000	MPR

The size of MDLUT is dynamically 25 at the minimum to 200(4 frames) at the maximum and related to the interval of mini-slot the interval of mini-slot can be dynamically programmed by the number of activating ONU. The table 4 show how to refer the address when MDLUT read and write a grant. Every 25 bits address is red and written per interval of half frame and 1 byte consists of upper address and low address. The address which is written in MDLUT increase the low address of LUT in regular sequence after reading low address it refer MPR and the various upper address is increased by one time. At that time 1 byte is allocated for write address which is made by combination of upper address and low address. The address which read MDLUT increase upper address of LUT in regular sequence and When upper address reach 25, low address is increased by one time.

C. Ranging Grant Circular Buffer(RGCB) scheduler

As described in an whole operation outline, an window scheduling is operated by the request of cpu. For the moment the cpu writes window size for opening in WSR (window size register. It starts to write ranging grant or PLOAM grant in PGR (PLOAM Grant Register) according as the purpose of opening the window is for acquiring serial number or for measuring the equalizing delay. In RGB, an W_Pro grant is written as many as the number of WSR.

At this time, the grant which is memorized in PGA is written in the middle of window. And

W_End grant is written at the end of window. The table 2 show the grant code for this. When PLOAM clock occur, the generator and predictor of PLAOM read contents of RGCB and DGCB by 26 times, at this time the grant of RGCB is prior to the that of DGCB. For this reason the generator of PLOAM cell replace the value of grant of the W_End and W_Pro as UA_GR and write it in grant field of downstream PLOAM cell.

D. Data Grant Circular Buffer(DGCB) scheduler

A MAC processor provide the generator and predictor of PLOAM cell with 26 data grants per half frame. At this time 25 data grants which are distributed from MDLUT as same interval are moved to DGCB and DS_GR is also moved at the 26th data. The size of DGGB is 32 bytes and sometimes DGGB can overflow in window opening scheduler. To prevent overflowing, DCCB inform MDLUT that it cannot receive data in the case that the address counter of DBCB have larger value than the number of the distributed grant (28) for half frame, to prevent overflowing. When DGCB scheduler derive the grant of itself to PLOAM cell and predictor. It delivers 26 grants per half frame.

E. MAC-MUX scheduler

MAC-MUX scheduler deliver the grant to the generator and predictor of PLOAM cell after selecting several kinds of grants handled in MAC according to priority or selecting grant which request fixed field. The order of delivering grant is decided by priority and the grant related to window opening has the highest order and the grant which will fill 26th field (that are PO_GR (PLOAM GRANT), unused grant and OMCC) has the second highest order. The grant which has lowest order is data grant (CBR, VBR), and DS_GR, UA_GR

A microprocessor help MAC-MUX scheduler to select PLOAM grant and OMCC grant periodically by writing active ONU in Alive Group Register (ARG). When the PLOAM cell is provided at the 27th grant field of the first PLOAM cell of the first frame per 4 frames or the OMCC cell grant is provided at the 27th grant field of the 2th, 4th, 6th frame AGR is referenced. If the bit value of appropriate AGR is 1 when PLOAM cell of 64 ONUS or OMCC grant is selected, the appropriate grant value is filled and if it is 0 UG_GR is filled

IV. A circuit design and verification of implementation

A. The process of verification

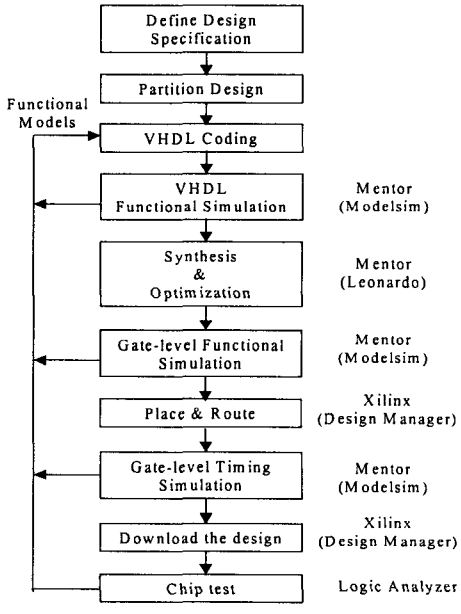


Fig. 6Hardware design flow.

The fig. 6 show the procedure of a designing FPGA by using Mentor and Xilinx tool. First of all, after coding OLT and ONU as VHDL (Very-high-speed Hardware Description Language), creating test vector and executing function verification by using Mentor(Modelsim) tools. Xilinx FPGA(xcv600e-7-hq240) is implementation by compounding OLT and ONU as Gate-level by placement and route through Xilinx tool. Timing simulation is also executed by using Modelsim

and receving delay information and resynthesized VHDL file from the result of P& R(Placement and Route). We finish confirming operation at the speed of 160Mbps by targeting a compounded circuit as Xilinx xcv600e-7-hq240 and then verify if the value of equalizing delay is measured exactly and the data sent from ONU to OLT is recovered or not. And also we finish verifying the accuracy of MAC operation and confirming it offer various bandwidth needed for ONU dynamically.

The TC_M compounded of single chip is compounded as 50% of the number of logic cell. (about 300,000 gate) in Xilinx xcv600e-7-hq240 and the used memory is the inter 1.8kbyte RAM. The operating speed of the embodied chip satisfied standard proposal of 155.52Mbps of up/downstream by verifying it at 160Mbps. Even though the ratio of error to bits is shown differently by special quality of optical module, this system operate with very stability and has no bit error up to ▯ 27dB at the result of test. So this system using several fiber core divided from a fiber core by splitter offers 32 (optionally maximum 64) optical subscriber system with connection to itself

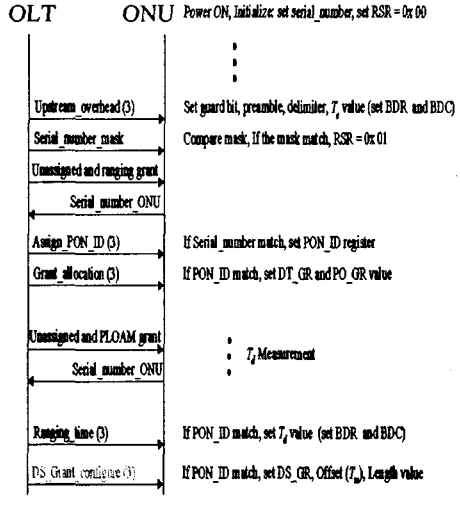


Fig. 7 Signal between OLT and ONU.

B. Experiment of working TC chip and software together

The fig. 7 show the signal between OLT and ONU. First when the power of ONU is on, several kinds of initiating occur. That process include writing a serial number and initiating 8 bits of Ranging Status Register(RSR) of ONU, RSR. It has the very first value of RSR=0x00. RSR[0] means the status of RR(Ranging Ready), RSR[1] means the status of GA(Grant Allocated), RSR[3] means the status of MC (Measurement Completed)and RSR[4] means the status of DC(Divided slot grant configured).

A general raging procedure is shown as below like fig. 7. The OLT transmit Upstream _overhead message that include contents of the overhead used by ONU in case that it transmit cells to upstream and preliminary assigned equalizing delay three times.

When Upstream _overhead message arrives ONU start to write the contents of three bytes of overhead and if there is the value of Te (preliminary assigned equalizing delay) it write that value. At the next step, in case that OLT know a serial number, it transmit Serial_number _mask message which include a whole serial number by loading with PLOAM cell at a time. If the value of mask in this message same with the serial number of ONU itself. It prepare to respond to raging cell and change the serial number to RSR=0x01.

After then, OLT open the window to know if there are ONUs trying to attend ranging and send ranging permission and unassigned permission to the downstream. According to this, if there are ONUs that respond, ONU respond with upstream ranging cell that include Serial_number_ONU message immediately or after Te. If this response message arrive at OLT without collision. OLT transmit assigned PON_ID through Assign_PON_ID message to ONU three times.

OLT can execute delivering message related to each ONU and OAM by means of 1 byte PON_ID not 8 bytes of serial number. OLT assign data permission (it makes ONU to send data) and PLOAM permission (it makes ONU to send permission) by means of three times of Grant_allocation message. Only in case that the upper process is done successfully, ONU renews

RSR to 0x02.

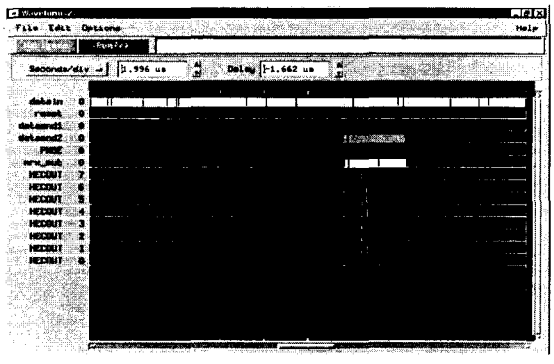


Fig. 8 The ranging cell observed by logic analyzer

Subsequently OLT starts to measure equalizing delay; that is value of Td. As shown figure 8, after the windows of PMSE (Phase Monitor and Synchronizer Enable) is opened, ONU respond according to PLOAM permission and succeed in measuring equalizing delay more than two times, OLT assigns the value of equalizing delay through ranging time message. If ONU is assigned the value of equalizing delay, OLT start to change the value of register into RSR=0x06 related to equalizing delay of ONU. Fig. 9. The mini-slot observed by logic analyzer.

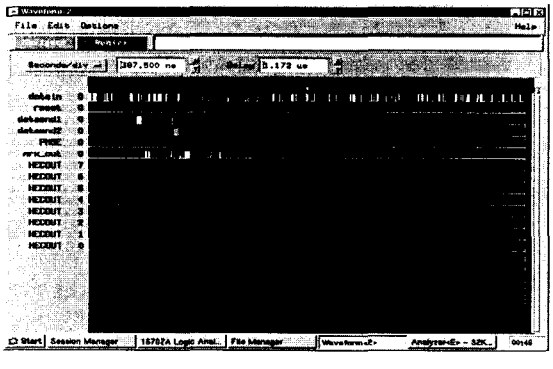


Fig. 9 The divided_slot observed by logic analyzer

Lastly OLT is assigned the grant value of divided_slot, offset value and length through Divided_slot_grant_configuration message.

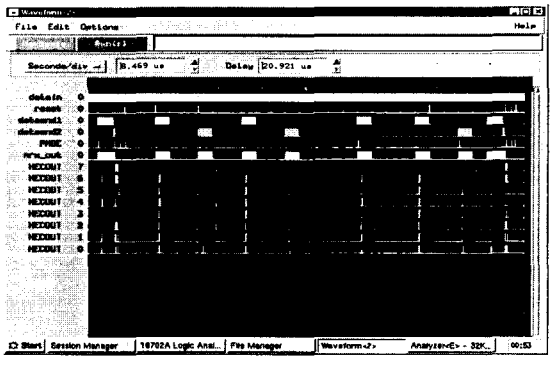


Fig. 10 The upstream frame observed by logic analyzer.

Therefore RSR is renewed to 0X0E. Fig. 9 show dataend1 signal and dataend2 signal in upstream mini_slot that is inputted to receipt tip of OLT in the form of mrx_out signal through optical connector and each offset value is 0 and 7 and the length is 7. MAC controller of APON fill payload field of min_slot which is a part of divided_slot with the information of MAC in each ONU for assigning upstream bandwidth dynamically and equally. Fig. 10 show mrx_out signal which is inputted to receipt tip of OLT when the length of Q of ONU1 is 5 and the length of Q of ONU2 is 3. At this time, MPR value is 1 and it is scheduled per half frame. So the result value of that makes equal distribution Fig. 10 upstream frame observed by logic analyzer. Fig. 11. show a picture of FPGA board.

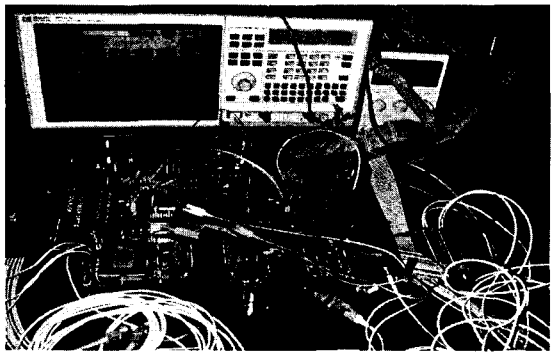


Fig. 11 A picture of FPGA board.

V. conclusion

In this paper, we propose and implement the algorism of MAC scheduler which can be programmed for providing ONUs with various bandwidth. First of all, we make the length of mini_slot in grant demanding protocol 7byts and implement that one divided_slot has 8 mini_slot. We can program that the maximum number of grant assignment are from 25 to 200 per every half frame, get total sum of the number of each activating ONUs and the length of Q and assign grant dynamically based on operating with limited algorism and also are able to program that a distributed range of assigned grant is half frame at the minimum to 4 frames at the maximum. Grant distribution is assigned per same interval by limited algorism. The grant cycle of PLOAM cell to ONU is 4 frame and located to 27th grant field of first PLOAM cell at 2th, 3th and 4th frame. In case that a CPU requests opening windows for ranging, the length of windows have to be 3 cells at the minimum to 127 cells at the maximum and have to be operated exactly to measure equalizing delay. And also considering chip dimension and operating speed, we design and propose grant distributor having the structure of variable look-up table which is a important element of MAC scheduler and confirm the quality of operation of MAC scheduler at FPGA board test and mock experiment by connecting embodied OLT and ONU. And we confirm if grant distributor is suitable for OLT by the information of the length of Q which is collected from ONUs.

TC_M which is compounded by single chip is compounded by 50% of logic cell(300000 gate) from the result 0f P&R in Xilinx xcv600e-7-hq240 the used memory in TC_M is 1.8K bytes internal RAM. Because the implemented operating speed of chip is verified at 160Mbps, it satisfy up/down stream 155.52Mbps of standard clue. Even though Bit error ratio get to be different according to special quality of optical module, this system is able to be operated stably having no bit error down to ▯ 27db. So APON (ATM Passive Optical Network) offers inter-connection between subscribers within a radius of 20 km in the form of FTTx(Fiber to any) and the cost of building APON(ATM Passive Optical Network) is low because maximum up to 32 (optionally up to 64) subscriber system using several fiber core divided from a fiber core by splitter can access to information super highway .

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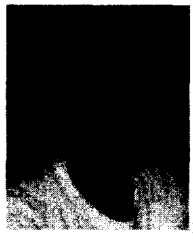
저자소개



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