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Design of a Digital PWM Controller for a Soft Switching SEPIC Converter

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ABSTRACT

This paper presents analysis, modeling, and design of a low-harmonic, isolated, active-clamped SEPIC for future avionics applications. Simpler converter dynamics, high switching frequency, zero voltage-Transition-PWM switching, and a single-layer transformer construction result. This paper describes complete design of a digital controller for a high-frequency switching power supply. Guidelines for the minimum required resolution of the analog-to-digital converter, the pulse-width modulator, and the fixed-point computational unit is derived. A design example based on a SEPIC converter operating at the high switching frequency is presented. The controller design is based on direct digital design approach and standard root-locus techniques.

Keywords: SEPIC converter, zero voltage-Transition-PWM switching, and a digital controller for a high-frequency switching power

1. Introduction

Future commercial aircrafts and vehicles will need high-performance isolated front-end converters for supplying power to loads such as in-flight entertainment systems in addition to the communication and navigation equipment. High-performance implies small distortion of the line current, as well as high efficiency, over a range of operating voltages and line frequencies.

It can be expected that digital controllers will be increasingly used even in low-to-medium power, high frequency switching power supplies where conventional analog controllers are currently preferred because of cost and performance reasons[1,2]. This paper addresses practical design of a digital controller for a power supply that operates at the high switching frequency.

Attention is given to the digital implementation with limited resources in terms of resolution of A/D and D/A (PWM) blocks and the time available to perform the required computations. Typical system under consideration is shown in Fig.1.

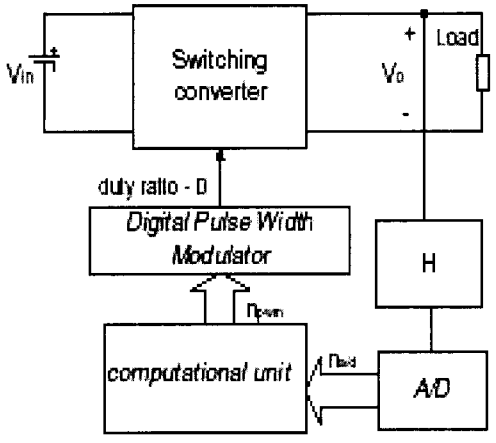

Fig.1. Digital control system for a switching converter

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2. STEADY STATE ANALYSIS

The active-clamped SEPIC with a definition of the switch network and waveforms of interest is shown in Fig. 2. The waveforms of the leakage inductance current (I_r.) and the clamp voltage across the main transistor (V_1) are shown in Fig. 3.

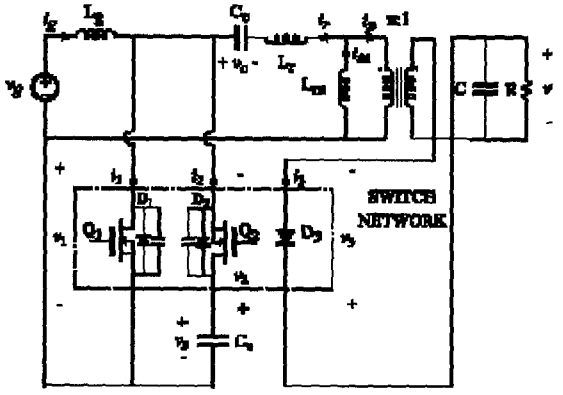
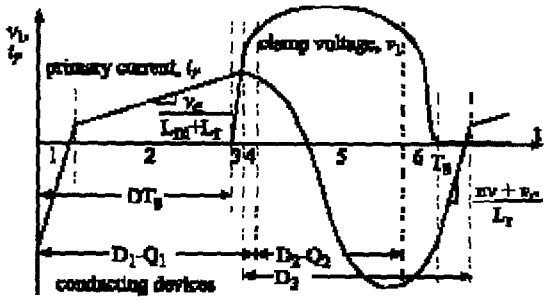


Fig. 2. Definition of converter currents and voltages and switch network.

Fig. 3. Steady-state waveform of the clamp voltage and primary current.



The conducting devices are also shown corresponding to the six intervals of a switching period. The main transistor-diode combination Q_1-D_1 conducts for time DT_s, where D is the duty cycle and T_s is the switching period. Interval 1 is the time when D_1 conducts and Q_1 has to be turned on with ZVT-PWM. Similarly Q_2 is turned on with ZVT-PWM shortly after interval 4 when the current in D_2 is still positive. During interval 5, the current in the leakage inductance reverses, and discharges C_1 during interval 6 [3].

A. ZVT-PWM condition

Let us define the following parameters [4,5]:

1. *M*: The over all output-to-input converter voltage gain,

$$M = \frac{V_o}{V_{in}} \tag{1}$$

2. V_{ng} : The normalized cell-input voltage to the converter input voltage, (V_{ng}=1+M for Sepic converter)

$$V_{ng} = \frac{V_g}{V_{in}} \tag{2}$$

3. I_{nF}: The normalized cell-output current to the converter output current, (I_{nF} =1+M for Sepic converter).

$$I_{nF} = \frac{I_F}{I_o} \tag{3}$$

4. V_{nF}: The normalized constant filter capacitor (C_F) voltage to the converter input voltage, (V_{nF} =1 for Sepic converter)

$$V_{nF} = \frac{V_F}{V_{in}} \tag{4}$$

5. I_{nT}: The normalized constant filter inductor (L_T) current to the converter output current, (I_{nT}=1 for Sepic converter)

$$I_{nT} = \frac{I_T}{I_o} \tag{5}$$

6. Z_o: The characteristic impedance,

$$Zo = \sqrt{\frac{L_r}{C_r}}$$

7. Q: The normalized load, $Q = \frac{R_o}{Z_o}$ Where R_o is the converter load resistor.

8. f_s: The switching frequency, $f_s = \frac{1}{T_s}$ Where T_s is the switching period.

9. f_o : The natural frequency, $f_o = \frac{1}{2\pi\omega_o}$ Where $\omega_o = \frac{1}{\sqrt{L_r C_r}}$, C_r the resonant capacitance and L_r the resonant inductance.

10. f_{ns}: The normalized frequency, $f_{ns} = \frac{f_s}{f_o}$

11. *D* : The duty ratio of the main switch.

12. D_1 : The duty ratio of the auxiliary switch.

13. α, β, γ, and δ: The intervals for the modes of operation.

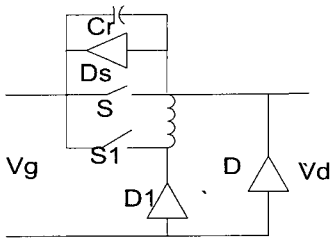


Fig. 4. ZVT-PWM Switching Cell.

Figure (4) shows the switching cell for ZVT-PWM. The switching waveforms of the modes of operation are shown in Figure (5). The generalized analyses for the switching-cell yields to the following generalized equations:

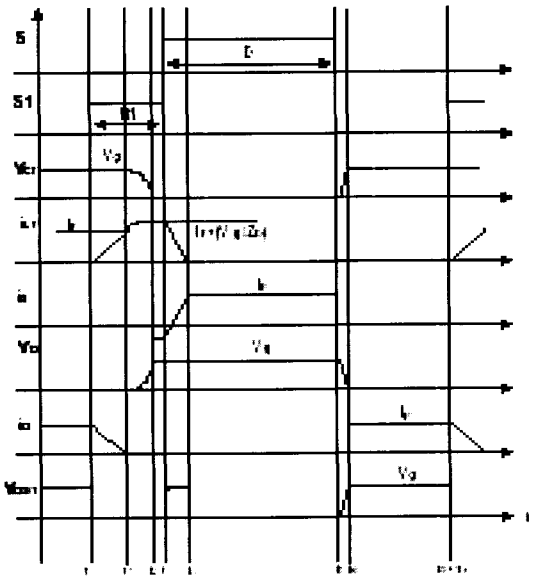


Fig. 5. Switching Waveforms for the ZVT-PWM Switching-Cell.

$$\alpha = \omega_o(t_1 - t_2) = \frac{MI_{nF}}{QV_{ng}} \text{ (Mode 1)} \quad (6)$$

$$\beta = \omega_o(t_2 - t_1) = \frac{\pi}{2} \text{ (Mode 2)} \quad (7)$$

$$\gamma = \omega_o(t_6 - t_5) = \frac{QV_{ng}}{MI_{nF}} \text{ (Mode 3)} \quad (8)$$

$$\frac{V_{nD}}{V_{ng}} = -(D + D_1) + \frac{f_{ns}}{2\pi}\left(1 + \alpha - \frac{\gamma}{2}\right) \text{ (Gain Equation)} \quad (9)$$

Other properties can be also obtained from the generalized analysis such as switches and component stresses and the range for the ZVT-PWM soft-switching condition. The generalized equation for the soft-switching condition for the switching cell is given by:

$$D_1 \geq \left[\frac{f_{ns}}{2\pi}\left(\alpha + \frac{\pi}{2}\right)\right] \quad (10)$$

Also, the normalized average main switch voltage is given by:

$$V_{n,sw\text{-}ave} = \frac{V_{sw\text{-}ave}}{V_{in}} = \frac{f_{ns}}{2\pi} V_{ng}\left[1 + \alpha + \frac{\gamma}{2I_{nF}} + \frac{2\pi}{f_{ns}}\left(1 - D - D_1 - \frac{f_{ns}}{2\pi}\gamma\right)\right] \quad (11)$$

B. Conversion ratio

To find the steady-state dc-dc conversion ratio, the usual inductor volt-second balance and capacitor charge balances are performed on the respective elements. The volt-second balance on L_g and L_m gives the following two equations

$$V_s = \frac{V_{in}}{D_1} \quad (12)$$

$$M = \frac{nV}{V_{in}} = \frac{D - X}{D_1 + X}\frac{1}{1 + \beta} \quad (13)$$

where

$$\beta = \frac{L_r}{L_m} \quad (14)$$

Charge balance on the output capacitor gives

$$M = \frac{D}{D_1}\frac{1}{(1+\beta)}\frac{2}{\left(1 + \frac{K}{D_1} + \sqrt{\left(1 + \frac{K}{D_1}\right)^2 + \frac{4KD}{D_1^2}}\right)} \quad (15)$$

where

$$K = \frac{2(L_r \| L_m)}{n^2 R_o T_s} \tag{16}$$

Duty cycle in terms of the conversion ratio can be expressed as:

$$D = \frac{(1+\beta)M}{1+(1+\beta)M}(1+K+K(1+\beta)M) \tag{17}$$

This expression allows us to predict the duty ratio variation over the line cycle when the required conversion ratio M is known. To find a condition for zero voltage switching of Q_1, a state-plane diagram (Fig.6) representing the resonance between L_r and C_r is utilized. ZVS is achieved when $r_2 > 1+M$. The condition is approximately expressed as [6]:

$$f_o \geq \frac{f_s}{\pi} \frac{\sqrt{(1+2M)D_1 - D}}{D_1(D - MD_1)} \tag{18}$$

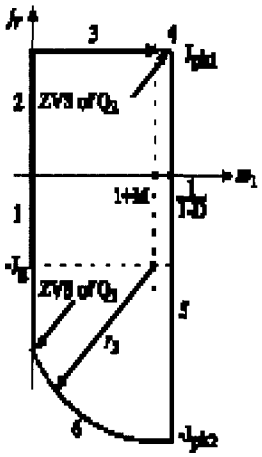


Fig. 6. Normalized state-plane diagram for finding ZVS Condition.

3. Resoution of Analog-to–Digital Converter and Digital Pulse Width Modulator

The system in Fig. 1 has an analog-to-digital (A/D) converter to sample the output voltage, a computational unit to determine the value of the switch duty ratio, and a digital pulse-width modulator (DPWM) that outputs a pulsating waveform that controls the switch(es) in the converter at the computed duty ratio. The DPWM serves as a D/A converter in the control loop. It is of interest to examine the required resolution of A/D and DPWM blocks [7].

A. Resolution of the A/D converter

To satisfy specifications for the output voltage regulation, resolution of the A/D converter has to enable error lower than the allowed variation of the output voltage ΔV_0:

$$\frac{\Delta V_o}{V_o} H \geq \frac{V_{\max_{a/d}}}{2^{n_{a/d}} V_o}, \quad H = \frac{V_{ref}}{V_o} \tag{19}$$

where:

V_{ref} - is the reference voltage

$V_{max\ a/d}$- is the full-range voltage of the analog-to-digital converter, assuming unipolar conversion in the range from 0 to $V_{max\ a/d}$

$n_{a/d}$ - is the resolution, i.e. the number of output bits of the A/D converter

H - is the output voltage sensor gain

Rearranging (19) gives the required A/D resolution:

$$n_{a/d} = \text{int}\left[\log_2 \frac{V_{\max_{a/d}}}{V_{ref}} \frac{V_o}{\Delta V_o} \right] \tag{20}$$

where,

int[ ] denotes taking the upper rounded integer value of the argument.

Equation (20) gives the minimum number of bits for the A/D converter to meet the design specifications in terms of the output voltage regulation. For example, if 2% variation of the output voltage is allowed, and if V_{ref} is at least 78.2% of the A/D full-range voltage, a 6-bit A/D converter can be used. The required A/D resolution can also be expressed in terms of the analog equivalent ΔV_q of the A/D least significant bit (LSB),

$$\Delta V_q \leq H \Delta V_o \tag{21}$$

B. Resolution of the digital pulse width modulator

Digital pulse width modulator (DPWM) produces a discrete set of duty ratio values. This means that in a steady state only a discrete set of output voltage values

can be obtained. If the desired output voltage value does not belong to one of these discrete values, the feedback controller will switch among two or more discrete values of the duty ratio. In digital control systems, this type of oscillation is known as the "limit cycle"[7].

A necessary condition to avoid the limit cycle oscillation is that the change in the output voltage caused by one LSB change in the duty ratio has to be smaller than the analog equivalent of the LSB of the A/D converter:

$$\frac{V_{\max a/d}}{H2^{n_{a/d}}} > V_g \Delta M(D) \quad or \quad \frac{\Delta V_q}{H} > V_g \Delta M(D) \tag{22}$$

For the SEPIC converter:

$$M(D) = D/(1-D), \quad \Delta M(D) = \frac{1}{2^{n_{PWM}}} \tag{23}$$

where, n_{PWM} is the DPWM resolution, i.e. the number of bits of the DPWM. Substituting (23) and (20) into (22) gives the required DPWM resolution:

$$n_{PWM} \geq \text{int}[\log_2(\frac{1}{1-D}(\frac{V_{ref}}{DV_{\max_{a/d}}}2^{n_{a/d}}+1))] \tag{24}$$

From (24) we can see that the minimum resolution of the DPWM depends on steady-state operating conditions in the circuit and the A/D resolution.

4. DIGITAL REGULATOR DESIGN APPROACHES

There are two basic approaches for digital controller design based on the conventional control theory: digital redesign and direct digital design. Based on comparisons of load transient responses, as well as achievable phase margin and bandwidth in power converter applications, direct digital design has advantages[8, 9]. On the other hand, digital redesign enables use of some of the well known controller design methods previously developed for continuous-time analog implementation. For the conventional digital controller design, or for applications of any of the methods offered by modern control theory, it is necessary to develop a discrete-time model of the converter. One approach is to take into account the switching action in the converter and treat the converter as a sampled-data system that leads naturally to a discrete-time model. Another, simpler approach is to start with a well-known continuous-time, averaged model of the converter and transform the model to a discrete-time equivalent using one of the well known transformation techniques.

Selections of the design and transformation method can be based on the system dynamics and constrains caused by limited resources available for implementation. For the converter configurations where the low frequency dynamics can be described with a first-order model (such as for converters in discontinuous conduction mode, DCM), a method with good transformation of integral properties can be used (Bilinear transform, Euler or Pole–Zero matching). These methods are also convenient for the case when the digital redesign is used and when a simple PI controller is adequate. For systems described by second-order dynamics and possibly RHP zeros [8] (such as converters in continuous conduction mode, CCM), methods that provide good transformation of integral and derivative properties (such as Pole-Zero Matching or Euler) give more accurate discrete-time equivalents of the continuous-time model. These methods also give a better transformation of controller properties if a digital redesign method is applied to a PID controller.

The controller was designed using the direct digital design approach. The system model is shown in Fig 7.

The closed-loop reference-to-output discrete-time transfer function C(z) of this system is:

$$C(z) = \frac{D(z)Z\{K_{pwm}(s)G_{vd}(s)\}}{1+D(z)Z\{K_{pwm}(s)G_{vd}(s)K_{a/d}(s)\}} \tag{25}$$

The transfer function of the DPWM is:

$$K_{pwm}(s) = K_{pwm} \cdot e^{-sT_{pwm}}, \quad K_{pwm} = \frac{1}{2^{n_{pwm}}-1} \tag{26}$$

The transfer function of the A/D is:

$$K_{a/d}(s) = \frac{K_{a/d}}{1+\frac{s}{\omega_{lp}}} e^{-sT_{a/d}}, \qquad K_{a/d} = \frac{1-2^{-n_{a/d}}}{V_{\max_{a/d}}} \tag{27}$$

The discrete-time transfer function H(z) of the analog plant is:

$$H(z) = Z\{K_{pwm}(s).G_{vd}(s).K_{a/d}(s)\} \tag{28}$$

In this case, the analog plant consists of the switching converter model, the pulse width modulator, and the analog-to-digital converter. The pole-zero matched transformation method was applied to obtain H(z).
The method is simple to apply and the discrete-time model has been shown to reproduce the plant transient responses with good accuracy. The obtained discrete-time control law is given by:

$$d[n] = d[n-1] + 52(e[n-1] + 0.8119e[n-2]) \tag{29}$$

where d[n] and d[n-1] are the new and one-cycle before values of the duty ratio, respectively, while e[n], e[n-1] and e[n-2] are the new, one-cycle before and two-cycles before values of the error signal.

Based on the DPWM resolution and the form of the control law, the hardware/software requirements for the computational unit can be found. Figure 8 shows a block diagram of the computational unit and the minimum number of bits needed for various blocks of the computational unit. Limited resolution of the fixed-point computational unit does not allow exact implementation of the control law. The closest approximation of the designed controller is given by:

$$d[n] = d[n-1] + 49.2(e[n] - 1.3e[n-1] + 0.81e[n-2]) \tag{30}$$

To reduce the number of multiplication, the control law described by (30) is rewritten in the following form:

$$d[n] = d[n-1] + 64(0.769e[n] - e[n-1] + 0.63e[n-2]) \tag{31}$$

The multiplication by 64 can be implemented using a shifting operation.

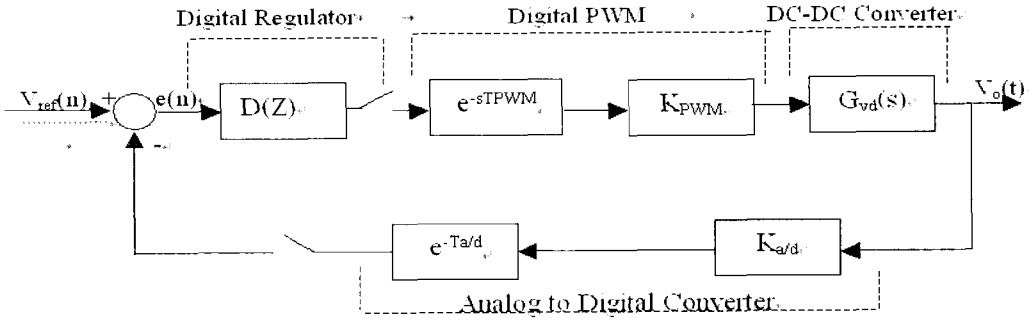


Fig.7. Block diagram of the digital control system

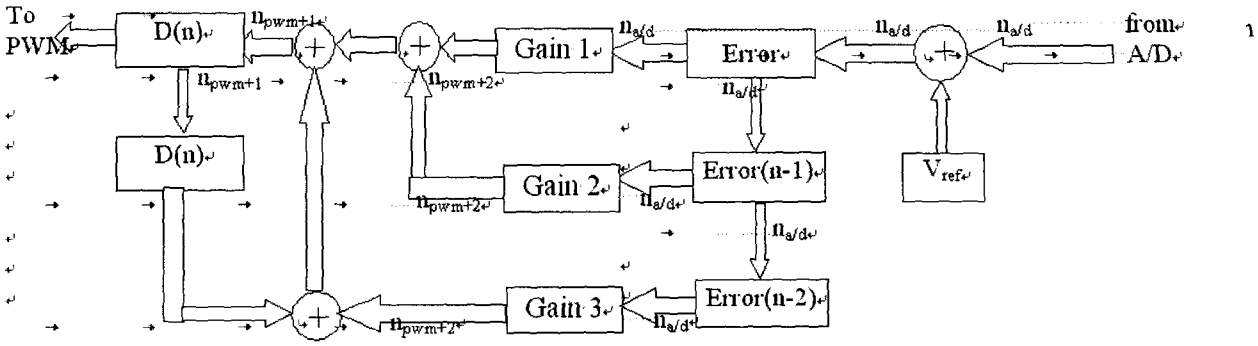


Fig.8. Block diagram of computational unit.

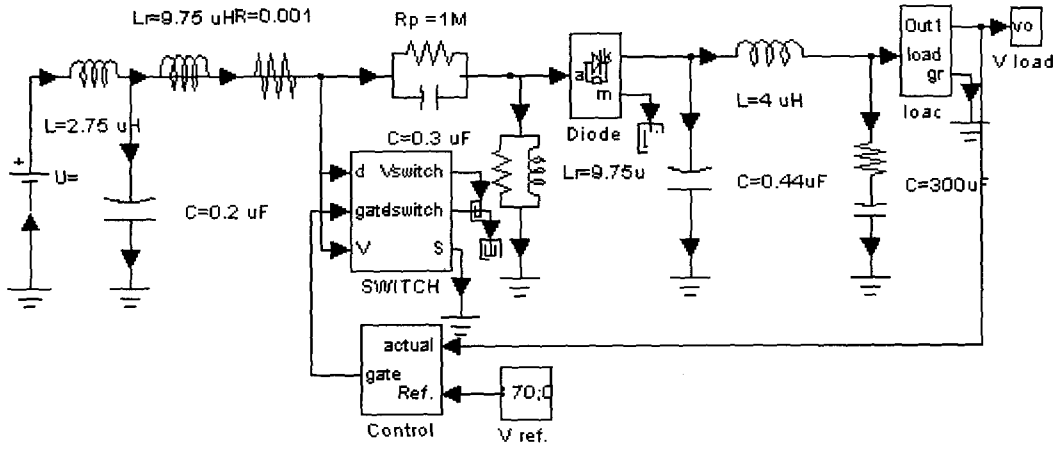


Fig. 9. The simulation of the SEPIC converter with PI control.

5. SIMULATION AND EXPERIMENTAL RESULTS

Converter simulations are performed in Matlab-power toolbox. It is shown in Fig. 9.

First, the dc-dc conversion ratio, input and output currents, intermediate voltages and power balance are verified at different duty cycles in open loop.

In Fig. 10 shows the output voltage and reference voltage with PI control at a change of the voltage reference from 50 volt to 70 volt. Fig. 11 (a) for simulation and (b) for experimentation show the important line voltage and current waveforms at nominal operating point.

Figures 12 (a) and (b) show load transient responses obtained in the experimental for the load current changes from 2.2A to 0.2A and from 0.2A to 2.2A. It can be observed that the load transients take about 30 μs to complete

6. CONCLUSIONS

This paper describes complete design and implementation of a digital controller for a high-frequency switching power supply. A SEPIC converter in PWM has a single-stage design with ease of isolation, a buck-boost conversion ratio for design flexibility, and input current with small ripple. Guidelines for the minimum required resolution of the analog-to-digital converter, the pulse-width modulator, and the fixed-point computational unit is derived. Experimental results are shown to validate the design approach and the allocation of resources in the implementation. It is shown how an active voltage clamp added to the SEPIC converter. It allows utilization of the transformer leakage inductance energy to achieve zero-voltages switching transistor while

limiting the peak voltage stresses on the transistor. A transformer having single-layered primary and secondary windings is designed to reduce proximity losses.

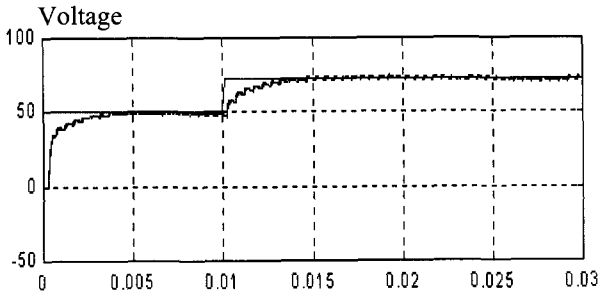


Fig. 10. The output and reference voltages of the converter.

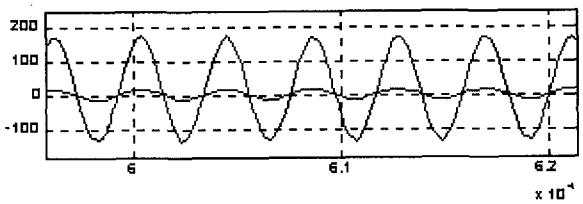


Fig. 11 (a) The simulation of line voltage and line current.

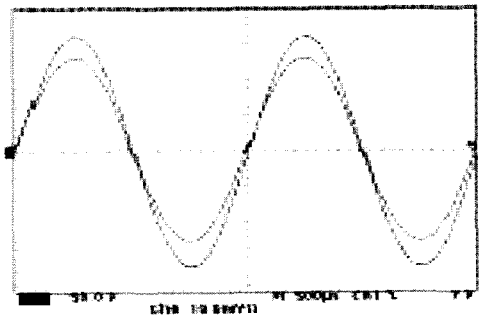


Fig. 11(b). The experimental of line voltage (outer at 50V/div) and line current (inner at 1 A/div).

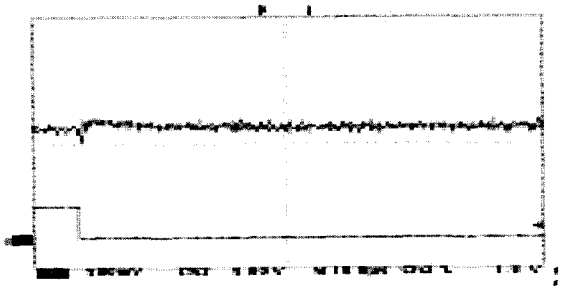


Fig. 12(a). Load transient response obtained with experimental system.

Change of output voltage (top) for the change for the output current from 2.2A to 0.2A

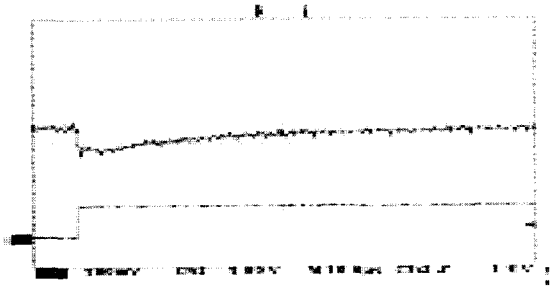


Fig. 12(b). Load transient response obtained with experimental system

Change of output voltage (top) for the change for the output current from 0.2A to 2.2A

Fig. 13 illustrates the limit cycle oscillation observed in an SEPIC converter when the DPWM resolution is too low.

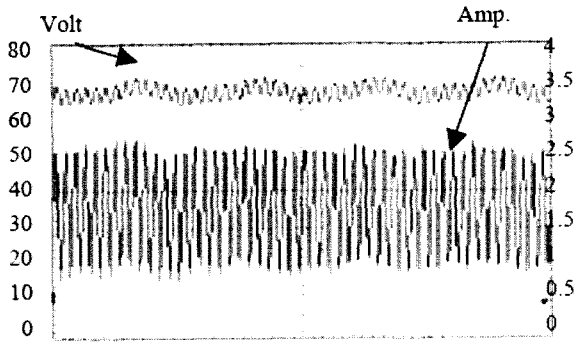


Fig.13(a). Output voltage (top) and inductor current (bottom) by low resolution of DPWM.

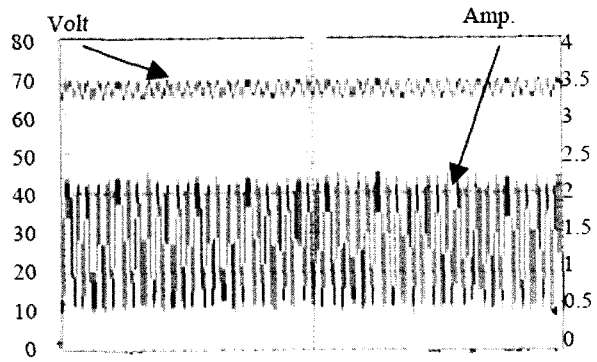


Fig.13(b). Output voltage (top) and inductor current (bottom) for the high resolution of DPWM.

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