論文
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IIPS를 위한 광선제어용 n-위상 OPTO-ULSI 프로세서의 디자인 (A Design of Beam Steering n-phase OPTO-ULSI Processor for IIPS)

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요 약

본 연구는 다기능의 광 네트워크에 있어서 256 위상 Opto-ULSI 프로세서를 구현하는 최적 위상 디자인을 제안한다. 이미 구성된 8 위상 프로세서에 대한 디자인의 실험 특성을 바탕으로 하여 본 연구에서 액정의 비선형성을 보정하며 최적의 위상을 찾아 대용량의 Opto-ULSI 프로세서를 구현할 수 있다. 이 연구는 최적의 위상 특성을 조사하고 액정의 비선형성 보정방법에 대한 개발을 통해 초기의 8 위상 Opto-ULSI 프로세서 개발을 중심으로 통합된 지능형 포토닉스 시스템 (IIPS)을 위한 광선제어 Opto-ULSI (BS) 프로세서 (OUP) 구현을 목표로 한다.

ABSTRACT

Thisstudy to design anoptimum phase implementing a 256 phase Opto-ULSI processor for multi-function capable optical networks. The design of an 8 phase processor is already in construction and will provide the initial base for experimentation and characterisation. The challengeis to be able to compensate for the non-linearity of the liquid crystal, find an optimum phase, and implement a larger scale Opto-ULSI processor. This research is oriented around the initial development of an 8 phase Opto-ULSI processor that implements a Beam Steering (BS) Opto-ULSI processor (OUP) for integrated intelligent photonic system (IIPS), while investigating the optimal phase characteristics and developing compensation for the non-linearity of liquid crystal.

Key words: Beam Steering, OPTO-ULSI, OPTO processor

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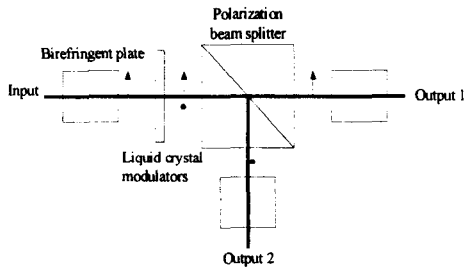
1.Introduction

In this age, the era of multimedia, there has been a tremendous bandwidth explosion in communication networks. High speed, long-distance and voluminous data transfers for data, voice, speech and moving images has come to be accepted as normal. These high bandwidth applications as well as use of the Internet as primary medium for data communication mean that there is currently an exponential growth of data traffic across the public communications networks. The facilitation ofthis high bandwidth demand and these new multimedia services is through the use of fibre optic technologies combined with application specific ULSI, which nowadays includes this concept of Opto-Electronic Integrated Circuits (OEIC). OEICs generally include optical components coupled with electronic ICs [1][2] whose example is the Opto-ULSI processor. This researchdevelops innovative concepts utilizing memory based pixels combined with 256 phase circuits for a Liquid Crystal on Silicon (LCoS) Opto-ULSIprocessor facilitate the implementation of intelligent reconfigurable photonic components and systems that provide high-bandwidth, ultra-parallel operation, and dynamic data interconnects. These new integrated intelligent photonic components will provide the new foundations for a future in which sensing, imaging, information processing and communication systems and networks will be pervasive. The steering and multicasting capability of this technology makes the Opto-ULSI processor exceptional for many applications, such as reconfigurable optical add/drop multiplexing, tunable optical filtering, dynamic spectral equalisation and variable true-time delay synthesis, dynamic optical interconnects, intelligent passive optical networks (PON), and adaptive photonic signal processing. Furthermore, the wavelength demultiplexing capability of the Opto-ULSI processor can be used to achieve dynamic add/drop multiplexing, tunable optical filtering, dynamic spectral equalisation and variable true-time delay. These features also make the system ideal for mobile multimedia type applications and, as all the components are based on standard CMOS technologies, it should also be suitable for low cost, low power consumer products [3].

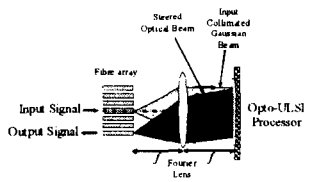
2.BeamSteeringOpto-ULSICell

An Opto-ULSI processor can steer a collimated beam with very high efficiency by applying an appropriate virtual blazed phase grating on the top layer of the silicon. Figure 1(a) shows the architecture of liquid-crystal 1x2 switch. It controls the polarised beam splitter to the desired states by the birefringent plate at the input. Without applying a bias, the laser passes through the liquid crystal and the polarisation beam splitter with the same polarisation. By applying a specific voltage on the liquid-crystal spatial modulator, it is rotated the liquid crystal molecules and resulted in changing the direction of the beam propagating through it. With sufficient voltage, the laser polarisation may rotate to orthogonality. The polarisation beam splitter then reflects the lasers to the other output port. Figure 1(b) shows the concept of a 1xN

Opto-ULSI-based optical switch. In this structure, a Fourier lens is used to convert the light emerging from an input optical fibre into a collimated beam with a suitable beam diameter. Then an appropriate holographic diffraction grating is uploaded ontothe Opto-ULSI processor. By changing the pitch of the blazed grating the collimated beam is steered and reflected back along a desired direction so that the Fourier lens focuses thesteered beam and couples it into an output fibre port [4].



(a)



(b)

Figure 1. (a) Architecture of a liquid-crystal 1x2 switch, (b) the architecture of a 1xN Opto-ULSI-based optical switch.

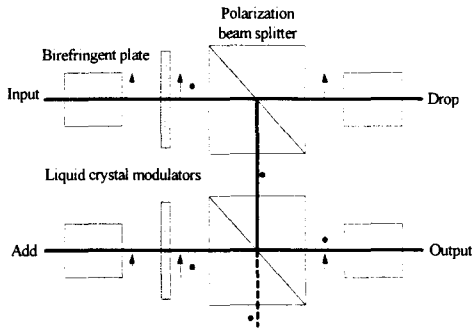


Figure 2. Architecture of an LC add/drop switch.

Figure 2 shows the architecture of a 2x2 add/drop switch. Without applying voltages on both liquid-crystal modulators, the input port connects to the drop port and the add port connects to the output port. With biasing voltages on the liquid-crystal modulators, the lasers from the input port are reflected by two polarisation beam splitters to the output port while the lasers from the add port are terminated in the optical cavity. The add/drop switch provides functionality of switching signals at the add/drop mode and protection of looping back added signals back to the drop port at the through mode [5].

An Opto-ULSI processor is a real-time reconfigurable device capable of impressing information onto an optical wavefront. Light phase modulation of Opto-ULSI processors may exist in many forms [6][9]. Figure 3 shows a schematic cross section through the pixel of a LCoS device. The device is illuminated with polarised light from above. A voltage between the pixel mirror and the common Indium Tin Oxide (ITO) counter electrode controls the state of the LC and hence the amount of the incident light reflected by the pixel. The voltage is maintained through the use of some form of

a storage element within the pixel. The applications of such devices are manifold and include information display, coherent optical data processing, data routing and holography. The overall field of Opto-ULSI processors has been reviewed in the past [3].

Figure 3. Schematic cross section through LCoS pixel.

There are currently two design types of Opto-ULSI processors. The first is based on Dynamic Random Access Memory (DRAM) while the other is founded on Static Random Access Memory (SRAM). In the DRAM design, each pixel consists of single transistor, grounded capacitor for information storage, and the top metal mirror. Since the information is stored as charge on the capacitor, this charge slowly leaks away so that the cell needs to be refreshed periodically.As a result, we have adopted the SRAM design, in which each memory cell is made up of the 6 transistors hence an 8-phase pixel is made up of the 3 memory cells, the multiplexer and the top metal mirror. In the 8 phase Opto-ULSI SRAM design, the function of the pixel is to switch one of eight phase input signals, translate one of the selected signal to a higher voltage (3.3 volts), and apply it to the top metal mirror (metal 6 in this chip). In each pixel there are three bits of data storage, which are based on three static RAM cells. The SRAM cells are based on a traditional six-transistor (6T) cell [6][7], comprised of two back to back inverters and input isolation transistors. The six bit line/bit bar line signals are all low voltage (1.8 volts). They are de-multiplexed through the multiplexer. The output voltage of the multiplexer is applied to a biased high-voltage inverter which has 2 transistors capable of 3.3V. Figure 4 shows the schematic of an 8 phase Opto-ULSI processors SRAM pixel.

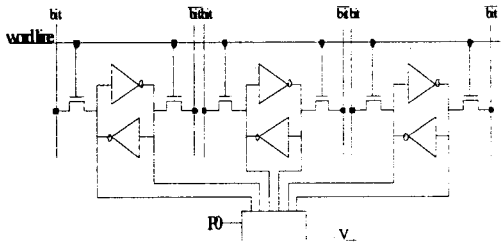
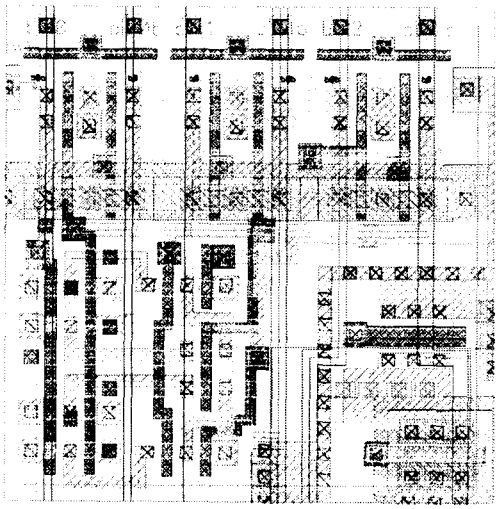


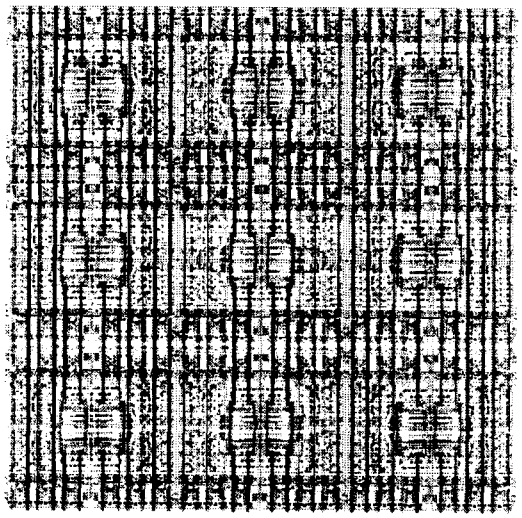
Figure 4. Schematic diagram of pixel with 6T SRAM cell.

Figure 5shows the layout for one pixel and for the pixel array. In this design, there are 2 voltage sources: 1.8 V for the SRAM cell and multiplexer and 3.3 V fora biased high-voltage inverter. The low voltage (1.8V) area is separated from the high voltage (3.3V) area using trench isolation as shown in Figure 5 where the area of the pixel is the world smallest size of 81m2. The pixel simulation consists of a transient simulation which simulates read/write operations into and from the SRAM cells and also simulates the functionality of the switch and the high voltage inverter. Figure 6 shows the simulation setup for the read/write operation of the SRAM cell. To write data to a cell, the write driver has to force the value into the cell and has to be able to overpower the transistors around the cell, which is critical,

especially when a '0' has to be written.



(a)



(b)

Figure 5. VLSI Layout for (a) one pixel (9m x 9m) and (b) for the pixel array.

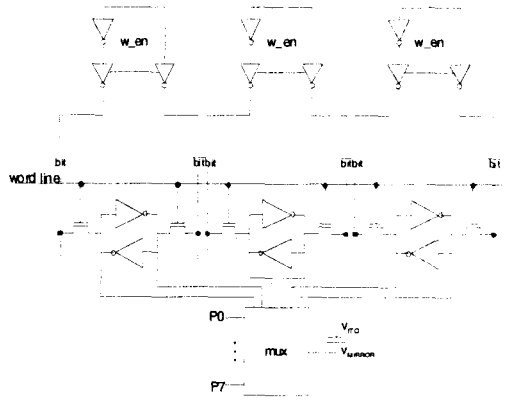


Figure 6. Simulation setup for the read/write operation of SRAM.

At the same time, when a read cycle is taking place or the circuit is simply not enabled, the write circuitry has to be completely cut-off from the other processes. This necessitates a tri-state device, which is enabled by write enable (WE) and write data (WD) allowing the data to be written. It is important in Figure 6 that the transistors driving the write driver circuitry are large, allowing the appropriate value to be written.

3.Opto-ULSIProcessor

3.18-PhaseArrayDesign

The total array size is 1024 X 1024 pixels in this design as shown in Figure 7. The array is divided into four blocks, each having 512 X 512 pixels. This is done to make the array as symmetric as possible and also to minimise the loading on the bit and ws lines. The control signals can be fed from the sides of the array minimising any increase in complexity.

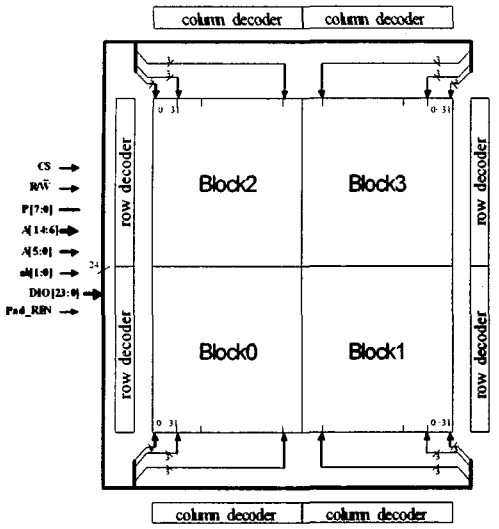


Figure 7. Schematic of the array design.

At the boundaries of the blocks, and between the row and column decoders, the power and ground lines are connected together whilst the intra-block signal lines are kept isolated. To accommodate the isolation of the signal lines, there is a small physical gap of 1 m between the blocks, which will have a negligible effect on the optical properties of the OPTO-ULSI processor and will result in optimised high density of the system.

3.2 Decoder Design for Opto-ULSI Processor

The decoding in this chip is performed separately for each block. The address lines are divided into two bits for selecting the block, six bits for selecting the columns, and 9 bits for selecting the rows. For the 8-phase SRAM design, NOR/NAND decoder is selected instead of other decoders in this design. To decrease potential glitches during signal transition, a SR latch is used in the address line. Figure 8 shows the schematic for the NOR/NAND type decoder ensuring the data validity and low power dissipation.

The proposed 256 phase Opto-ULSI processor is 12 x 12 mm in size with a 90% fill factor inclusive ofthe processing and interconnection circuitry. Layout of this device is depicted in figures 5(a) and (b). For an n-phase Opto-ULSI processor,a different implementation scheme must be utilised than that used for the 8 phase processor.

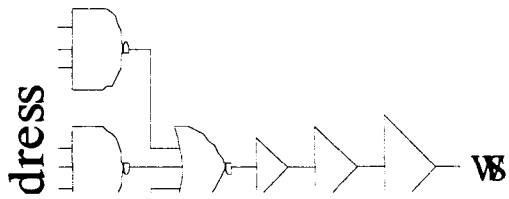


Figure 8. NAND/NOR Decoder.

The latter is implemented using an SRAM and a Multiplexer, but the former will have to use an alternative method, potentially using a shift register/counter instead of simple memory. There will be a corresponding increase in relative complexity, with the change from memory to register accounting for around 170 to 190 transistors per pixel alone.

3.3 ProposedOpto-ULSIProcessor

The main aim of this design is to investigate the possibility of finding an optimum phase fro a specific application and implementing and a 256 phase Opto-ULSI processor for multi-function capable optical networks. The design of an8 phase Opto-ULSI processor is already under construction as discussed in Section 3.1 and 3.2, and will provide the initial base for

experimentation. Therefore the challenge will be to compensate for the non-linearity of the liquid crystal, find an optimum phase, and implement an Opto-ULSI processor.

The research proposed in this research is oriented around the initial development of an 8 phase Opto-ULSI processor that is implemented in Opto-ULSI hardware, while focusing on the optimum phase and compensating for the non-linearity of liquid crystal. Figure 10shows the block diagram for n-phase array design for which this study is based. In this design, each pixel needs 8 bit linear shift register and a global clock for generating the different phase value. Figure 9 illustrates the basic pixel of an n-phase Opto-ULSI processor.

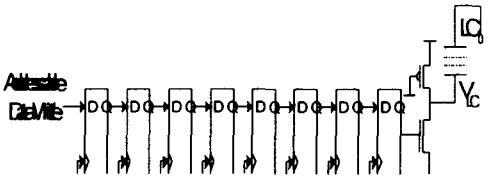


Figure 9. Basic block diagram of a proposed pixel.

A shift register consists of D flip-flop stages connected by a global clock that controls the input and output timing action of the flip-flops. The global clock runs at 256 times the phase clock, and a singular global circuit is added which generates the ITO signal, to get each different 256 phase. However, the main disadvantage of this circuit is the power required due to switching. To minimise the power consumption,gray code which is a special binary code that utilisesa single bit to change from one consecutive number to another is used in this design. The layouts and verification for the proposed 256 Opto-ULSI processor will be completed using 0.18m process and fabricated in the near future.

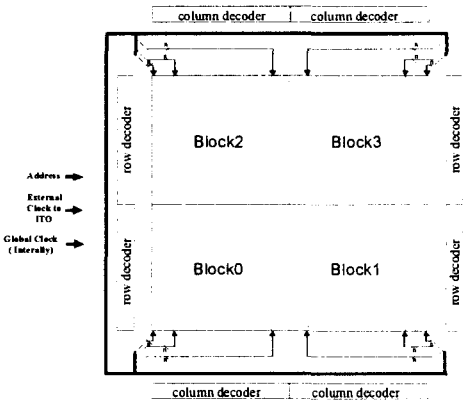


Figure 10. Block diagram for n-phase array design.

4.Conclusions

This research presents the realisation of a beam processor using Opto-ULSI technology that will be the "work-horse" of optical beam processing such as WDM, OXC, Add/Drop Multiplexing, proposing the implementation of 1 million pixel 8 phaseOpto-ULSI processor using LC (Liquid Crystal) on 0.18m CMOS silicon technology as part of a "sea-of-pixel" approach and, directing towards realisation of a 256 phase sea-of-pixels Opto-ULSI processor that introduces a significant advantage in applications whereby it is necessary to minimise cross-talk between optical channels. A novel concept of gray coded switching activity and NAND-NOR combined decoder for low power consumption and of compact layout optimisation for high density design is also presented to design the 256 phase OUP system.

5.References

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