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심볼간 간섭 채널을 위한 고정 지연 신호 검출기

(Fixed Decision Delay Detector for Intersymbol Interference Channel)

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요 약

순차적인 관찰값을 바탕으로 하고 신호검출에 소요되는 시간이 고정된 신호검출기의 제작에 관한 방법을 제안하며 이는 하드웨어의 복잡도를 감소시키는 장점이 있다. 제안된 방법은 Voronoi 다이어그램과 Delaunay 분할을 사용한다. 제안된 신호검출기 제작은 또한 고정 지연 트리 검색 검출 (FDTS) 방법에 기반을 둔다. FDTS 는 효율적인 순차적 신호검출 알고리즘이며 심볼간 간섭이 존재하는 채널에서 결정 궤환 등화기법 (DFE)과 결합하여 최적화에 근접한 성능을 보인다. 이러한 접근방법에서는 Voronoi 다이어그램 혹은 등가적으로 Delaunay 분할에 포함된 정보를 활용하여 다차원 유클리드 공간에서의 상대적인 관찰값의 위치를 계산하며 이러한 방법이 효율적인 계산을 유도하는 신호검출기의 제작에 이용된다 .

Abstract

A design method is proposed for the sequence detection with fixed decision delay with less hardware complexity using the concept of the Voronoi diagram and its dual, the Delaunay tessellation. This detector design is based on the Fixed Delay Tree Search (FDTS) detection. The FDTS is a computationally efficient sequence detection algorithm and has been shown to achieve near-optimal performance in the severe Intersymbol Interference (ISI) channels when combined with decision feedback equalization and the appropriate channel coding. In this approach, utilizing the information contained in the Voronoi diagram, or equivalently the Delaunay tessellation, the relative location of the detector input sequence in the multi-dimensional Euclidean space is found without any computational redundancy, which leads to a reduced complexity implementation of the detector.

Keywords : Intersymbol interference, Euclidean distance, Voronoi diagram, decision feedback equalization.

I. Introduction

The Voronoi diagram (VoD) is an important geometric structure and there have been numerous applications of this structure in computational geo -metry areas. Some of the applications include the efficient file management in the computer systems, the motion control in robot systems and the artificial neural network design[1][2]. In our application, the Voronoi diagram and the Delaunay tessellation is applied to the detection of the binary data in the intersymbol interference (ISI) channel. The ISI channel in the discrete time domain can be expressed in terms of linear combination of the channel input data and the channel impulse response[3]:

$$r_k = \sum_i f_i x_{k-i} + n_k \tag{1}$$

where r_k is the sampled received signal, f_k is the channel impulse response and n_k the noise compo -nent, respectively. The detection of the binary data in the ISI channel is equivalent to the estimation of the input x_k value based on the received samples r_k. In the following discussions, the concept of the Voronoi diagram and the Delaunay tessellation (DT)

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is applied to solve this binary detection problems especially in the ISI communication channel. The second section discusses the fixed delay tree search with decision feedback (FDTS/DF) detection scheme. In the third section, some of the basic concepts of the Voronoi diagram and its dual are reviewed. The fourth section describes application of Voronoi diagram and the Delaunay tessellation to the FDTS detector design. In the fifth section, the design example in the ISI channel is discussed.

II. Fixed Delayed Decision Feedback Equalization

The discrete time model for a general ISI channel combined with the FDTS/DF[4][5] is shown in Fig. 1. Here $x_k \in \{-1, 1\}$ is the channel input binary data and n_k is the additive Gaussian noise sampled at time $t = kT$, where T is the sampling period. With this linear channel model, the detector input r_k can be represented as a linear combination of the input x_k and the equalized channel response assuming the past decisions are correct :

$$r_k = \sum_{i=0}^{\tau} f_i x_{k-j} + n'_k = y_k + n'_k \tag{2}$$

where n'_k and y_k are the noise sample at the output of the forward filter and signal portion of the detector input, respectively, and f_k is the equalized channel impulse response and can be expressed in the frequen -cy domain as follows:

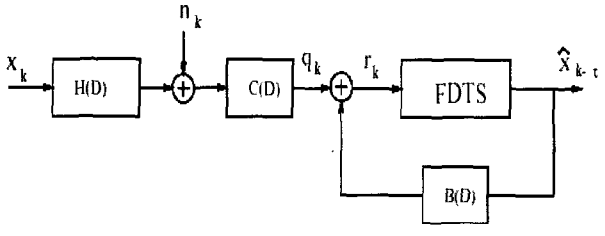

그림 1. 일반적인 심볼간 간섭채널에서 결정 궤환 FDTS 검출을 위한 채널모델.

Fig. 1. The discrete time channel model for a general ISI channel combined with the FDTS detector with decision feedback equalization.

$$F(D) = H(D)C(D) \tag{3}$$

where D represents one sample period delay and $H(D)$ and $C(D)$ are the discrete time channel impulse response and the impulse response of the forward equalizer, respectively. The equalizer consists of a forward filter and a feedback filter as in the conventional DFE structure[9][10]. The forward filter ($C(D)$ in our model) suppresses only the precursor intersymbol interference (ISI) terms, allowing residual postcursor ISI terms, but unlike the conventional DFE case, the feedback filter in FDTS/DF does not cancel all the residual postcursor terms allowing the first τ terms. The signal portion of the received sample at the output of the forward filter, q_k can be represented as the residual postcursor ISI terms as follows:

$$q_k = x_k f_0 + x_{k-1} f_1 + \cdots + x_{k-N} f_N. \tag{4}$$

At the input of the detector, only the τ ISI terms remain by the effect of the feedback filter, where $\tau \leq N$. The impulse response of the feedback filter in the frequency domain $B(D)$ can be expressed in terms of f_k as follows:

$$B(D) = \sum_{i=\tau+1}^{N} f_i D^{i-\tau} \tag{5}$$

where the length of the feedback filter is $N-\tau$. These uncanceled ISI terms (as many as the tree depth τ are utilized in the detection process to increa -se the effective minimum distance between the noise free channel output sequences. The original FDTS /DF with depth τ uses a binary tree with tree-depth τ to find the noise free detector input sequence close -st to the equalized noisy channel output sequence. The tree used in the FDTS/DF with depth 2 detector is shown in Fig. 2. The labels on each branch (1 or -1) represent the channel input data values at the corresponding time. There are 8 possible distinct paths in the look-ahead tree. At each clock cycle, the accumulated metric is computed for each of $2^{\tau+1}$ paths by comparing the nominal detector input se

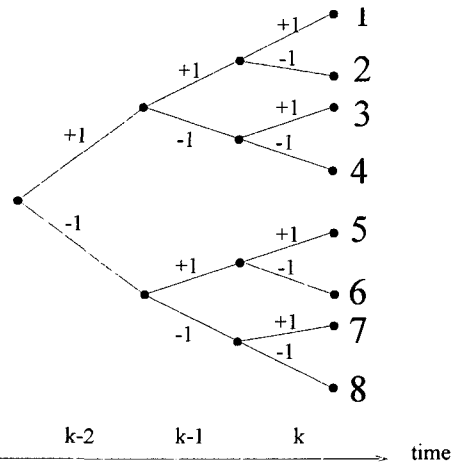

그림 2. 결정지연 시간이 2인 FDTS를 위한 트리구조

Fig. 2. The depth-two tree used for FDTS with $\tau = 2$.

-quence and the noisy channel output sequence. The accumulated path metric for the i_{th}

path at time k, $m_k^{(i)}$ is defined as the sum of the branch metric for the i_{th} path at time k, $\lambda_k^{(i)}$ and its appropriate parent path metric $m_{k-1}^{(i)}$ as follows:

$$\lambda_k^{(i)} = (r_k - y_k^{(i)})^2,\ 1 \le i \le 2^{\tau+1} \qquad (6)$$
$$m_k^{(i)} = m_{k-1}^{(j)} + \lambda_k^{(i)},\ 1 \le j \le 2^{\tau},\ 1 \le i \le 2^{\tau+1}$$

where $y_k^{(i)}$ is the noiseless detector input value at time k associated with the i_{th} path in the look-ahead tree. The appropriate parent path metric of each branch metric is decided depending on the previous decision value. If the smallest accumulated metric belongs to one of the upper half of the paths, "1" is decided as the estimated channel input binary data. Otherwise, "-1" is decided. Depending on which symbol is decided, only the upper half (in case of "1" detection) or lower half (in case of "-1" detection) of the paths are retained for the next iteration.

In the non-recursive path metric computation approach, the release of the detected data in the previous iteration is handled by including the internal feedback loop (separate from the ISI cancelling feedback filter, $B(D)$) while the original formulation of FDTS/DF manages this by appropriately discar-ding half of the tree at each iteration. In this approach, the detection is performed on the sequence of new detector input variable r'_k which are indepen-dent of the set of the previously detected binary data $\{\hat{x}_{k-\tau-1},\ \hat{x}_{k-\tau-2},\ \cdots,\ \hat{x}_{k-2\tau}\}$. These r'_k's are obtained by the internal feedback loop and can be expressed in terms of r_k as follows:

$$r'_{k-1} = \begin{cases} r_k, & \text{for } l = 0 \\ r_k - \sum_{i=\tau-l+1}^{\tau} f_i \hat{x}_{k-i-l}, & \text{for } 1 \le l \le \tau \end{cases} \qquad (7)$$

For the detection, the Euclidean distances between the detector input vector $[r'_k, r'_{k-1}, \cdots, r'_{k-\tau}]$ and the $2^{\tau+1}$ possible noiseless input vectors (which are also adjusted in the same way as in r'_k's) are measu-red and the decision is provided depending on the noiseless input vector which is closest to the noisy input vector and its associated $x_{k-\tau}$ value. The detection process in this non-recursive approach is equivalent to finding the nearest neighbor of the detector input vectors in the $\tau+1$ dimensional Euclidean space.

In the following sections, a new systematic way of design procedure for the FDTS detector with less hardware complexity using the concept of the Voronoi diagram and the Delaunay tessellation is discussed.

III. Review of VoD and DT

In this section, some of the basic concepts and the construction of the Voronoi diagram (VoD) and the Delaunay tessellation (DT) are reviewed which are related to the FDTS detector design.

The Voronoi diagram associated with a set of n points, $\{p_1, p_2, \cdots, p_n\}$, in the d-dimensional space partitions the space into n convex regions such that each region V_i, $1 \le i \le n$, contains the points lying nearer to p_i in its interior than to any other point, p_j, $j \neq i$[6]. The equation for B_{ij}, also called the linear

discriminant function in decision theory [7], is given by

$$h_{ij}(q)=\frac{1}{2}(p_i-p_j)\cdot q-\frac{1}{4}(p_i+p_j)\cdot(p_i-p_j) \quad (8)$$

where q is an arbitrary vector and ' $\cdot$ ' denotes the inner product operation in a d-dimensional space. When q is on the boundary B_{ij}, $h_{ij}(q)$ becomes zero. This equation can be used as a discriminant function for where a point q is located. If the function value is greater than zero, then the point q is in region H_{ij}. The region V_i can be represented in terms of B_{ij}, or equivalently H_{ij}, as follows:

$$V_i=\bigcap_{1\le j\le n, j\neq i} H_{ij} \quad (9)$$

This means that the Voronoi region associated with p_i, equivalently V_i, is the intersection of all half-spaces associated with p_i and p_j, $j\neq i$. But in this intersection, there could be some redundant half-space terms. The Delaunay tessellation, which is a dual of the Voronoi diagram, can be used to identify the redundant half-spaces (or equivalently redundant hyperplane boundaries) which is discussed in more details related to the binary symbol detection problems in the following section.

IV. Application to FDTS Detector Design

In this section, the design procedure for the FDTS detector with reduced hardware complexity using the concept of Delaunay tessellation is described in detail. The decision process in the FDTS detector with depth τ is equivalent to finding the nearest neighbor of the detector input vector in the $\tau+1$ dimensional Euclidean space[5][8], in which there exist $2^{\tau+1}$ compe -ting signal points. Half of these points correspond to $x_{k-\tau}=1$, and the other half to $x_{k-\tau}=-1$, where x_k is the channel input binary data at time k. Here the " *time* k" means the time at which the decision $\hat{x}_{k-\tau}$ is made. When the detector input vector is closest to one of the half of the points which correspond to $x_{k-\tau}=1$, then $\hat{x}_{k-\tau}=1$ is decided. Otherwise, $\hat{x}_{k-\tau}=-1$ is decided as the detector output. This can be rephrased as follows using the concept of the Voronoi diagram:

$$\hat{x}_{k-\tau}=\begin{cases} 1 \text{ if } \mathbf{r}'_k\in \bigcup_i V_i,\ 1\le i\le 2^\tau \\ -1 \text{ otherwise} \end{cases} \quad (10)$$

where we assume that V_i, $1\le i\le 2^\tau$, are the Voronoi regions associated with $x_{k-\tau}=1$, and $\mathbf{r}'_k=[r'_k, r'_{k-1},\cdots, r'_{k-\tau}]$ is the detector input vector at time k whose elements are described as in (7). The Voronoi region, V_i, is the convex polyhedron defined by

$$V_i=\bigcap_{1\le j\le 2^{\tau+1}, j\neq i} H_{ij} \quad (11)$$

where H_{ij} is the closed half-space in which all the points are closer to the point i than to point j as defined in the previous section. Equation (8) can be used to determine whether the detector input vector $\mathbf{r}'_k$ is in the region V_i or not. But the direct implementations of the decision procedure based on (11) (to determine whether the detector input vector is inside the region V_i or not) include a lot of redundancies. This means that some of the closed half-spaces (bounded by hyperplanes) are redundant in the intersection in (11). The Delaunay tessellation can be used to find the non-redundant half-spaces (or equivalently, non-redundant hyperplanes) in the intersection in (11). This is equivalent to finding two points i and j whose corresponding Voronoi polyhedra intersect in a face. These two points are called Delaunay neighbors. Now we have all the necessary hyperplanes that are required to determine whether a point in $\tau+1$ dimensional space belongs to V_i, $1\le i\le 2^\tau$, or not. Once we identify the hyperplanes associated with the Delaunay neighbor pairs, we can readily set up the detection rule that

estimates the value of delayed binary channel input, $x_{k-\tau}$ as follows:

$$\hat{x}_{k-\tau} = \begin{cases} 1 & \text{if } \mathbf{r}'_k \in \mathrm{Y}(\mathrm{I}_i \mathrm{I}_j H_{ij}),\ 1 \le i \le 2^\tau,\ i \ne j \\ -1 & \text{otherwise} \end{cases} \quad (12)$$

where i and j is defined such that point i is the Delaunay neighbor of point j. In the FDTS/DF detection scheme, however, the required hyperplanes in the decision are the ones which partition the $\tau+1$ dimensional space into two regions. One region associated with the channel input value, $x_{k-\tau}=1$, the other region with $x_{k-\tau}=-1$. For each point i, some of the neighbor pairs (i,j) can be further eliminated without affecting the overall decision boundary. The Delaunay neighbor pairs (i,j) or equivalently the half spaces H_{ij} are redundant in the binary data detection point of view as long as each Voronoi region V_i, $1 \le i \le 2^\tau$, which is assumed to belong to one class $x_{k-\tau}=1$ and is created by the intersection of all the half spaces, H_{ik} except H_{ij}. (where both the point k and the point j are the Delaunay neighbors of the point i), dose not intersect with any region which belongs to another class $x_{k-\tau}=-1$. In other words, for each point i, some of the Delaunay neighbor, point j, is redundant in the binary detection point of view if the following condition holds:

$$(\mathrm{I}_k H_{ik}) \mathrm{I}\ R^- = \phi,\ i \ne k \text{ and } k \ne j \quad (13)$$

where both the point j and k are the Delaunay neighbors of point i, R^- represents the region where $x_{k-\tau}=-1$ and point i is assumed to be one of the noiseless detector input vector associated with $x_{k-\tau}=1$.

In the implementation point of view, each term in the intersection in (12) can be implemented by a $(\tau+1)$-tap finite impulse response (FIR) filter whose coefficient values can be determined by the discriminant function shown in (9). The output value of each FIR filter is added by a threshold term (θ_{ij}) and this is passed through a two level slicer whose output value is either 0 or 1, depending on the region where the detector input vector $\mathbf{r}'_k$ belongs. The slicer outputs are connected to the input of the logical AND gate and the outputs of the AND gate consist of each term in the union in (12). Each term in the union is connected to the input of the logical OR gate and the binary output value of OR gate is used in the decision. The block diagram of FDTS detector with depth τ using the Delaunay tessellation is shown in Fig. 3. This block diagram has the same structure as the multi-layer artificial neural network, since AND and OR can be also converted into the neuron structure by simple algebra[2].

V. Detector Design Example

In this section, the design example of the FDTS detector with depth 2 are described in ISI commu -nication channels. The channel impulse response is assumed to be $\{f_k\} = \{1.0, 0.4, -0.1\}$ which is the typical response in the high data rate (high density) digital storage channel.

As the first step in the detector with depth $\tau=2$

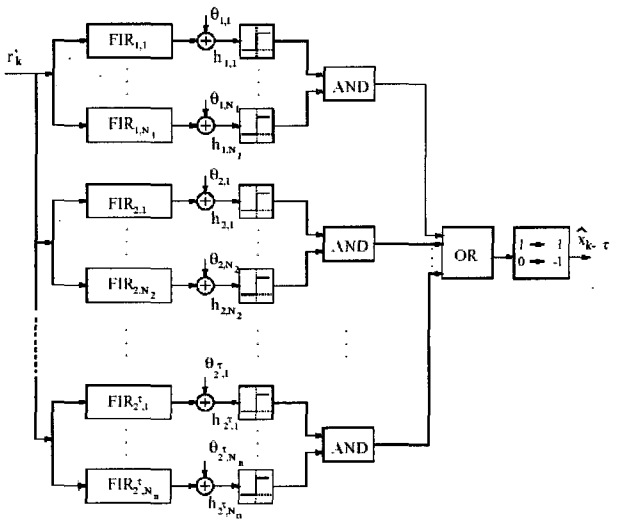

그림 3. Delaunay 분할방법을 사용하여 구성한 지연시간 τ 의 FDTS 검출기의 블록도.

Fig. 3. Block diagram of FDTS detector with depth τ using the Delaunay tessellation method.

design procedure, we have to figure out all the 8 possible noise free detector input vectors in the 3 dimensional space. Once the 8 vectors are obtained, the algorithm for the Delaunay tessellation and the test condition for the redundant Delaunay neighbors shown in (13) are applied to get the necessary and sufficient hyperplanes which divide the $\tau+1(=3)$ dimensional space into two regions. Under our channel environment with tree depth $\tau=2$, 9 hyperplanes are shown to be involved in this division. Table 1. shows the Delaunay neighbor pairs which are necessary for the construction of the decision boundaries. In this table, the column and row indices represent the indices of the noiseless detector input vectors and the column-row index pairs of the "o" marked position indicate the Delaunay neighbor pairs. Here we list only the sufficient pairs for the binary detection. Then the detection rule using the non-redundant half spaces can be readily set up for the $\tau=2$ case as described in (14):

$$\hat{x}_{k-2}=\begin{cases} 1 \text{ if } \mathbf{r}'_k \in (H_{15} \cap H_{16}) \cup H_{26} \\ \qquad\qquad \cup (H_{35} \cap H_{36} \cap H_{37} \cap H_{38}) \\ \qquad\qquad \cup (H_{46} \cap H_{48}) \\ -1 \end{cases} \tag{14}$$

where $\mathbf{r}'_k$ is the detector input vector as described in the previous section. For the implementation of this detection rule with minimum number of multipliers, each term in the discriminant function involved in the detection boundary should be rearranged by factoring out the channel coefficients. The resulting detector is shown in Fig. 4. The BER curves for DFE and the FDTS detector with $\tau=2$ is shown in Fig. 5. for the performance comparison. FDTS detector with $\tau=2$ has about 1 dB gain over the conventional DFE at BER=10^{-5}.

VI. Conclusion

A systematic way of designing the FDTS detector is proposed. This design method uses the concept of the Voronoi diagram and its dual the Delaunay tesse

표 1. 예시된 채널을 위한 Delaunay 인접페어를 위한 표.

Table 1. A table of the Delaunay neighbor pairs for the example.

	1	2	3	4
5	O		O	
6	O	O	O	O
7			O	
8			O	O

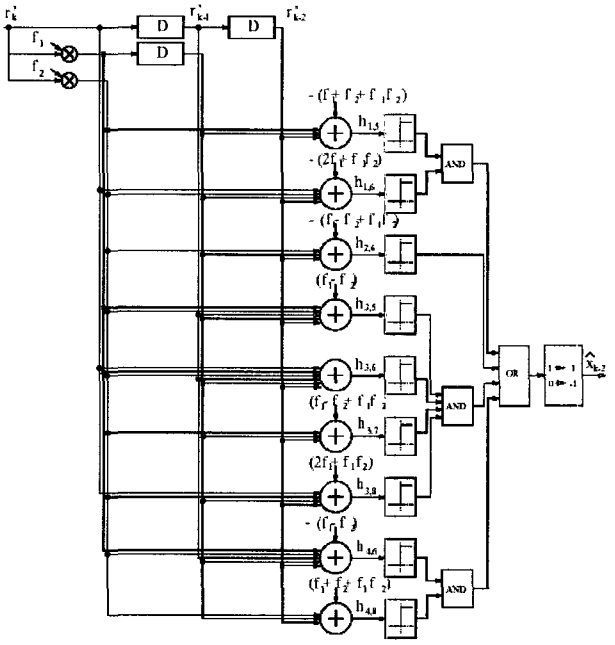

그림 4. 채널 임펄스 반응이 {1.0, 0.4, -0.1}인 채널을 위한 지연시간 2인 FDTS 검출기의 구현

Fig. 4. Implementation of FDTS detector with $\tau=2$ for channel impulse response, {1.0, 0.4, -0.1}.

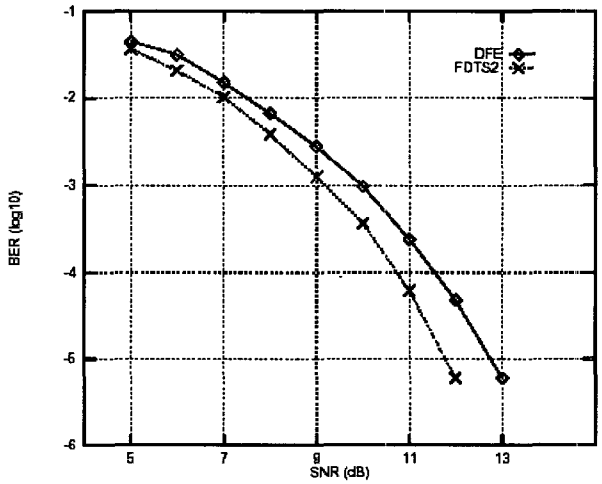

그림 5. 예시된 채널을 위한 비트 오류율.

Fig. 5. Bit-error-rate curves for the example channel.

-llation. The method is essentially the procedure for finding the minimum number of hyperplane bounda -ries and the multipliers for the binary detection problem in the multi-dimensional space with the application of the efficient multi-dimensional space partitioning techniques. This method is shown to significantly reduce the hardware complexity of the FDTS detector without any performance degradation. Design example in the ISI communication channel environment shows that the required number of multipliers increases linearly with the depth τ while the required number in the original tree-search algorithm increases exponentially.

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