CMOS Compatible Fabrication Technique for Nano-Transistors by Conventional Optical Lithography

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Abstract—**The trend of decreasing the minimal structure sizes in microelectronics is still being continued. Therefore in its roadmap the Semiconductor Industries Association predicts a printed minimum MOS-transistor channel length of 10 nm for the year 2018. Although the resolution of optical lithography still dramatically increases, there are known and proved solutions for structure sizes significantly below 50 nm up to now.**
In this work a new method for the fabrication of extremely small MOS-transistors with a channel length and width below 50 nm with low demands to the used lithography will be explained. It's a further development of our deposition and etchback technique which was used in earlier research to produce transistors with very small channel lengths down to 30 nm, with a scaling of the transistor's width. The used technique is proved in a first charge of MOS-transistors with a channel area of W=200 nm and L=80 nm. The full CMOS compatible technique is easily transferable to almost any other technology line and results in an excellent homogeneity and reproducibility of the generated structure size. The electrical characteristics of such small transistor will be analyzed and the ultimate limits of the technique will be discussed.

Index Terms—**CMOS Process; Nanostructure; MOS transistor**

I. INTRODUCTION

Regarding the 2003 Edition of the International Technology Roadmap for Semiconductors [1], a significant increased scaling of the minimum MOS-transistor structure sizes for the next 15 years is predicted. The minimal printed transistor gate length should be decreased from 80 nm yet to 10 nm in the year 2018, which will result a physical channel length of 7 nm.

The resolution of optical lithography continually increases, but to date there are no known and proven solutions for mass production of transistors with structure sizes well below 50 nm with the needed accuracy and reproducibility. Existing alternatives such as e-beam or X-ray lithography do not allow a cost-effective mass production of integrated circuits.

In previous publications we already demonstrated a novel deposition and etchback technique which made it possible to produce transistors with a channel length down to 30 nm with excellent homogeneity and reproducibility and low demands to the used lithography [2-4]. The technique applied only conventional optical lithography. The main idea of that technique was the use of optical lithography only to define the local position of the transistors' gate electrodes, while the channel length was defined by very precise and accurate deposition and etching techniques. Unfortunately, only the channel length was in the sub-100 nm-region, the channel width was limited by the optical resolution. Now we developed a new method which enables to structure both – the channel width and channel length – by the deposition and etchback technique, so real "Nano-Transistors" – transistors with a channel length and a channel width down to 25 nm – can be fabricated without high demands to the used lithography.

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II. STRUCTURE DEFINITION PROCESS

Figure 1 shows the significant process steps for the definition of the MOS-transistor's active area, which defines the channel width of the transistor. First of all a pad-oxide is thermally grown and a nitride layer is deposited by LPCVD (Low Pressure Chemical Vapour Deposition) for the LOCOS technique (Local Oxidation of Silicon), similar as in the standard CMOS process. On top of these layers a sacrificial polysilicon layer is deposited and structured by conventional optical lithography (Figure 1a). The resolution of the applied lithography process is not important, because the resist mask only defines the local position of the transistor's channel area, but not the geometrical size (in this case channel width) of the transistor. The used etching process for the polysilicon layer is extremely anisotropic, because vertical sidewalls of this layer are important for the deposition and etchback technique. After the removal of the resist mask a TEOS-oxide layer is deposited conformally (Figure 1b) by LPCVD and etched back anisotropically in a special RIE-Process (Reactive Ion Etching) until a spacer surrounding the sacrificial oxide layer appears (Figure 1c). Only a very slight overetch is allowed for the etchback step, else the TEOS-nano-spacer would be reduced in its height in a non tolerable manner.

The next step is the removal of the sacrificial polysilicon layer in an SF_6-plasma with high selectivity to all other layers followed by the transfer of the TEOS-nanostructure into the nitride and oxide layer by a high anisotropic RIE-process (Figure 1d).

If the deposition process for the TEOS-oxide is absolutely conformal and the etchback process is ideal anisotropic, the linewidth is identical to the thickness of the prior deposited TEOS-oxide layer. However, if the real processes are not absolutely conformal respectively anisotropic, the linewidth is thinner but still reproducible and exactly determined by the TEOS-oxide thickness. With our equipment the linewidth of the TEOS-mask equals 0.9 times the TEOS-oxide thickness. The accuracy and homogeneity of the linewidth is due to the well controllable layer deposition and etchback techniques very high compared to other lithography techniques for such small structures.

To prevent the lateral oxidation under the nitride mask (birds beak), a nitride spacer is formed on the vertical sidewalls of the masking layers by deposition and etchback of a second nitride layer (Figure 1e). This complete structure is used as mask for the local field oxidation (Figure 1f). The width of the active area is defined by the thickness of the TEOS-oxide and by the thickness of the second nitride layer, not by any lithography. Due to the high accuracy of layer deposition techniques, sub-100 nm feature sizes with high precision and homogeneity are producible.

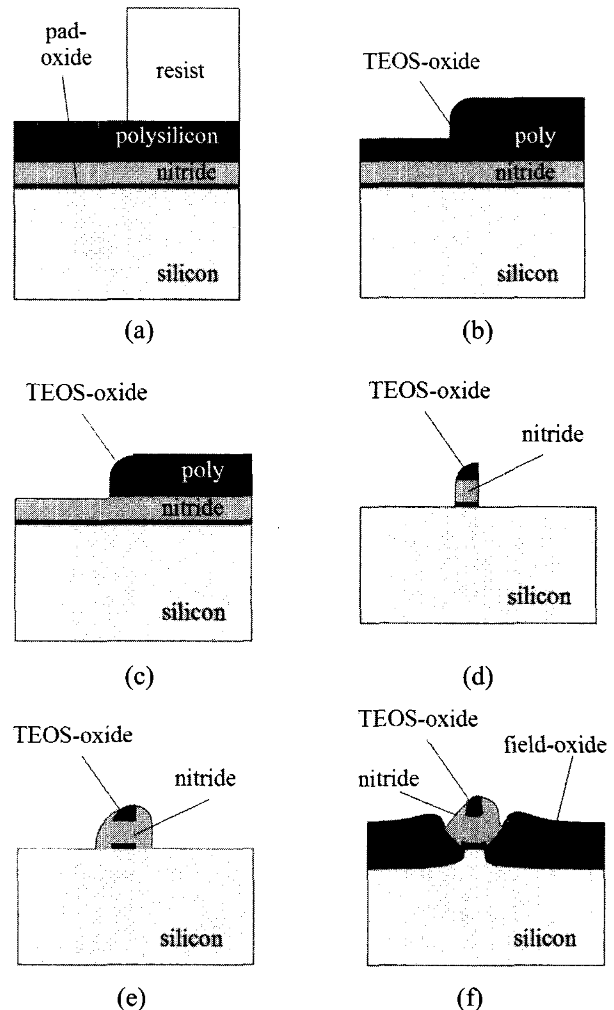

Fig. 1. Process steps of the deposition and etchback technique to define the transistor's channel width (simulation results).

To generate active area structures with standard dimensions, which are needed for larger transistors or for the contact regions of the Nano-Transistors, a resists mask is structured by normal lithography before the TEOS is etched back (this is not shown in the cross sections of Figure 1 and is done between the steps of Figure 1b and Figure 1c).

Figure 2 shows a SEM-photo (Scanning Electron Microscope) of the cross section after the local oxidation. In the center the active area – only 180 nm wide – surrounded by the field-oxide can be seen. The nitride layer for the masking during the local field oxidation is still on top of the active area.

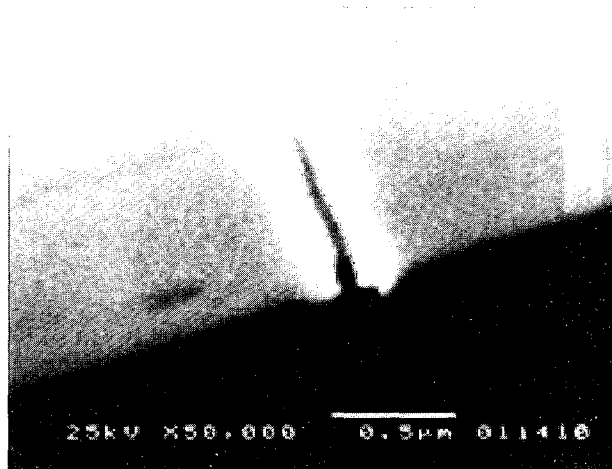

Fig. 2. Cross section of a 180 nm wide active area, fabricated with the modified deposition and etchback technique.

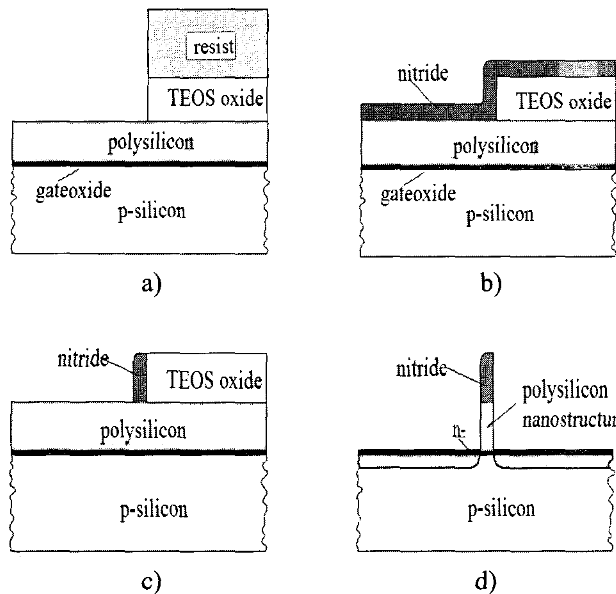

Fig. 3. Significant steps of the deposition and etchback technique for the gate definition.

We already presented the deposition and etchback technique for the polysilicon gate electrode before [2-4]. In this case TEOS-oxide is used as sacrificial layer and nitride is used as masking layer. With the materials of the first deposition and etchback technique masking of a polysilicon layer would not be possible.

Figure 3 presents the significant steps of that structure definition technique, which defines the channel length of the MOS transistor with sizes in the deep-sub-100 nm-region and high accuracy of the line width.

III. MEASUREMENT

Figure 4 shows a first transistor with a channel length of 200 nm and a channel width of 80 nm, manufactured by the enhanced depositions and etchback technique. The nano scaled active area is placed in the lower part of the picture. It could be seen as the thin horizontal line between the expanded contact regions for drain and source connections. The polysilicon gate electrode is surrounding the left row of contact holes and crosses the nanoline of the active area in the center of the picture.

Figure 5 presents the measured input and output characteristics of the manufactured nano scaled transistor. The transistor's threshold voltage is about V_{th}=1.2 V, peak transconductance is about $g_{m,max}$=0.195 μs at V_{DS}=0.1 V. It equals a peak transconductance of g_m/W=0.975 μs/μm standardized on the channel width.

The output characteristics shows the transistor's drain-source voltage between 0 and 5 V. The gate-source voltage is varied between 0 and 2.5 V with steps of 0.5 V. The drain-source voltage graphs for V_{GS}=0 V, 0.5 V and 1 V are overlaying each other. The transistor is punching by a drain-source voltage over V_{DS}=1 V.

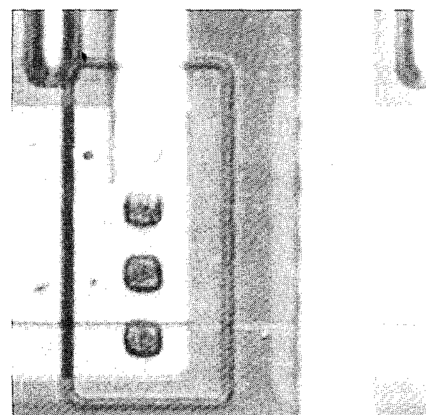

Fig. 4. Top view of a nano-transistor with W=200 nm and L=80 nm.

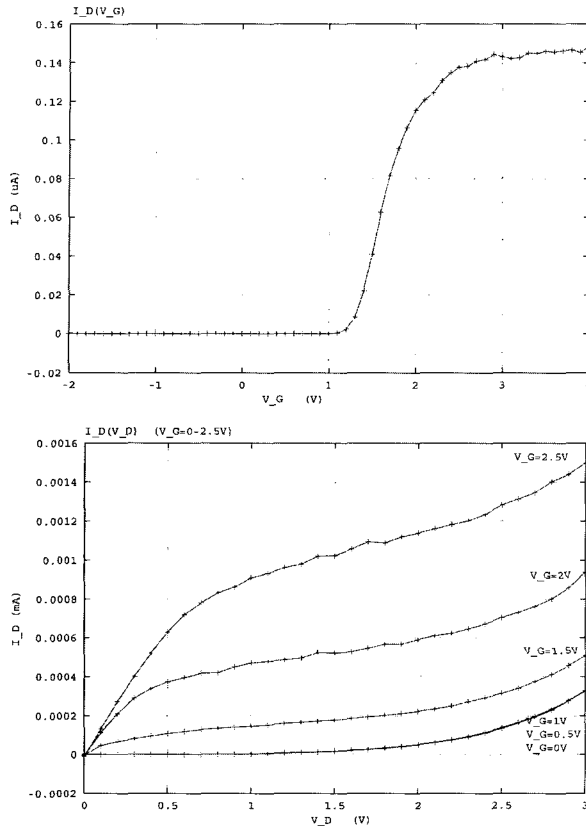

Fig. 5. Input and output characteristics of the transistor.

IV. Conclusion

A new fabrication technique for MOS-transistors, with dimensions in the deep sub-100 nm region for the channel length and channel width, has been presented in this paper. Main idea of this technique is to use optical lithography only to define the local placement of the transistor, while the channel length and width are both defined by deposition and by etching processes with a high precision in the sub-100 nm region. The new method is proved in a first MOS-transistor with a channel area of W/L=200 nm/80 nm. In future we will be able to manufacture transistors with channel width and length below 50 nm. Because of the new process results in an excellent homogeneity and reproducibility, it will be possible to make statistic analysis of behavior of deep nano scaled MOS-Transistors.

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Biography of the authors are not available at the time of publication