

# Flowable oxide CVD Process for Shallow Trench Isolation in Silicon Semiconductor

Sung-Woong Chung, Sang-Tae Ahn, Hyun-Chul Sohn, and Sang-Don Lee

**Abstract**—We have proposed a new shallow trench isolation (STI) process using flowable oxide (F-oxide) chemical vapor deposition (CVD) for DRAM application and it was successfully developed. The combination of F-oxide CVD and HDP CVD is thought to be the superior STI gap-filling process for next generation DRAM fabrication because F-oxide not only improves STI gap-filling capability, but also the reduced local stress by F-oxide in narrow trenches leads to decrease in junction leakage and gate induced drain leakage (GIDL) current. Finally, this process increased data retention time of DRAM compared to HDP STI. However, a serious failure occurred by symphonizing its structural dependency of deposited thickness with poor resistance against HF chemicals. It could be suppressed by reducing the flow time during F-oxide deposition. It was investigated collectively in terms of device yield. In conclusion, the combination of F-oxide and HDP oxide is the very promising technology for STI gap filling process of sub-100nm DRAM technology.

## I. INTRODUCTION

Most of processes are confronted by challenge due to rapid decrease in design rule. The gap-fill process is one of them. Especially the structure of STI could be restricted by gap-fill limitation of High-density plasma

(HDP) CVD, such as trench depth, trench sidewall dielectrics and active width. To resolve this restriction, we have developed a new STI process using flowable oxide (F-oxide) chemical vapor deposition (CVD) for DRAM application [1]. Since the F-oxide has the fluid characteristics similar to a spin-on-glass film at the moment of deposition, it shows excellent gap filling capability. However, the nano-pores generated in narrow trenches during densification annealing make F-oxide to be susceptible to a severe cleaning condition. The dense HDP oxide over the F-oxide can prevent the exposure of nano-pores to cleaning chemicals.

**Table 1.** Deposition conditions of flowable oxide.

conditions	a	b	c	d	e
thickness (Å)	150	220	280	150	220
in-situ flow	O	O	O	X	X

It has been known that junction leakage has a strong relationship with stress at the interface of Si and field oxide [1-3]. T. Kuroi et al. reported that crystal defects were generated by local stress and the stress increased with the reduction in the isolation pitch [4]. Therefore, the minimization of the local stress is one of the key solutions to suppress junction leakage at the sub-100nm technology. Fortunately, the F-oxide exhibits less thermal mismatch with Si compared to HDP oxide. Therefore, it is expected that the local stress around field oxide can be released. In this paper, the effect of the addition of F-oxide on the junction leakage and the data retention time was investigated.

However, since F-oxide in narrow trench is porous, there was an uncertainty about a serious failure as ever.

Manuscript received JANUARY 12, 2004; revised MARCH 11, 2004.  
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The main point is to understand the deposition behavior of F-oxide. In this work, we investigated the effect of deposition profile on the device characteristics and DRAM chip yield. And we discussed the feasibility of F-oxide CVD as STI process for sub-70nm technology.

## II. EXPERIMENTAL

The F-oxide CVD process is the method depositing liquid  $\text{Si}(\text{OH})_4$  film like gel by supplying silane and hydrogen peroxide gases at the temperature of about  $0^\circ\text{C}$ . The subsequent densification annealing was performed in  $\text{N}_2$  furnace at  $1050^\circ\text{C}$ . Since deposited film has the behavior like liquid, the surface should be modified into the hydrophilic surface before deposition. And then HDP oxide was deposited over the F-oxide. The thermal expansion coefficient and the intrinsic stress of F-oxide were obtained by measuring the stress hysteresis and the local stress near a trench was estimated through simulation using TSUPREM-4. DRAM cell array with 100nm-design rule was used for the evaluation of isolation characteristics with a F-oxide layer and a thin nitride film. The 256-Mbits SDRAM with 130nm-design rule was also used to investigate the device performance such as hot carrier immunity, gate induced drain leakage and data retention time when F-oxide CVD was applied. Finally, 256Mbits DRAM chip yield was used to search for integration issues and then the failure type was classified.

## III. RESULTS AND DISCUSSION

Even though the F-oxide is deposited by low pressure CVD, it shows the fluid characteristics like water. The deposition profile of F-oxide depends on sizes and densities of patterns due to the surface tension of  $\text{Si}(\text{OH})_4$ . Fig. 1 shows the deposition profile of F-oxide at a wide field. As it is far from active region, the thickness of F-oxide was reduced. Fig. 2 shows the deposition profiles of F-oxide in the cell array. The F-oxide in the narrower trench was much thicker than that in wide trench. Since the  $\text{Si}(\text{OH})_4$  has high surface energy, it was thought that F-oxide becomes thicker at

the bottom of trench as the trench space decreases in order to reduce exposed surface area. It can be explained by capillary phenomena of  $\text{Si}(\text{OH})_4$  phase. Due to this, F-oxide is useful for the reduction in aspect ratio of narrow trench. As expected from results of Fig. 2, followed HDP CVD could fill even the trench as narrow as even 60nm trench space.

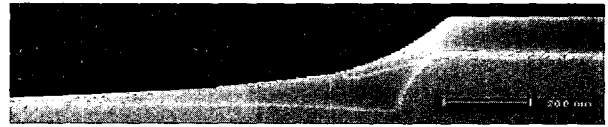


Fig. 1. Profile of flowable oxide deposited near wide isolation region.

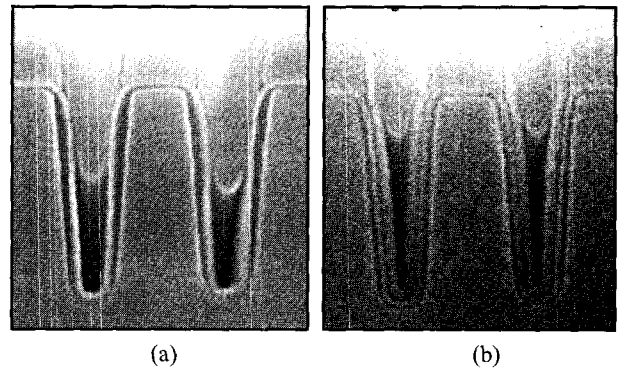
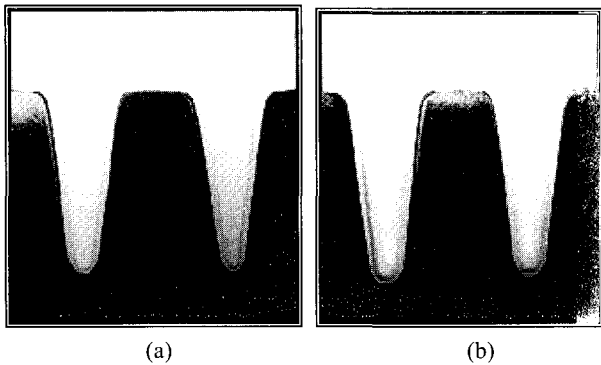


Fig. 2. Cross-sectional SEM photographs exhibiting deposition profiles of flowable oxide. They were observed in DRAM cell array with (a) 80nm opening space and (b) 60nm opening space.

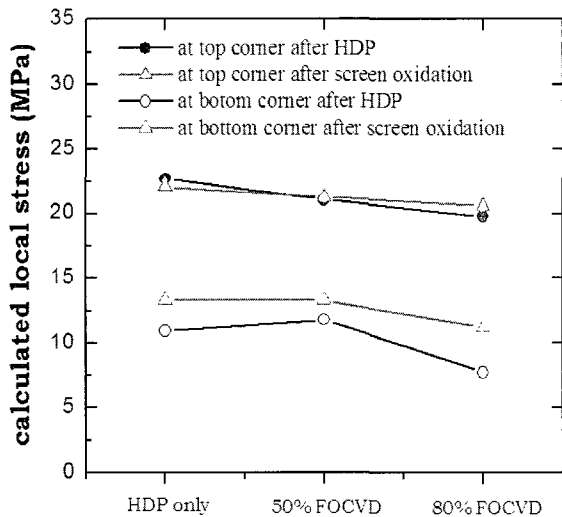
Moat depth was measured using SEM and TEM, in order to examine that very thin F-oxide at the trench sidewall could make the moat deeper after chemical cleaning. Fig. 3 shows TEM cross-sectional photographs for HDP STI and F-oxide STI. Any chemical attack on F-oxide layer at the trench sidewall could not be observed. Some voids were observed at the bottom of trenches in the F-oxide STI from TEM photographs. However, they were confirmed to be nano-pores exaggerated during preparation of TEM sample.

Fig. 4 shows the local stresses related to F-oxide thickness in narrow trenches. Stress simulation provided the estimated values of local stresses at the top and the bottom corners of trenches. The local stress decreased with F-oxide thickness. Even though they were calculated by using the thermal expansion coefficient obtained from the flat film, the F-oxide layer was effective to reduce the local stress. Considering that the F-oxide inside narrow gap is more porous, it was

expected that the local stress could be more effectively suppressed in narrow trenches.



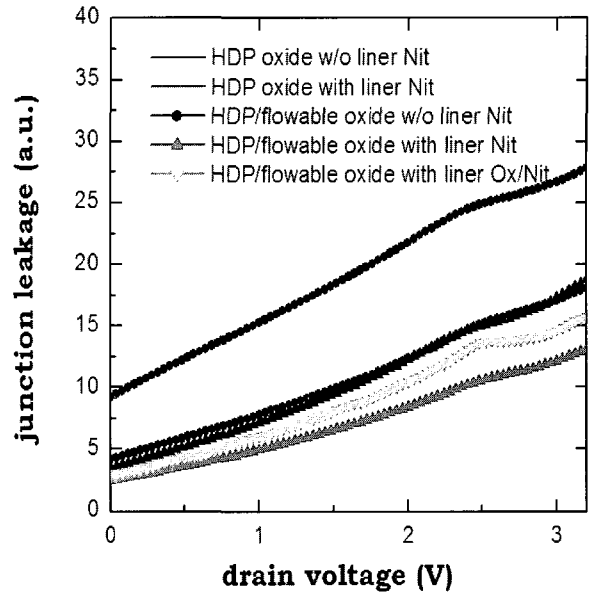
**Fig. 3.** TEM photographs of STI filled by (a) HDP CVD and (b) the flowable oxide CVD. The samples were prepared after gate electrode deposition. The moat depths and trench profiles of two processes were similar.



**Fig. 4.** The simulated local stress as a function of flowable oxide thickness in narrow trenches. The critical points with peak stress are located at the top and bottom trench corners.

Fig. 5 shows the p-n junction leakage measured with 256-kbit cell arrays of 100nm-scaled DRAM. The F-oxide STI provided the improved junction leakage characteristics compared to the conventional HDP STI. Considering that HDP STI with thin liner nitride was comparable with F-oxide STI without thin liner nitride, the effect of stress relaxation originated from the use of the F-oxide was similar to the application of liner nitride into HDP STI. By the insertion of thin nitride film into the F-oxide STI, the additional reduction in junction leakage was obtained. The junction leakage current of HDP STI could be reduced as much as 3 times by the

introduction of F-oxide layer or liner nitride. Therefore, it was evident that the buffer layer such as F-oxide or thin nitride film could suppress the generation of interface traps near the trench.

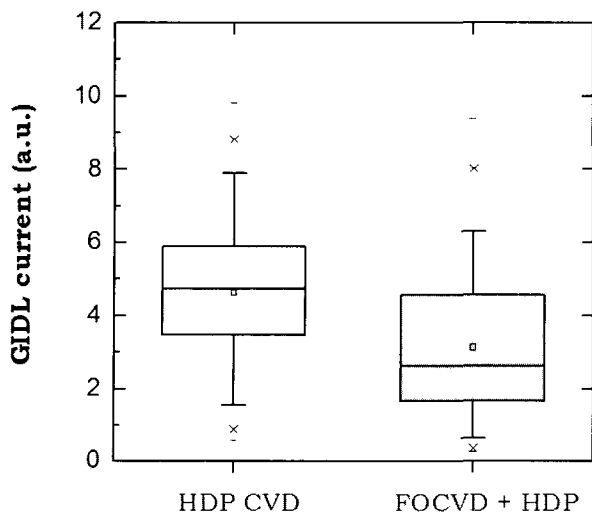


**Fig. 5.** The p-n junction leakage curves measured in 100nm-scaled 256-kbit cell arrays. The junction leakage generated by STI with the flowable oxide was suppressed when compared with the HDP STI.

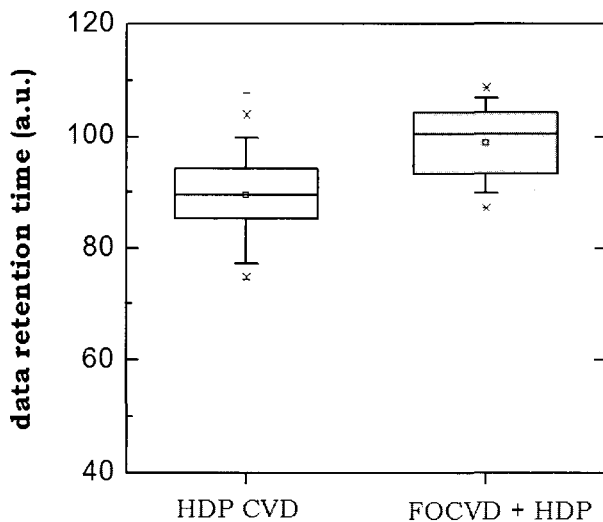
The reliability of 130nm-scaled 256Mbit DRAM using F-oxide STI was examined. In this experiment, thin nitride liner was used in both of HDP STI and F-oxide STI. Fig. 6 shows the gate induced drain leakage (GIDL) current, which is generally known as the major source of degradation of refresh characteristics of DRAM. The reduced GIDL current was obtained by using the F-oxide. It is clear that the introduction of F-oxide CVD into STI process contributes to the reduction of junction leakage of cell transistor. And the improvement of leakage performance would be resulted from buffering of local stress.

Fig. 7 shows the refresh characteristics of 256-Mbits DRAM. The data retention time is exhibited at  $10^{-4}\%$  cumulative failure. The data retention time of DRAM cells using F-oxide as gap-fill materials was improved by about 10% compared with conventional HDP while there were no differences in cell capacitance and threshold voltage of cell transistor. Based on these results, we concluded that there is considerable stress relaxation effect of F-oxide process on the reduction in the cell

junction leakage and GIDL current. And it led to the improvement of refresh performance.

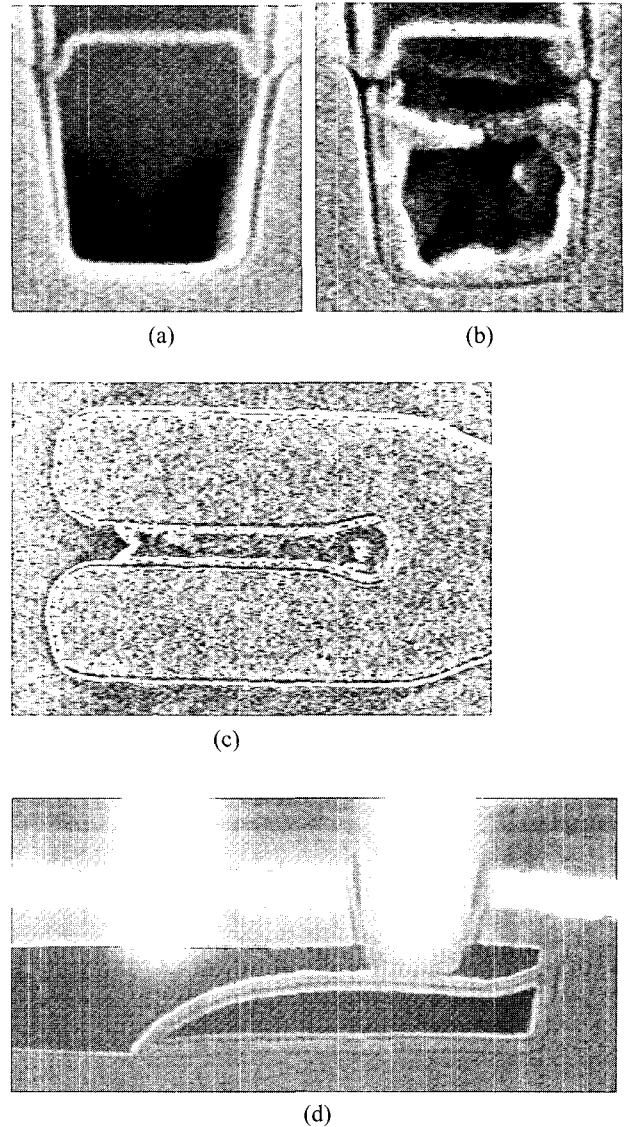


**Fig. 6.** Gate-induced drain leakage (GIDL) current values measured in 80-kbit cell arrays with 130nm minimum feature size. The voltage between drain and source is 6V and the gate voltage was grounded.



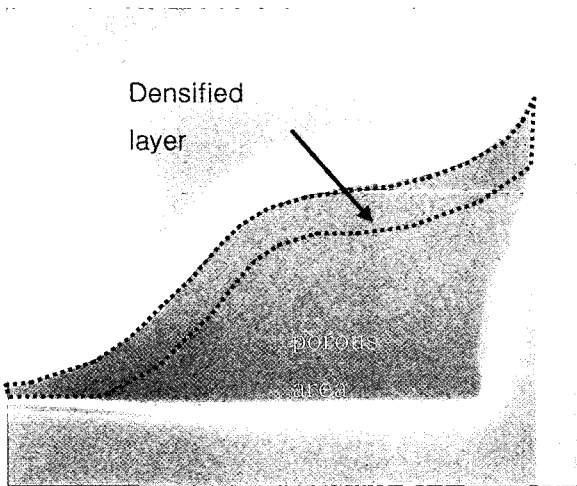
**Fig. 7.** The data retention time values measured in 256-Mbits DRAM. The time was obtained at 10-4% cumulative failure.

As mentioned above, F-oxide serves some advantages such as gap-filling capability and refreshes characteristics. However, serious damage of F-oxide was observed at specific pattern. Fig. 8 shows SEM pictures for serious damage region. Gate residues were observed at the abnormal

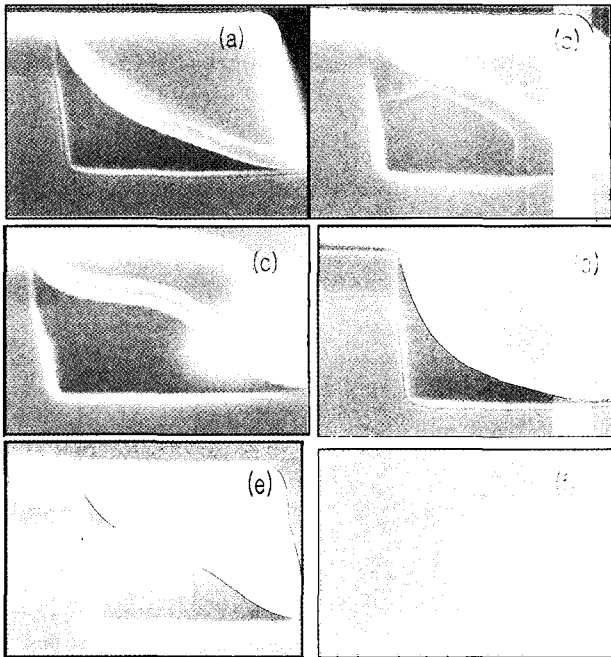


**Fig. 8.** SEM pictures explaining dc failure mechanism. Gate electrode was deposited through chemical attacked area and that should induce the dc failure. (a) normal isolation profile (b) abnormal isolation profile (c) plane view of abnormal isolation region (d) cross-sectional view of abnormal isolation region.

region. Gate materials were found in the isolation oxide in failure chip differently from normal structure. It was thought because HF chemical attack made the hollow area near the trench. Hence some contacts could be connected with this abnormal gate electrode. Fig. 9 shows the failure mechanism described by the characteristics of the F-oxide. Succeeding annealing process densifies the only surface region of F-oxide. The porous area below the dense layer should avoid exposing in the HF solutions.



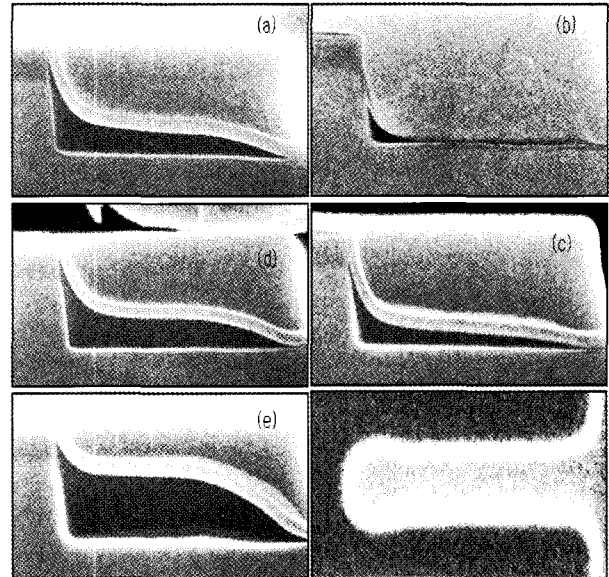
**Fig. 9.** Diagram showing the chemical attack from HF solutions. White line represents active Si surface that will be exposed after following integration processes.



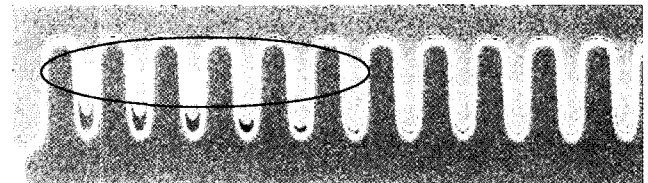
**Fig. 10.** The deposition profiles of F-oxide at the short U-shaped pattern. (a), (b), (c) additional flow step and (d), (e) skipped in-situ flow. (f) plane view of short U-shaped pattern.

In order to solve the above issue, it was thought to be very important to understand flow characteristics of F-oxide. TABLE I shows the deposition conditions about thickness of F-oxide and in-situ flow. Fig. 10 shows the deposition profiles of F-oxide at the short U-shaped patterns. The thickness at the pattern dramatically increased as the thickness on the flat wafer increased. It was obtained the F-oxide deposited with suppressed flow condition was thinner. Fig. 11 shows the deposition profiles of F-oxide

at the long U-shaped pattern. Since F-oxide could move as far as micron order, F-oxide near the narrow pattern would pile up. It was found the F-oxide at the pattern was thinner in the case of suppressed flow condition in spite of same thickness.



**Fig. 11.** The deposition profiles of flowable oxide at the long U-shaped pattern. (a), (b), (c) additional flow step and (d), (e) skip in-situ flow. (f) plane view of short U-shaped pattern.



**Fig. 12.** SEM photograph of HF chemical damaged area. It was inspected after removal of sacrificial thermal oxide for the control of threshold voltage.

Fig. 12 shows the SEM plane view of chemical attacked area. The circled part indicates the region etched by HF solutions. Fig. 13 shows device yield and dc failure rate with several conditions of F-oxide deposition. The yields of three groups were comparable to that of HDP CVD group, but the other one group showed significant drop of yield. The major cause of the yield drop was dc failure.

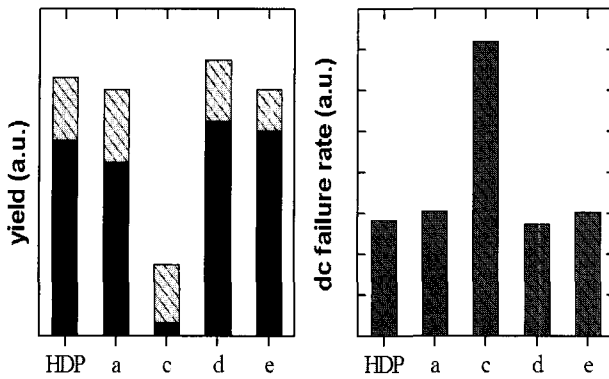


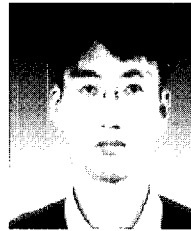
Fig. 13. (a) 256 Mbit SDRAM chip yield and (b) dc failure rate with related to deposition condition.

#### IV. CONCLUSIONS

The new STI process using the combination of F-oxide CVD and HDP CVD was successfully developed for nano-scaled DRAM technology. The gap filling capability was startlingly improved and it could be very easily obtained even though the only F-oxide CVD was added into conventional process with HDP CVD. The new STI process using F-oxide CVD was successfully proved using the productive 130nm DRAM device. Moreover, its low thermal mismatch from Si resulted in the improvement of the device performance such as junction leakage and data retention time. In conclusion, F-oxide did not cause any issue except for dc failure in worse cases. However, controlling the deposition profile of F-oxide could easily solve dc failure. Therefore, F-oxide STI process was believed to be the promising candidate for new STI process of 70-nm scaled technology.

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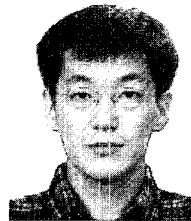
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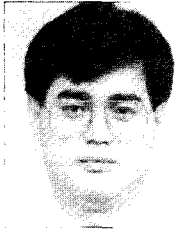
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