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Hydrogenated a-Si TFT Using Ferroelectrics

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요 약

강유전체($SrTiO_3$) 박막을 게이트 절연층으로 하여 수소화 된 비정질 실리콘 박막 트랜지스터를 유리 기판 위에 제조하였다. 강유전체는 기존의 SiO_2, SiN 등과 같은 게이트 절연체에 비하여 유전특성이 매우 뛰어나 TFT의 ON 전류를 증가시키고 문턱전압을 낮추며 항복특성을 개선하여 준다. PECVD에 의하여 증착된 a-Si:H는 FTIR 측정 결과 2,000 cm^{-1}과 635 cm^{-1} 및 876 cm^{-1}에서 흡수 밴드가 나타났으며, 2,000 cm^{-1}과 635 cm^{-1}은 SiH_1의 stretching과 rocking 모드에 기인한 것이며 876 cm^{-1}의 weak 밴드는 SiH_2 vibration 모드에 의한 것이다. a-SiN:H는 optical bandgap이 2.61 eV이고 굴절률은 1.8~2.0, 저항률은 10^{11}~10^{15} Ω-cm 정도로 실험 조건에 따라 약간 다르게 나타난다. 강유전체($SrTiO_3$) 박막의 유전상수는 60~100 정도이고 항복전계는 1MV/cm 이상으로 우수한 절연특성을 갖고 있다. 강유전체를 이용한 TFT의 채널 길이는 8~20 μm, 채널 넓이는 80~200 μm로서 드레인 전류가 게이트 전압 20V에서 3.4 μA이고 I_{on}/I_{off} 비는 10^5~10^8, V_{th}는 4~5 volts이다.

ABSTRACT

In this paper, the a-Si:H TFT using ferroelectric of $SrTiO_3$ as a gate insulator is fabricated on glass. High k gate dielectric is required for on-current, threshold voltage and breakdown characteristics of TFT. Dielectric characteristics of ferroelectric are superior to SiO_2 and Si_3N_4. Ferroelectric increases on-current and decreases threshold voltage of TFT and also can improve breakdown characteristics. $SrTiO_3$ thin film is deposited by e-beam evaporation. Deposited films are annealed for 1 hour in N2 ambient at 150℃ ~ 600℃. Dielectric constant of ferroelectric is about 60~100 and breakdown field is about 1MV/cm. In this paper, the TFT using ferroelectric consisted of double layer gate insulator to minimize the leakage current. a-SiN:H, a-Si:H (n-type a-Si:H) are deposited onto $SrTiO_3$ film to make MFNS(Metal/ferroelectric/a-SiN:H/a-Si:H) by PECVD. In this paper, TFT using ferroelectric has channel length of 8 ~ 20 μm and channel width of 80 ~ 200 μm. And it shows that drain current is 3.4μA at 20 gate voltage, I_{on}/I_{off} is a ratio of 10^5 ~ 10^8 and V_{th} is 4 ~ 5 volts, respectively. In the case of TFT without having ferroelectric, it indicates that the drain current is 1.5 μA at 20 gate voltage and V_{th} is 5 ~ 6 volts. If properties of the ferroelectric thin film are improved, the performance of TFT using this ferroelectric thin film can be advanced.

키워드

a-Si:H Thin Film Transistor, Ferroelctric ($SrTiO_3$), Double Layer Gate Insulator

Ⅰ. Introduction

Today, amorphous silicon is widely used in optical to electrical conversion device and wide area film device. Especially, it is used such as a switching device for active matrix LCD, contact

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image sensor for a-Si:H TFT and Fax, and a-Si:H solar cell. Usually, amorphous silicon TFT uses a-SiN:H as a gate insulator [1],[2]. Induced dielectric constant of a-SiN:H is 7.5. To increase a driving current of TFT, an insulator with a large of induced dielectric constant is needed. Recently, much works have advanced on TFT gate insulating layer. High k gate dielectrics are required for a-Si:H TFT structure because the conventional a-SiN:H film is too thin to minimize the threshold voltage and the leakage current. A thick layer can be used with the high k material to lower the parasitic capacitance between the gate and the source (and drain). A thick layer is used to prevent the top-to-bottom metal shortage, which is a killing factor for the yield. The high k dielectric material is usually used in combination with a high quality dielectric interface layer to lower the interface density of states. Ferroelectric thin film is suitable as gate insulator because of large dielectric constant. In this paper, we have fabricated a-Si:H TFT using gate insulator with ferrodielectric and compared their electrical characteristics with gate insulator a-SiN:H TFT used as commonly.

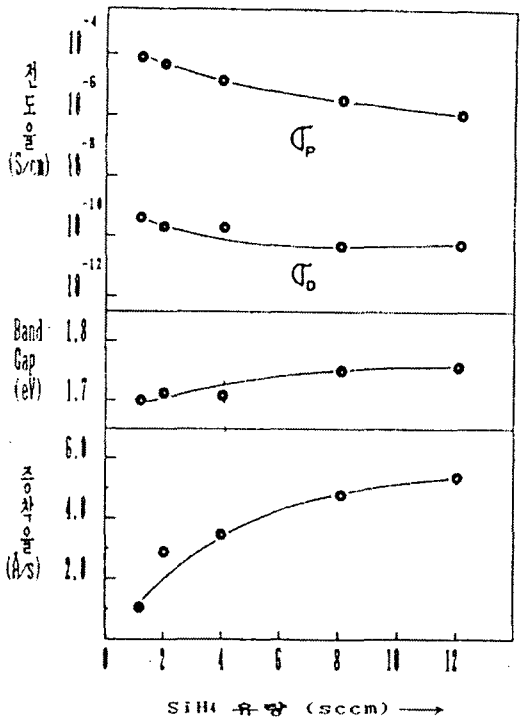


그림 1. a-Si:H의 전기 광학적 특성
Fig 1. Electrical and optical characteristics of a-Si:H (a-Si:H properties as SiH_4 flow rate).

II. Fabrication and Characteristics of Thin Films

Amorphous silicon is deposited using plasma enhanced chemical vapor deposition (PECVD). At this time, electrical and optical characteristics of amorphous silicon such as conductivity, optical band gap and deposition rate are changed under deposition condition such as SiH_4, flux, chamber pressure, RF power and substrate temperature. Figure 1 shows the characteristics of experimental results according to amorphous deposition condition. From the results shown in Figure 1, photo and dark conductivity are diminished according to SiH_4 flux, dark conductivity is changed 10^{-9} ~ 10^{-11}(S/cm), in the case of photo conductivity is varied range from 10^{-4} to 10^{-6} (S/cm). Also, optical band gap shows 1.7 ~ 1.8eV, as a flux of SiH_4 is increased, it is deposited from 1.0 to 6.9 (Å/sec). As shown in Figure 1, we can estimate the trade-off relation between conductivity and optical band gap according to a flux of SiH_4 and control the optical band gap by adjusting a flux of SiH_4. But, the change of conductivityand optical band gap is little according to chamber pressure condition. The deposition rate is ranged from 1.0 to 3.0 (Å/sec). Also, the change of electrical and optical characteristics is a little according to RF power. Figure 2 shows the IR spectrum result. It represents a relation between Si of a hydrogenated amorphous silicon film and bonding of H. Frequency of fundamental infrared absorption modes depends on a mass of oscillation dipole and amount of bond between elements including dipole. The a-Si:H film shows a type of vibration mode, it shows SiH_4 stretching mode at wave number 2000 cm^{-1}. Also, it represents a rocking mode at wave number 635 cm^{-1}. The bond represented at weaker bond range 800 ~ 900 cm^{-1} depends on the vibrational mode of SiH_2. Therefore, the fabricated a-SiH film in this experimental setup shows that Si-H

bonding of stretching/rocking mode exists [3],[4]. The gate insulator layer and a-SiN:H film of passivation film are fabricated using PECVD by mixing SiH_4 gas and NH_3 gas. Etching rate of a-SiN:H increases and refraction diminishes as NH_3/SiH_4 increases. Also, their characteristics are not related with RF power. The Eopt value is around 2.4 Ev [5],[6].

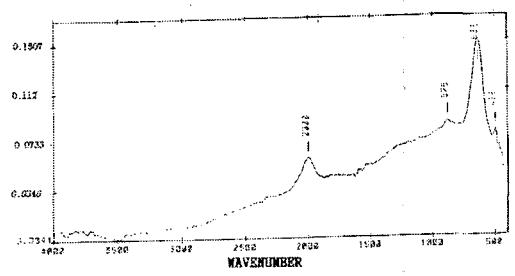


그림 2. a-Si:H의 FTIR 특성
Fig 2. FTIR characteristics of a-Si:H.

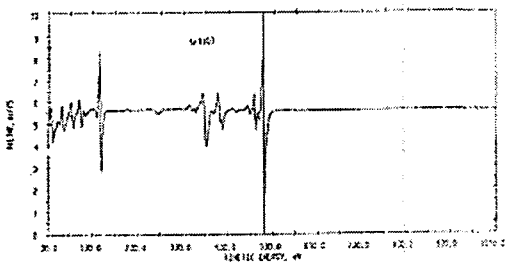


그림 3. $SrTiO_3$ 박막의 X-RD 측정
Fig. 3. X-RD analysis of $SrTiO_3$ thin film.

Ferroelectrics ($SrTiO_3$) film is fabricated by E-beam evaporator. Figure 3 shows X-RD analysis of $SrTiO_3$. The used ferroelectrics target forms ceramic type with high pressed PELLET. Dielectric constant of ferroelectric thin film is 60 ~ 100 and has high value compared with another insulator. It has a high breakdown field about 1 MV and an excellent characteristic as an insulator. Figure 4 shows dielectric constant and breakdown field of ferroelectrics ($SrTiO_3$) as annealing temperature.

III. Characteristics and Structure of Thin Film Transistor

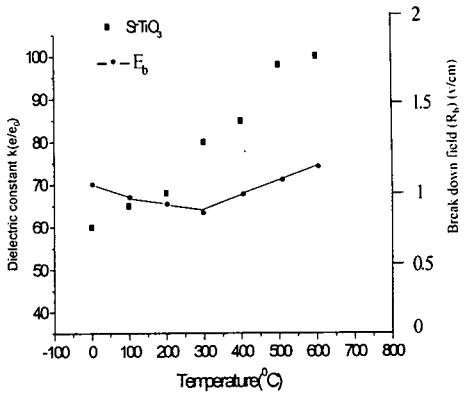


그림 4. 강유전체의 유전상수와 항복 특성
Fig 4. Dielectric constant and breakdown field of ferroelectrics ($SrTiO_3$) as annealing temperature.

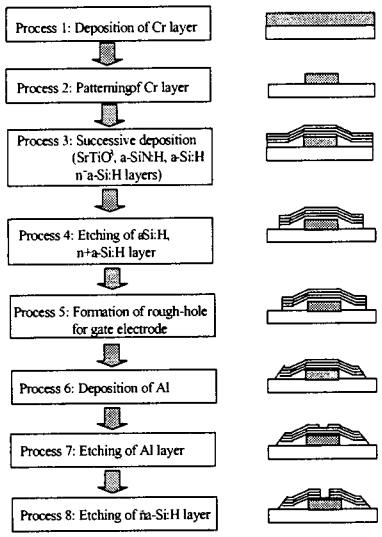


그림 5. a-Si:H TFT의 제조공정
Fig 5. Fabrication process of a-Si:H TFT.

Figure 5 shows a cross-section and fabrication process of thin film transistor fabricated in this experimental setup. Figure 6 shows microscope picture of a-Si:H TFT. The gate electrode is formed by patterning with length of 8 μm~16 μm and width of 80~200 μm after depositing with gate electrode (Cr) 1000 Å under corning 7059 glass substrate. We have fabricated a-SiN:H, a-Si:H and n^+a-Si:H samples on gate electrode in sequence and ferroelectric ($SrTiO_3$), a-Si:H and n^+a-Si:H samples, respectively. The thickness of these thin films is formed with $SrTiO_3$ (2000 Å),

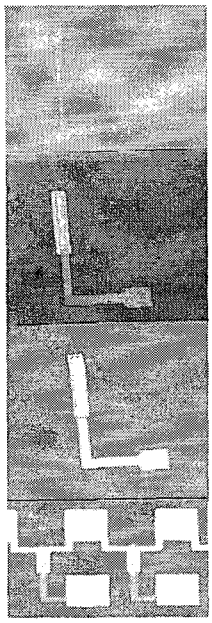


그림 6. a-Si:H TFT의 공정별 현미경 사진
Fig 6. Microscope picture of a-Si:H TFT.

a-SiN:H (3000 Å), a-Si:H(2000 Å) and n^+a-Si:H (500 Å). We have used a RIE (Reactive Ion Etching) method to etch after forming a-Si:H pattern of channel layer. RIE equipment is used RI mode of PECVD. After hole pattern is formed, a-Si:N:H is conducted RIE and the used gas is used by mixing CHF_3 and O_3. Ferroelectric ($SrTiO_3$) is mixed with HF:DI at a rate of 1:5 and etched by dipping with 17 seconds. To form a source drain electrode, the film is patterned after depositioning 4000 Å of Al by

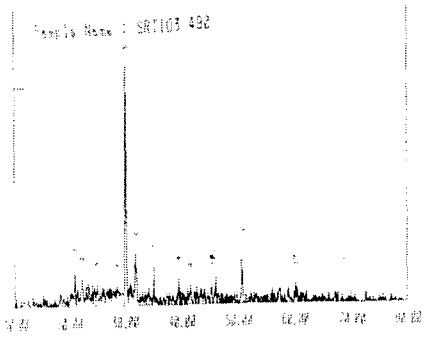


그림 7. 강유전체의 X-RD
Fig 7. X-RD analysis of ferroelectrics ($SrTiO_3$).

E-beam evaporator. Finally, n^+a-Si:H is conducted by RIE using CF + O_2 and gas for S/D metal pattern. To compensate a damage by RIE process, the n^+a-Si:H is annealed at temperature 200 ℃ in vacuum state. To test characteristics of fabricated sample, we have gained an I-V, V_{th} and I_{on}/I_{off} characteristics by using probe station and HP4145B parameter analyzer. Figure 7 shows X-RD analysis of ferroelectrics($SrTiO_3$). Figure 8 shows SEM picture of a-Si:H TFT.

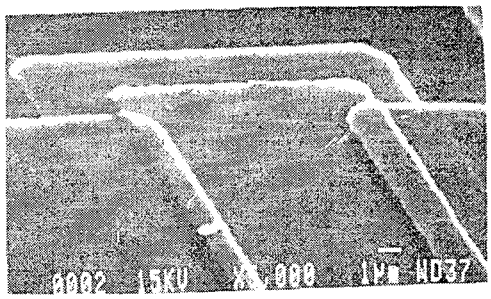
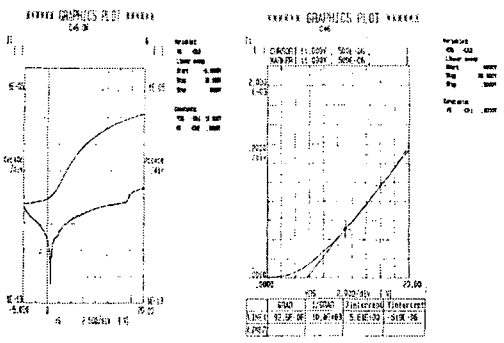
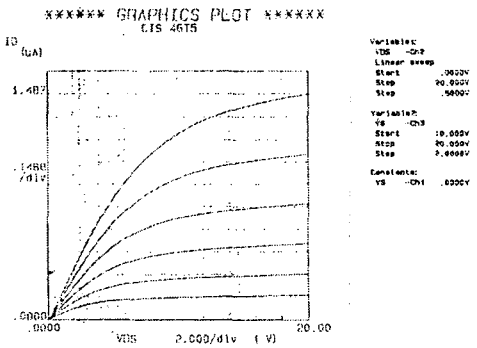


그림 8 a-Si:H TFT의 SEM 사진
Fig 8. SEM picture of a-Si:H TFT.

We have annealed for 1 hour at a temperature 200 ℃ to compensate damage by RIE process. To measure the electrical characteristics of the fabricated samples, we obtained characteristics of I-V, V_{th} and I_{on}/I_{off} by using probe station and 4145A parameter measurement equipment. As shown in Figure 9, the saturation current at gate voltage 20 volts without having ferroelectric TFT is 1.4 μA, I_{on}/I_{off} is 10^3 and V_{th} is 5.6 volts. In the case of TFT with ferroelectric gate insulator layer as shown in Figure 10, saturation current at gate voltage 20 volts is 3.4μA, V_{th} is 4.5 volts and I_{on}/I_{off} gives a values range from 10^5 to 10^6. We have estimated that the leakage current of TFT with ferroelectric layer is smaller than that of without ferroelectric layer. That is to say, the V_{th} of the TFT with two layers using ferroelectric and a-SiN:H compared with TFT of gate insulator with a-SiN:H layer shows a small value and has 1 volts. I_{on}/I_{off} has 10^2 ~ 10^3 order value. Its I-V current has a 1.5μA times in the same gate and drain volts. From the results, we can estimate that the ferroelectric layer employing two layers gate insulator has good quality insulator characteristics. It enhanced good elec-



(a) I_{on}/I_{off} ratio (b) Threshold voltage (V_{th})



(c) I-V curve

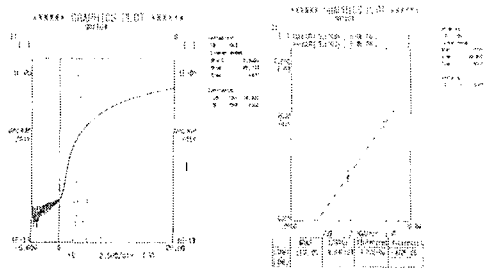
그림 9. a-Si:H TFT의 전기적 특성

Fig 9. Electrical Characteristics of a Si:H TFT Without Ferroelectric.

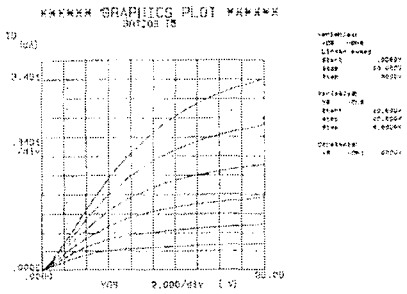
trical characteristics. Also, the leakage current can be diminished using two layers insulator.

IV. Conclusions

From the experimental results, the TFT with ferroelectric has a higher value of I_{on}/I_{off} compared with TFT having a gate insulator employing a-SiN:H. In the case of I_{off} current, leakage current between source and gate by using two layers gate insulator ($SrTiO_3$/a-SiN:H) reduces, pin hole employing gate insulator with one layer is more larger than two layer gate insulator. The probability of generation of pinhole by using two layer is more smaller. Also, I_{on} current increases as dielectric constant of gate insulator increases. This effect gives the increase of I_{on}/I_{off}. As dielectric constant increases, V_{th} get smaller 1 volts value. The channel is formed in



(a) I_{on}/I_{off} ratio (b) Threshold voltage (V_{th})



(c) I-V curve

그림 10. a-Si:H TFT의 전기적 특성

Fig 10. Electrical Characteristics of a Si:H TFT With Ferroelectric.

small gate voltage. From the I-V curve, we can estimate that drain current of TFT with $SrTiO_3$ at same gate voltage increases over 1.5 μA. And, leakage current between gate and source is much smaller. Under the voltage stress condition, TFT with ferroelectric compared to thin film has no influence on the voltage stress condition. From the results, we can estimate that TFT with ferroelectric has no interface trap. These phenomena give good results. Ferroelectric thin film can be applicable to TFT application such as HDTV display device.

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저자소개

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