Quantitative Analysis on Voltage Schemes for Reliable Operations of a Floating Gate Type Double Gate Nonvolatile Memory Cell

Seongjae Cho, Il Han Park, Tae Hun Kim, Jung Hoon Lee, Jong Duk Lee, Hyungcheol Shin, and Byung-Gook Park

***Abstract*—Recently, a novel multi-bit nonvolatile memory based on double gate (DG) MOSFET is proposed to overcome the short channel effects and to increase the memory density. We need more complex voltage schemes for DG MOSFET devices. In view of peripheral circuits driving memory cells, one should consider various voltage sources used for several operations. It is one of the key issues to minimize the number of voltage sources. This criterion needs more caution in considering a DG nonvolatile memory cell that inevitably requires more number of events for voltage sources. Therefore figuring out the permissible range of operating bias should be preceded for reliable operation. We found that reliable operation largely depends on the depletion conditions of the silicon channel according to charge amount stored in the floating gates and the negative control gate voltages applied for read operation. We used Silvaco Atlas, a 2-D numerical simulation tool as the device simulator.**

***Index Terms*—Multi-bit nonvolatile memory, double gate MOSFET, depletion condition, charge amount, negative control gate voltages**

I. INTRODUCTION

Double gate nonvolatile memory cell is considered as a good candidate for high density integration [1]. The operation of a nonvolatile memory cell needs more voltage sources compared to that of conventional MOSFET device depending on cases such as program, erase, and read operations. It cannot be overemphasized that the number of voltages fed into terminals should be as minimized as possible. More number of voltage sources mean more circuits that should be implemented and this problem challenges engineering economics. But prior to considering the economics, functional reviews on the voltage schemes must be taken into account in detail. In this paper, quantitative analysis on those voltage schemes are performed for reliable operations of a double gate MOSFET nonvolatile memory device focusing on gate voltage effects in program and read operations.

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II. DEVICES STRUCTURE

Figure 1 shows the bird's eye view structure of the floating gate type double gate nonvolatile memory cell. The gate length of the device is 70 nm, and the thickness of tunneling oxide is 7 nm for sufficient data retention. The doping concentration of p-type silicon channel is 1×10^{18} cm^{-3} and the inter-poly dielectric layers between control and floating gates are composed of oxide-nitride-oxide triple layers.

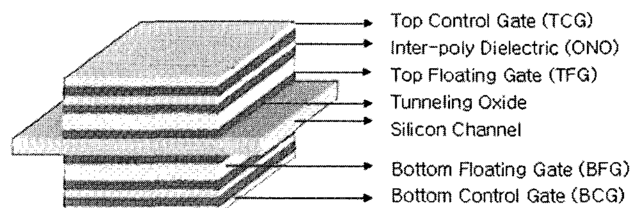


Fig. 1. Floating Gate Type DG MOSFET NVM cell.

This structure was intended for NOR type memory cell, which means the program operation is based on channel hot electron injection (CHEI) mechanism. In the short channel regime under 100 nm, the electrons cannot be easily accelerated along the channel. But channel electrons with insufficient kinetic energies can overcome the oxide energy barrier more easily aided by negative biases on the bottom control gate (BCG) with smaller positive voltage on the top control gate (TCG) [2]-[3]. This program operation based on channel initiated secondary electron injection (CHISEL) had been kept through the simulation work consistently. The quantitative analysis were conducted by Silvaco Atlas, a 2-D numerical device simulator [4]. We read the information stored in the top floating gate (TFG), which means the TCG was swept and the BCG was biased to check the information. The reverse situation is possible analogously if we need to read the information on the BFG, but we only consider a single case for convenience. This explanation is valid throughout the paper.

III. Results and Discussions

1. Variation in the Number of Channel Electrons after Program Operations

The negative bias on the bottom control gate is necessary for programming operation but the magnitude of the voltage should not be larger than some upper limit. Excessively negative voltage degrades the injection of channel electrons into the top floating gate. Figure 2 shows such a relation between negative voltage on BCG and the

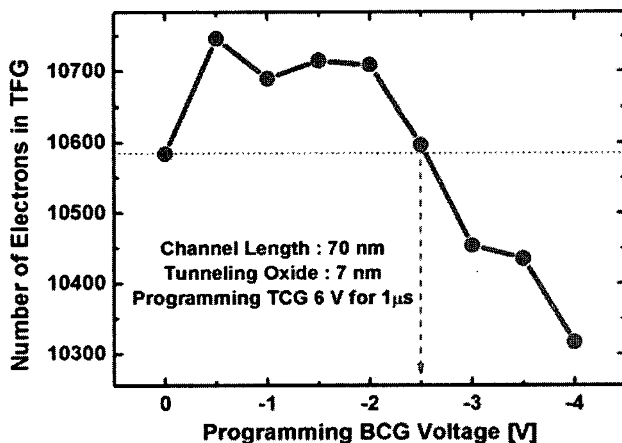
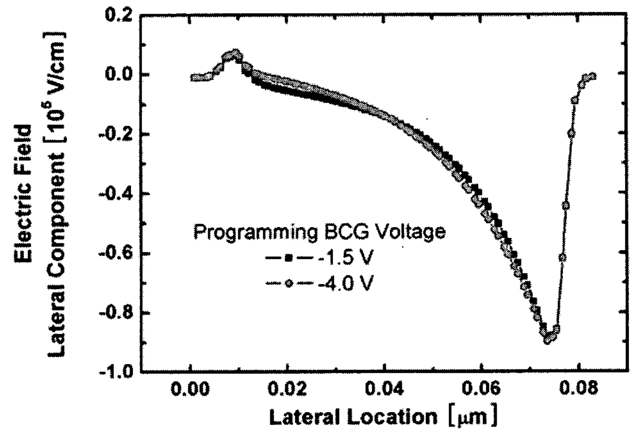
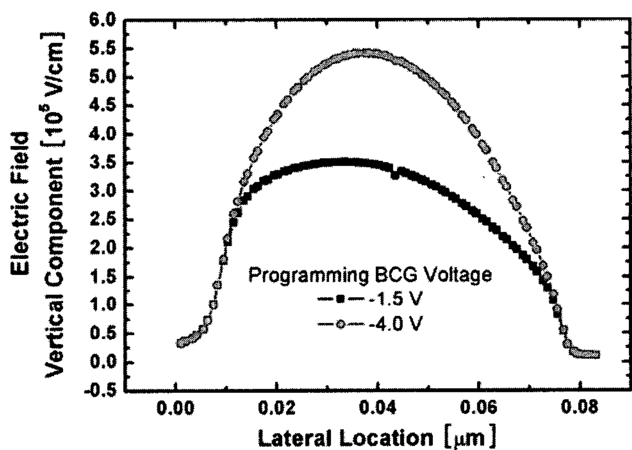


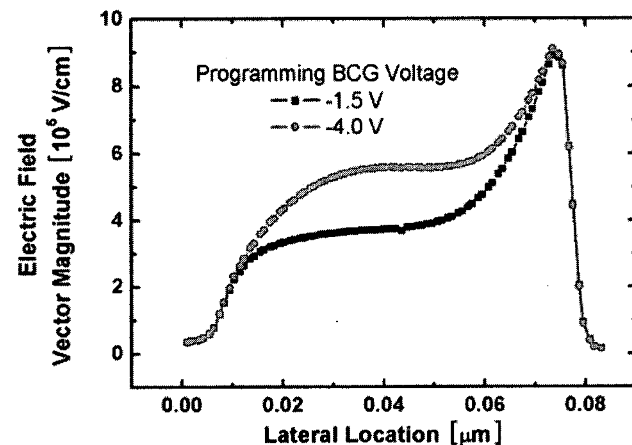
Fig. 2. Number of channel hot electrons injected into TFG aided by CHISEL with negative BCG voltages. The programming gate voltage is 6 V, the drain voltage 2 V, and the source is grounded. The program operation time is 1 us.



(a)



(b)



(c)

Fig. 3. The electric field in (a) lateral direction (b) vertical direction, and (c) the magnitude of electric field vector.

number of electrons injected into TFG after program operations.

As can be seen in figure 2, there was an upper limit on BCG voltages for appropriate amount of injection. More negative bias lower than -2.5 V degraded the injection of channel hot electrons. In this region, the number of electrons tunneled into TFG was smaller than the number in zero programming BCG voltage case. Although there was no monotonous tendency in voltage region from 0 V to -2.5 V, voltage values which lie in this range can be used for programming BCG. This phenomenon can be accounted for in terms of electric field and potential inside the p-type silicon channel. Figure 3 shows the electric field analysis inside the channel of the cell. Two BCG voltages were chosen for comparison. To compare the effects of bottom control gate voltages, two representative values were adopted. One is -1.5 V chosen from less negative voltage, i.e., from 0 V to -2.5 V so that the channel hot electron injection is superior and the other is -4.0 V whose value is below -2.5 V so that the injection is inferior.

The electric field analysis shown in figure 3 were performed on the channel electrons existing along the inversion layer beneath the silicon-gate oxide interface. For this reason, the beginning of the lateral location was a little deep inside the source end and the final location was also around the drain end. The vertical electric field mainly attributed to the magnitude of electric field vector, but the lateral electric field was the important clue that explained the degradation of CHEI due to more negative BCG voltages. According to figure 3(a), the electrons in source region experience larger lateral electric field in magnitude

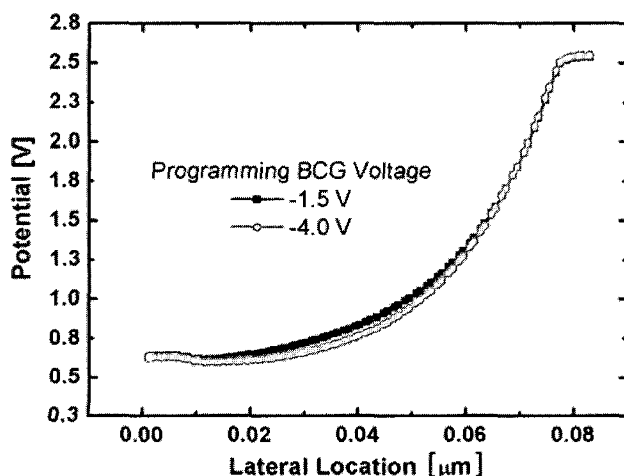


Fig. 4. Potential inside the channel along the inversion layer.

when -1.5 V was applied to the BCG, and this means more electrons are repelled from the source to the channel. Therefore larger number of electrons are present in the channel and the probability of injection into TFG becomes higher [5]. Figure 4 shows the potential inside the channel, which explains another reason for difference in amount of CHEI.

When more negative voltage was imposed on the BCG, the potential barrier for the electrons in the source region to overcome to get into channel region was higher compared with that in case of less negative voltage. Therefore the electric field as well as potential barrier explains the degradation of CHEI in using excessively negative BCG voltage.

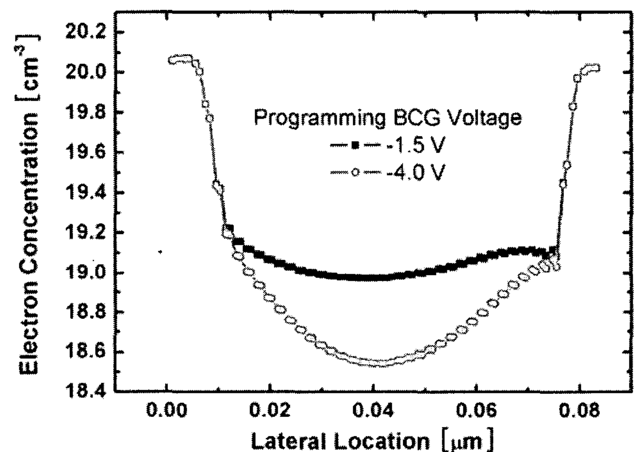


Fig. 5. The distribution of electron along the inversion layer.

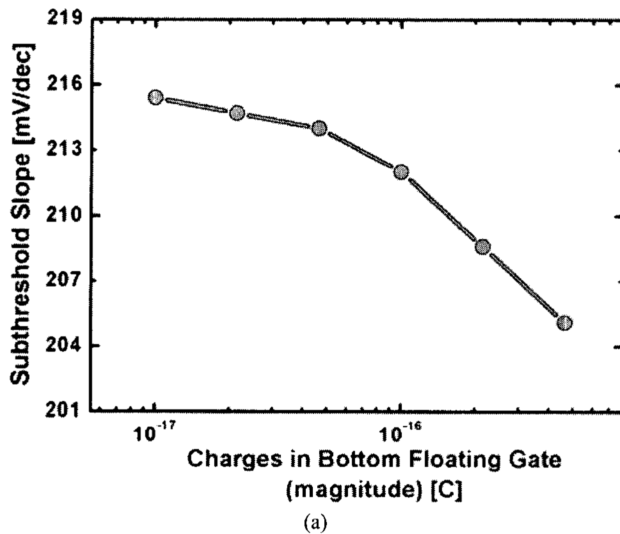
To summarize, the source electrons are prevented from flowing into the channel by the smaller lateral electric field at the source end and the higher potential barrier source electrons see toward the channel when excessively negative BCG voltage is used in program operation. Consequently, in the channel region, the electron concentration with -1.5 V BCG voltage is about five times higher than with -4.0 V BCG voltage as seen figure 5.

2. Read Operations in Fully Depleted (FD) Channel and Partially Depleted (PD) Channel

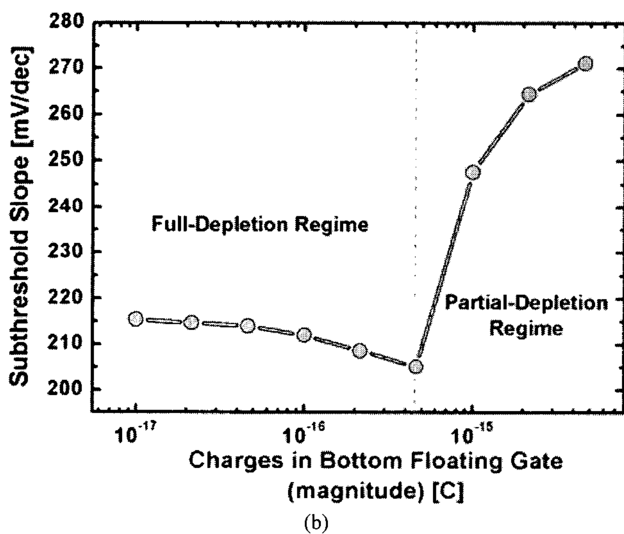
The TCG voltage for program operation should be also considered for reliable operations. Figure 6 shows relation between the amount of charges stored in the BFG and the subthreshold slope. Subthreshold slope is one of the

factors that characterize the read operation and is determined by the charges in the BFG as will be demonstrated. Even though the subthreshold slope is much higher than that of other devices, owing to the inter-poly dielectric layer and the floating gates, the minimization of the subthreshold slope should not be underestimated. The expeditious movement of electrons by the control gate is still important in memory devices, especially for NOR type memory cell which uses CHEI mechanism for program operations. The amount of charge is largely dependent on the programming TCG voltages, which in turn means that TCG voltage substantially determines the device characteristics. The charges programmed in the BFG can put the p-type silicon channel into either fully depleted condition or partially depleted condition.

The effects of the BFG charges on the silicon channel are same as those of BCG negative bias in a sense that they determine whether the silicon channel is fully depleted (FD) or partially depleted (PD).



(a)



(b)

Fig. 6. Subthreshold slope according to charges in the bottom floating gate. (a) Fully depleted channel for small amount of charges (b) Partially depleted channel for large amount of charges.

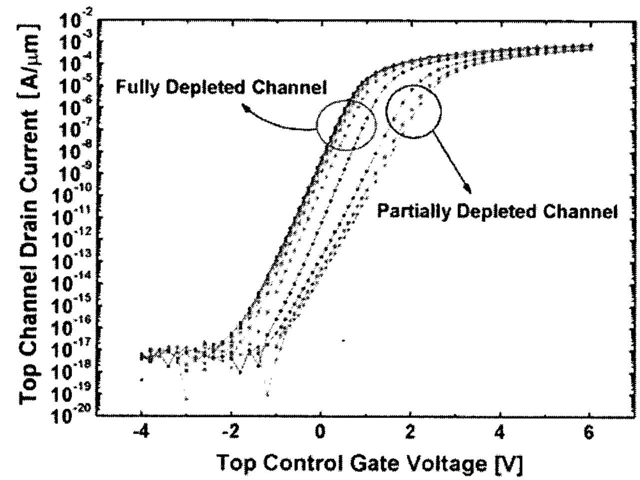


Fig. 7. Top channel drain current versus top control gate voltage.

The subthreshold slope was investigated for 10 state. 1 state for the top channel means erased state and 0 state for the bottom channel means programmed state. For a certain reference gate voltage between 0 V and threshold voltage, the drain current level of a programmed state is lower and that of an erased state is higher definitely, which gives the digits for describing states. Up to some amount of charges in BFG, subthreshold slope decreased monotonically as the amount increases and the absolute value of the subthreshold slope was also low level. But beyond that amount of charges, subthreshold slope jumped to high values drastically and increases monotonically as charges in BFG increase. Figure 7 shows the characteristic curve for top channel drain current versus top control gate voltage in read operation. Negative voltage of -1.5 V was biased on the bottom control gate to decouple the electrons from the channel in read operation. This negative value can be chosen somewhat arbitrarily as far as it decouples the channel electrons but the same value used in program operation is adopted to avoid generating more voltage schemes. -1.5 V lies in the voltage range that enhances CHEI so that BCG voltage of -1.5 V can be used both program and read operations.

The I_d-V_g curve shown in figure 7 shows the changing

tendency of subthreshold slope. Read disturbance in nonvolatile memory read operation can be defined as the difference between the threshold voltages of 10 state and that of 11 state or analogously those of 00 state and 10 state [6]. It means how much the state of the top channel is influenced by the charges trapped in the bottom floating gate. The gate voltages to generate same top channel drain current should be also same but are different actually according to the charges in BFG. The gate voltages differed more severely as the BFG traps larger amount of charges.

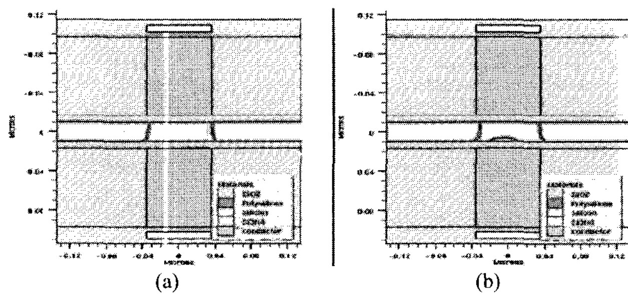


Fig. 8. Examination of depletion region in p-type silicon channel (a) Fully depleted channel. -4.64×10^{-16} C in the bottom floating gate (b) Partially depleted channel. -1×10^{-15} C in the BFG.

Appropriate amount of charges are important in elevating the threshold voltage in nonvolatile memory cell to make definitely distinguishable logic states but the amount should be kept under an upper limit for small read disturbance. The beginning of the full depletion condition edge can be the good upper limit deciding the amount of charges. The 2-D numerical analysis on the channel region were obtained with threshold voltage conditions on each case, 0.86 V in (a) case and 1.43 V in (b) case. Figure 8(b) shows the thinning of the depletion region due to large amount of charges in BFG. Large number of electrons in BFG accumulates majority carriers near the bottom channel of p-type silicon and the fully depleted channel turns into a partially depleted channel. Figure 8 shows the rough boundaries between FD and PD conditions which are drawn with thick and dark line. Onset of PD occurs when charges of around -1×10^{-15} C flow in the BCG. As the depletion width became thinner, subthreshold slope was degraded since the depletion capacitance becomes large [7].

Once the gate oxide is defined, subthreshold slope becomes a function of the depletion region width. Consequently, the increase of BCG charges degrades the subthreshold slope characteristics. But subthreshold slope was 200 mV/dec or higher as can be seen figure 6. This is due to the fact that the top control gate is not directly upon the gate oxide but is intervened by inter-poly dielectric layers and top floating gate above the gate oxide. Therefore effective oxide thickness becomes large and t_{ox} should not be substituted by 7 nm but higher value.

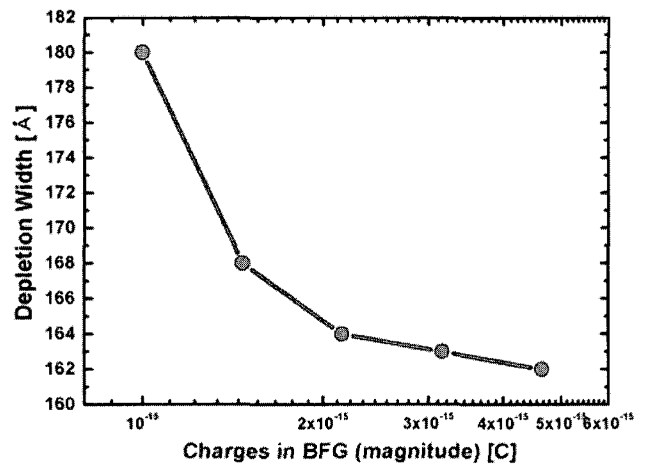


Fig. 9. Depletion width in partially depleted channel regime.

In spite of this relatively insensitive slope characteristic of floating gate type nonvolatile memory, the minimization of subthreshold slope cannot be underestimated. Subthreshold slope is the parameter that enables us to estimate the controllability of gate voltage on the channel electrons. In program operation, the electrons in the source should readily roll out to the channel by the high gate voltage and disappear promptly at the low gate voltage for easy formation of the channel. Thus sensitivity of electrons for the gate voltage is still important when it comes to the nonvolatile memory devices especially to NOR type memory cell which uses CHEI program mechanism. Figure 9 shows that the depletion region width becomes thinner as the amount of charges in BCG becomes large after the onset of partial depletion of the channel. As discussed in this subsection, characteristics of read operation are better in FD condition than in PD condition. In order to make silicon channel fully depleted, appropriate amount of charges are required so it is important to avoid using too much positive TCG voltages

in program operation. This consideration should be counted in circuit designs for voltage schemes.

3. Negative Bias Control in Read Operations

It can be guessed that negatively increasing BCG voltages will give similar results discussed for the charges in the bottom floating gate so far.

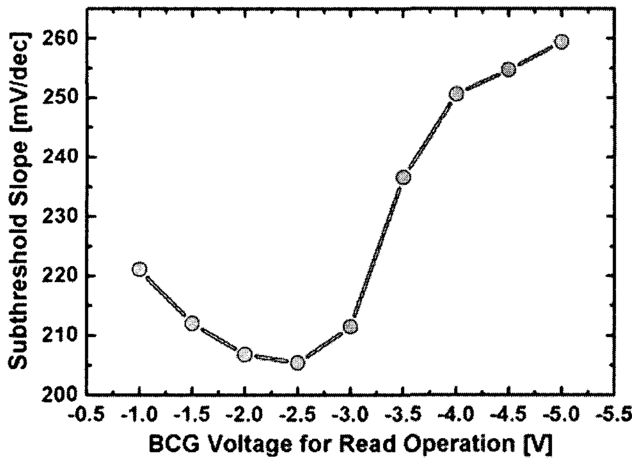


Fig. 10. Subthreshold slope according to read BCG voltages.

We could investigate the effects of BCG voltages in read operation confining fixed number of electrons in the BFG and the fixed charge -1×10^{-16} C. Figure 10 illustrates subthreshold slope depending on the BCG read voltages. The effects of more negative BCG voltages on subthreshold slope is much like those of charges trapped in the BFG as can be seen fig. 6. As can be inferred from figure 10, the onset of conditions for partially depleted channel lies in around -3.0 V. By the same token, the voltage commencing PD could be detected using graphical method as used in fig. 8 and the location turned out to be -3.5 V in this case. The BCG voltages for read operation were varied from 0 V to -5.0 V with -0.5 V spaced actually. But under BCG voltage of 0 V or -0.5 V, the memory cell has negative threshold voltage so those bias conditions are out of consideration.

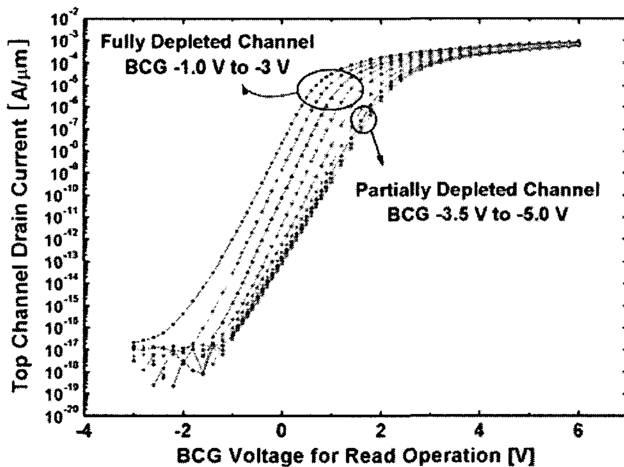


Fig. 11. Top channel drain current versus bottom control gate voltage in read operation.

Figure 11 shows I_d-V_g characteristic and the change of subthreshold slope as the bottom control gate voltage in read operation varies. It is relatively hard to see the change clearly compared with the case concerned with charges in the BFG since the subthreshold slope saturates more rapidly but the general tendency is still similar. The negatively larger BCG voltages give same effects with those resulted by more BFG charges which determine whether the p-type silicon channel is in FD or PD condition and consequently the subthreshold slope.

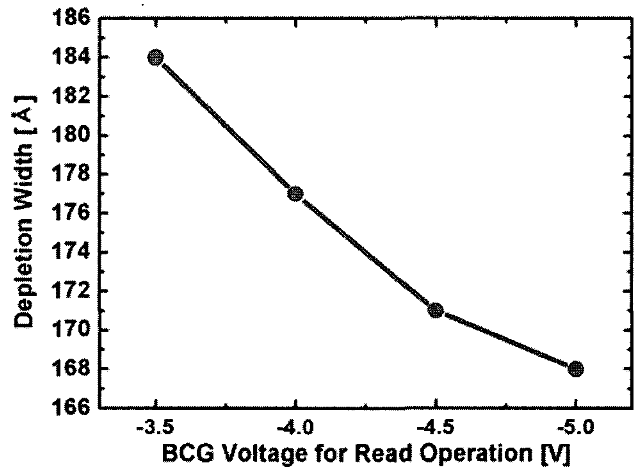


Fig. 12. Depletion width for BCG voltages in the range that makes channel partially depleted.

As can be seen in figure 12, depletion width becomes narrower as the BCG bias goes more negative. More negative BCG voltage has a positive effect in a sense that it can suppress the read disturbance more strictly [8]. For example, assuming same amount of charges stored in BFG, the read disturbance identifying the state of the top channel is smaller with -3.0 V than with -1.0 V on BCG in read operation. Therefore the magnitude of negative BCG voltage should be lowered as far as the read disturbance is

effectively suppressed.

IV. CONCLUSIONS

As mentioned so far, several essential criteria have been set up for voltage schemes for the reliable operation of a floating gate type DG MOSFET nonvolatile memory cell based on quantitative analysis. We focused on field analysis and channel conditions to identify voltage schemes valid ones. The two pillars in determining the voltage schemes are the minimizability and the functionality of voltage sources. The former is undoubtedly a crucial factor in designing driving circuits but the latter should always be considered in advance. Excessively negative BCG program voltages become hindrance to CHEI, far from promoting the injection. Also in read operation, smaller negative BCG voltages are more desirable. Since the characteristics of read operation in FD channel condition are better, less negative BCG voltages that fall into the specific voltage range are recommended in implementing the voltage schemes as far as positive threshold voltages are achieved under those BCG bias conditions. Positive TCG voltage in program operation also should be cautiously controlled. Excessively high positive TCG voltage in program operation inhales excessive channel hot electrons into the TFG, which causes increase of the subthreshold slope, i.e., the sensitivity of electrons to the TCG voltage in read operation and the degradation of read disturbance. It is the preferable way to make these voltages small in magnitude and combine them into as small numbers as possible if only they are guaranteed to be in permissible operating range.

ACKNOWLEDGMENTS

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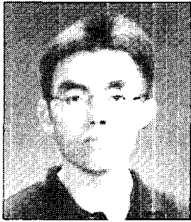

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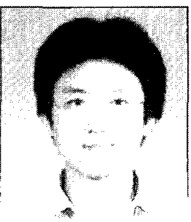

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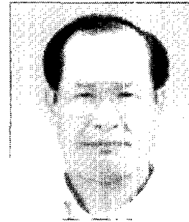

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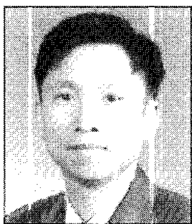

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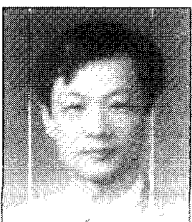

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