A System-on-a-Chip Design for Digital TV

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Abstract—**This paper presents a system-on-a-chip (SOC) design for digital TV. The single LSI incorporates almost all essential parts such as CPU, ISO/IEC 11172/13818 system/audio/video decoders, a video post-processor, a graphics/OSD processor and a display processor. It has analog IP's inside such as video DACs, an audio PLL, and a system PLL to reduce the system-level implementation cost. Descramblers and Smart Card interface are included to support widely used conditional access systems. The video decoder can decode two video streams simultaneously. The DSP-based audio decoder can process various audio coding specifications. The functional blocks for video quality enhancement also form outstanding features of this SoC. The SoC supports world-wide major DTV services including ATSC, ARIB, DVB, and DIRECTV.**

Index Terms—**SOC, digital TV, audio decoder, video decoder, video post-processor, ATSC.**

I. INTRODUCTION

The DTV market is still on its early stage and many manufacturers of DTV sets and set-top boxes as well as component suppliers are competing to increase their market shares. The price competition has already started and the pressure on material cost will get heavy as the market grows. To reduce the material cost for mass production, the cost performance for core components is very important. Furthermore, the trend is that the basic function of DTV is no more the only interest of customers and many new features are introduced especially from the PC area. It seems that even features such as internet connection, USB devices handling, etc will be implemented in DTV in the near future. This means the complexity of DTV SOC are getting higher and thus a stable, well organized, architecture as a base platform is essential for the further development to be successful and effective.

The rule of thumb is that the more features an SOC supports, the higher the SOC can be appraised in the sense of usability. Extensive integration makes the effort and extra cost for PCB design to be small but the cost of the LSI itself remains still as a problem. As a consequence, the decision of what to integrate and what to leave outside is the most important thing for the planning of SOC development. Considering the current status of the market and the technology, we estimated the effort and effect of integrating each functional block into a single LSI, and finally reached the specification of the SOC.

The outline of this paper is as follows. In section 2, the overall picture of the SOC is briefly reviewed. Information on CPU and peripherals, also including bus and memory system is presented in section 3. System decoder, audio decoder, and video decoder together form the base part of the SOC and appear in section 4. Functions for video quality enhancement are described in section 5 in detail as another important feature of the SOC. Finally, conclusions are reached in section 6.

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II. Overall Picture

The SOC integrates a high-performance CPU core, ISO/IEC 11172/13818-1 system decoder, ISO/IEC 11172/13818-3 and Dolby AC-3 audio decoder, ISO/IEC 11172/13818-2 video decoder, display processor, analog composite video decoder, graphics/OSD processor, and several peripherals including UART, ISO/IEC 7816-3 Smart Card interface, GPIO and I2Cs[1][2][3][4]. Analog IPs (two video DACs, audio PLL and x12 PLL) are also integrated to lower the overall system cost, as shown in Figure 1. Various indispensable features are integrated to reduce the total cost and number of chip components required for digital TV and DTV tuner applications for ATSC, DVB, ARIB, DIRECTV, etc[5][6][7][8].

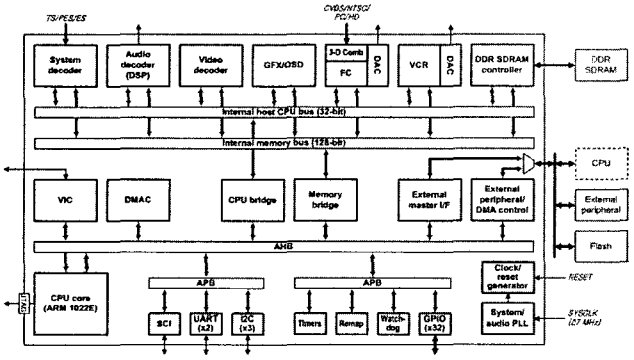

Fig. 1. Block diagram.

III. CPU and Peripherals

1. CPU

To meet performance requirements for covering full spectrum of digital TV applications, such as data broadcasting, PVR (Personal Video Recorder), and so on, the SOC integrates ARM1022E which incorporates ARM10ETM processor core by implementing ARMv5TE architecture. ARM1022E is a 32-bit RISC processor core which is compatible with ARM and Thumb instruction sets. Its main components include integer core, MMU (Memory Management Unit), instruction cache, data cache, branch predictor, prefetch unit, 64-bit AHB (Advanced High-performance Bus) interface, and EmbeddedICE-RT logic for JTAG-based debug.

The cache organization is specialized to provide flexible methods for improving the overall performance. 32KB level 1 cache consists of 16KB instruction cache and 16KB data cache. To minimize conflict cache misses, each cache is 64-way associativity. In addition to high degree of associativity, it is possible to select cache operation scheme either of write-through and write-back per-region basis for the data cache. Cache replacement scheme is also programmable either of pseudo-random or round-robin to reduce the number of cache misses.

Regarding power consumption, caches implement not only low-power CAM (Content-Addressable Memory) but also cache power-down capability.

2. Bus & Memory System

The nature of digital TV always devours memory bandwidth. Besides real time characteristic inherited from its ancestors, there is a solid demand for sacrificing memory bandwidth to achieve the merit of digital era. The SOC has several features on bus and memory system to exploit all feasible memory bandwidth.

The bus system is a composition of four different bus systems: AHB (Advanced High-performance Bus), APB (Advanced Peripheral Bus), host bus, and unified memory bus. From the viewpoint of the CPU, AHB has the highest position is the bus hierarchy and others bus are connected with it though bridges. Memory Bridge connects AHB to memory controller. CPU Bridge connects AHB to host bus by which CPU controls the video/audio processing blocks. Slow peripherals like smart card are grouped into APB bus and are connected to AHB as single bus slave.

In point of the memory, the video/audio processing units and the CPU are at the same distance from the memory. Moreover, video/audio processing unit can access the memory without CPU's assistance. With this structure, since the CPU does not position between video/audio processing units and the memory, the SOC is able to do seamless switching from operations that utilize the CPU to others that don't. The memory contention due to intensive memory accesses is resolved by priority based arbitrations with a starvation preventing algorithm.

AHB bus has a multiple-layered 5x8 bus matrix

structure which can accommodate up to five bus masters with individual bus transactions at the same time. For example, it is possible that the CPU accesses smart card while DMA controller, simultaneously, performs a block move on the memory. DMA controller has eight channels. Each can operate independently. Together with the AHB bus matrix, DMA controller can execute concurrent DMA transactions. For instance, it is capable to handle a transaction from an external peripheral to memory stick and another from OSD to the memory.

Regarding memory system, DDR SDRAM controller, instead of normal SDRAM, is integrated to increase memory bandwidth. Several DDR configurations are supported including 128M bit x1, x2, x4, 256M bit x1, x2, and x4 with choice of 32/64-bit, and 148.5/162MHz.

3. Peripherals

The SOC integrates some on-chip peripherals. It has 32 programmable GPIO pins, two UART channels with modem/IrDA, and a PWM output pin. Total of three I2C interfaces are supported. Two of them are master interfaces and the other one can be a master or slave. It supports a watchdog timer and dual input timers, too. To support various conditional access systems, the SOC has a smart card interface so that it can be directly connected with Philips TDA8004T without any glue logics. It also satisfies NDS extension to meet DIRECTV's requirements [9].

In addition to on-chip peripherals, the SOC supplies an external peripheral bus interfaces categorized into four interfaces: external master bus interface, static memory controller interface, external DMA interface, and external bus arbitration unit. Using the external master bus interface, an external CPU, such as Pentium, can control the SOC while accessing its DDR memory through the external DMA controller. For this case, the SOC acts just like a coprocessor.

IV. System, Audio, Video Decoder

Input streams are accepted in the form of ISO/IEC 13818-1 TS (transport stream), PES (packetized elementary stream) and DVD PS (program stream) [1][10]. The system decoder can process two streams simultaneously with 32 PID filters and 32 section filters per channel. It extracts PCR from the input TS and this can be used for system time clock recovery as specified in ISO/IEC 13818-1[1]. Descramblers such as DES-ECB, MULTI2, CS, and CSS are included for DIRECTV, ARIB, DVB, DVD, respectively. Furthermore, DIRECTV's Advanced Security Feature is also supported [12]. The integrated high-performance DSP handles decoding of commonly used audio standards including AC-3, MPEG, PCM, DTS, AAC and MP3[3][11]. Digital PCM outputs for 6-channel and down-mixed 2-channel may be connected with external audio DACs. The dedicated H/W video decoder can decode two HD video sequences simultaneously. The digital video bitstreams compliant with MPEG-1 and MPEG-2 MP@HL are decoded and converted into a suitable HD/SD display format. Using a memory compression algorithm, it can use only a half or a quarter of the full memory requirement.

V. Video Display Processor

The video display processor supports various functions related with format conversion, image enhancement and display control.

1. Input Interface

DTV video bitstreams are decoded in the internal video decoder block, and transferred to display processor through external memory. In addition to DTV video, the SOC can receive widely used video signals such as composite video, PC input(up to XGA) and component signals(up to 1920x1080, 30i) in the digitized format(D1/YC4:2:2/YC4:4:4/RGB4:4:4). The main functions of input interface include automatic format detection, 3D comb filtering, VBI slicing, D1 decoding and color-space conversion.

2. Format Converter

The format converter supports spatial/temporal video format conversion including scanning-type, aspect ratio,

and chrominance sub-sampling conversions. The SOC has internally two format converters: one for main display and auxiliary one for PIP or VCR output. The auxiliary format converter can be used for simultaneous VCR output for recoding or it is in charge of the sub-window such as PIP/Split-Screen/POP. When operating for VCR output, it converts the high-definition display of the main screen into a 480i/576i composite video through composite video encoder, which produces CVBS and S-video together with CGMS and Macrovision functionality for copy protection. Through such conversion, DTV images can be stored in the analog VCR. In addition, auxiliary format converter can display contents that are independent of the main display content.

Various display modes are provided such as zoom-in/-out, PIP(Picture In Picture), POP(Picture Out of Picture), Split-screen and multi-PIP. They can be categorized into single window, two windows and multiple windows depending on the number of display windows. Arbitrary scaling and positioning of each window is supported for any case. For two-window mode such as PIP/Split-screen, typical combinations of two input video sources include DTV/NTSC, DTV/PC, DTV/component, NTSC/NTSC, NTSC/PC and NTSC/component. Also, DTV/DTV mode is supported for dual DTV channels. POP/multi-PIP is quite useful for channel scanning.

- **De-interlacing**

Format converter includes the motion-adaptive 3-D de-interlacing functions for up-conversion of interlaced SD to HD-resolution. It interpolates the image data using not only spatial but also temporal information as follows. First, it detects the motions using information between four adjacent fields. If there is no motion, temporal interpolation is performed using the pixel data at the same position in the previous/next fields. If there is large motion, spatial interpolation is accomplished using the adjacent pixels in the current field. In the actual implementation, both spatial/temporal interpolation results are averaged depending on the amount of motion.

3. Video signal enhancement

- **Contrast enhancement**

The histogram equalization is implemented for dynamic contrast enhancement depending on the luminance distribution of the video signals. The CDF computation block computes the CDF of the input luminance. The CDF control block restricts allowable range of control points by two lines because the histogram equalization may enhance contrast too much in low-contrast images. Then, the histogram information is temporally filtered by IIR filter in order to avoid flickering artifacts. Finally, the input luminance is transformed by the computed CDF.

- **Sharpness enhancement**

Both 1x9 FIR filter and 3x3 FIR filter are implemented. Depending on the filter coefficients used, the 1x9 filter may be used as a band-peaking or band-bass filter. If used as a band pass filter, it realized more enhanced sharpness control by reducing the filtering error through coring and clipping operation, which reduces low level noise of the filtered signal and suppresses the high level component of filtered signals, respectively.

4. Graphics/OSD

The graphics/OSD block is composed of 2-D graphics engine and OSD (on-screen display) controller. The graphic engine supports the primitives such as line/point drawing, rectangle filling, text manipulation and bitblt functions. It also performs color, Boolean and arithmetic operations. Both RGB and YCbCr color space are supported.

Fig. 2. Package top view.

There are seven planes for Graphics and OSD, which consists of one H/W cursor (32x32), two pseudo/true-color planes, video plane, one 1-bit switching plane, one still picture plane, and one background color plane. A pixel can be expressed in the form of pseudo-color (256 colors by look-up table) as well as true-color (16/24/32 bits/pixel) with full-screen drawing capability. Two look-up tables having the size of 256x32 are prepared for supporting pseudo-color representation. Alpha blending is also supported up to 256-level. Anti-flickering feature is equipped for the interlaced display.

VI. Conclusions

In this paper, we have presented a highly integrated SOC design. The fundamental functional blocks including CPU, system/audio/video decoders, video display processor, and graphics/OSD processor are included to lower the system cost. For pre-silicon verification, the overall design was partitioned into 6 separate FPGAs placed on 24-layer PCB. Some modules such as system decoder and video processor had their own FPGA emulation environment. RTL and gate level simulation of the top design also were included in the verification procedures.

0.13 um 1P 6M logic low-voltage process was used for ASIC implementation. The core and I/O voltages are 1.2 V and 3.3 V, respectively. The package is 600-ball TEBGA and its top view is presented in Figure 2. The next version SOC is under development and it will support USB, PCI to reinforce connectivity, with improved video quality.

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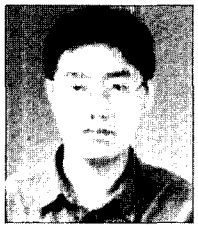

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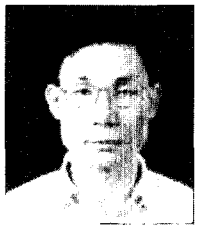

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