Giga-Hertz-Level Electromagnetic Field Analysis for Equivalent Inductance Modeling of High-Performance SoC and SiP Designs

Jason J. Yao*, Keh-Jeng Chang, Wei-Che Chuang**, and Jimmy S. Wang*****

Abstract—**With the advent of sub-90nm technologies, the system-on-chip (SoC) and system-in-package (SiP) are becoming the trend in delivering low-cost, low-power, and small-form-factor consumer electronic systems running at multiple GHz. The shortened transistor channel length reduces the transistor switching cycles to the range of several picoseconds, yet the time-of-flights of the critical on-chip and off-chip interconnects are in the range of 10 picoseconds for 1.5mm-long wires and 100 picoseconds for 15mm-long wires. Designers realize the bottleneck today often lies at chip-to-chip interconnects and the industry needs a good model to compute the inductance in these parts of circuits. In this paper we propose a new method for extracting accurate equivalent inductance circuit models for SPICE-level circuit simulations of system-on-chip (SoC) and system-in-package (SiP) designs. In our method, geometrical meshes are created and numerical methods are used to find the solutions for the electromagnetic fields over the fine meshes. In this way, multiple-GHz SoC and SiP designers can use accurate inductance modeling and interconnect optimization to achieve high yields.**

Index Terms—**Electromagnetic fields, inductance, high-yield designs, system-on-chip, system-in-package, wirebonds.**

Manuscript received October 20, 2005; revised December 3, 2005.
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I. INTRODUCTION

The technology of SoC design made tremendous progress in recent years and the circuits are becoming highly complex. Chip fabrication must also improve to benefit from the innovation of circuit design. However, new challenges arise as the channel lengths are reduced and frequencies increase. In the past, circuit designers only need to consider the effects of parasitic resistance and parasitic capacitance. Now the speed of chips is surpassing multiple GHz, so the accompanying parasitic inductance also increases significantly and can no longer be ignored. Meanwhile, the interconnecting wires between chips are also becoming performance bottlenecks and need special attention for accurate modeling for inductance calculation.

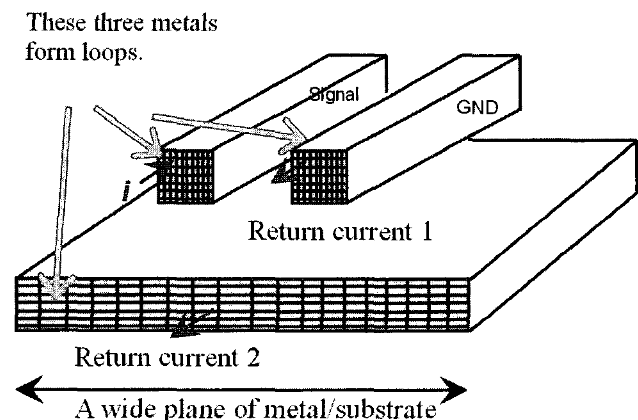


Fig. 1. Accurate inductance modeling with fine meshes.

Considering that the performance bottleneck of SiP and SoC shifted from transistors to on-chip and chip-to-chip interconnects, our inductance research focuses on applying the PEEC-based electromagnetic field simulation

methodology [1] to modeling non-ideal transmission lines as inductance circuits for SPICE-level circuit simulations. It is motivated by the new SiP and SoC interconnect schemes shown in Figures 2 and 3.

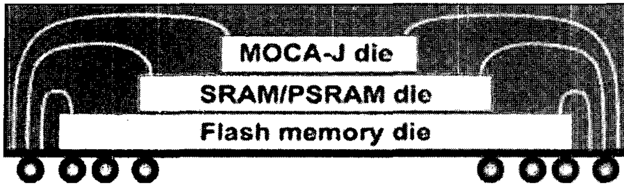


Fig. 2. SiP's solder bumps and wirebonds requiring accurate interconnect modeling [2].

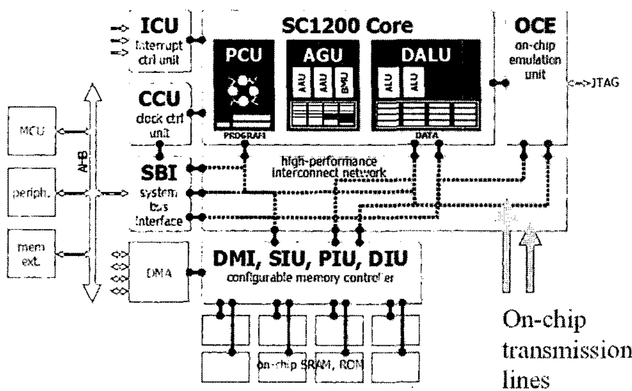
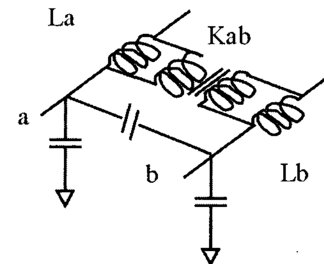


Fig. 3. SoC's on-chip transmission lines requiring accurate interconnect modeling [3].

Solder bumps, shown in Figure 2, have many advantages over wirebonds, especially in impedance control. However, the maturity, flexibility and high-yield of wirebonds make them more widely used than solder bumps now and in the near future for the chip-to-chip interconnects in SoC as well as SiP. For signal integrity, power integrity, and multiple-GHz performance in SoC and SiP, it is essential in providing designers with high-performance and low-noise on-chip and off-chip transmission lines for high-yield products. Since the availability of nearby continuous ground or shield is not always possible for the SoC or SiP transmission lines, accurate electromagnetic field simulations should be used for equivalent inductance modeling of those non-ideal transmission lines.

II. Previous Work

For GHz-level SoC or SiP designs, coupling noise, simultaneous switching ground bounce, and false oscillation are the three major packaging parametric DFM yield killers, where DFM stands for design for manufacturability. Even though S-parameter-based packaging models have been widely used, accurate electrical modeling of on-chip and chip-to-package interface for SPICE-level time-domain simulations, shown in Figure 4, is becoming necessary.



SPICE K model (Kab=Mab/SQRT(La*Lb))

Fig. 4. SPICE L, C modeling of critical interconnects.

Shown in Figure 5 is a physical design of SiP utilizing wirebonds as the off-chip interconnects. For long and critical chip-to-chip interconnects, providing complete ground plane for them is not possible in the depicted SiP designs, but shielding wires parallel to the signal wires can be provided for improved signal integrity.

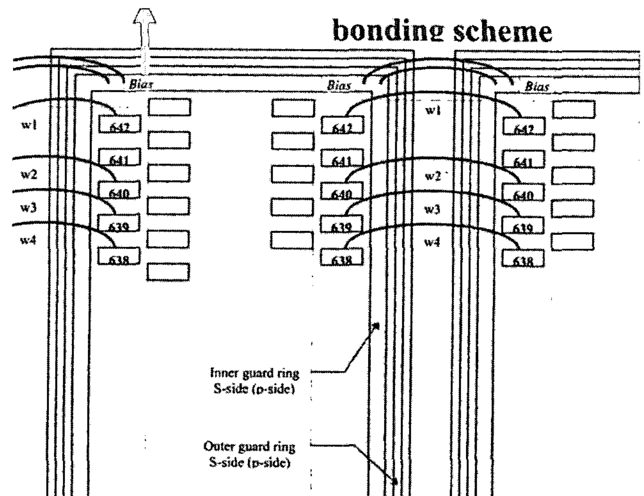


Fig. 5. The physical design of bonding wires [2].

For stacked chips in SiP, also known as SoP shown in Figures 6 and 7, ground planes or "electromagnetic references" do exist. They are "broken grounds" similar to the situation in Figure 5, but their resulting inductance models can be accurately simulated by PEEC. Designing fine meshes that can model the transmission-line effects for wirebonds with four broken ground planes, as exemplified in Figure 7, is proposed and implemented in this paper for high-yield SoC and SiP designs.

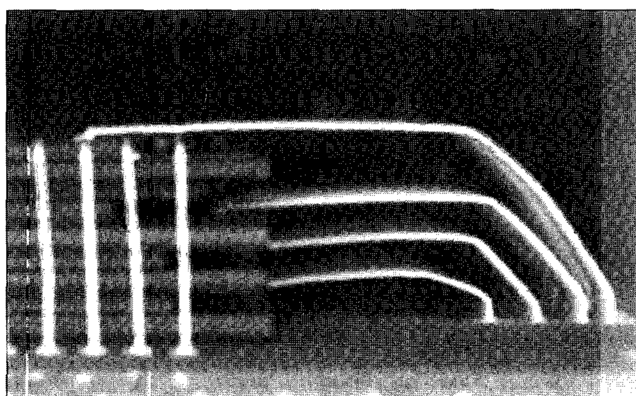


Fig. 6. Complex wirebonds in SiP with stacked multiple chips.

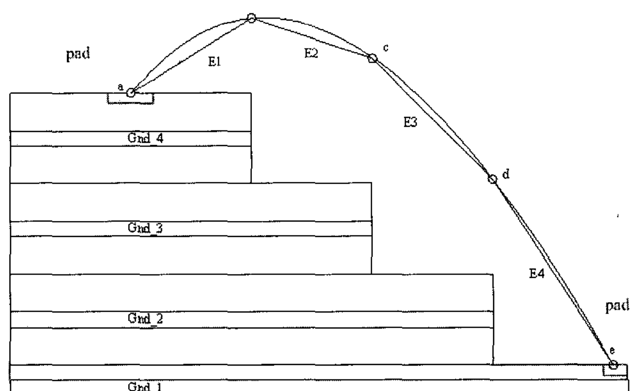


Fig. 7. Using electromagnetic field simulation to model the complex transmission-line effects in wirebonds in SiP.

In essence, to achieve accurate electromagnetic field simulation for SiP and SoC, we propose Figure 7 for high-yield inductance modeling.

III. PEEC Electromagnetic Simulations

PEEC-based electromagnetic simulations can provide inductance matrices containing both self inductance and mutual inductance, as shown in Figure 4. On the other hand, there are many signal wires and power wires in an SiP or SoC. The resulting inductance matrices among those wires require huge data, so the first step in our methodology is to begin with a simplified simulation window with correct electromagnetic boundary conditions.

Shown in Figure 8 is a simplified physical simulation of the wirebonds in the SiP in either Figure 5 or Figure 6, where self and mutual inductances must be accurately modeled.

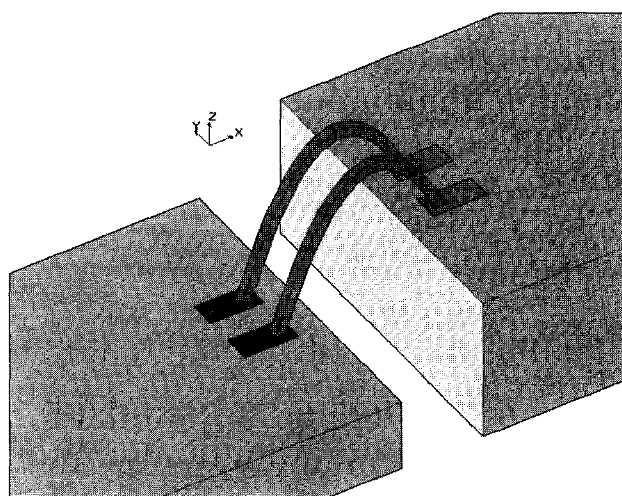


Fig. 8. A first step to achieve accurate electromagnetic field simulation.

Comparing Figure 8 with real-world transmission-line designs, we design our modeling methodology to include the four essential electromagnetic simulation building blocks, shown in Figure 9, for inductance modeling of various on-chip and off-chip inductance modeling.

For Cases 1 and 2 in Figure 9, the resulting self inductance data per one millimeter-long wire vs. line width above one complete ground is shown in Figure 10. Our

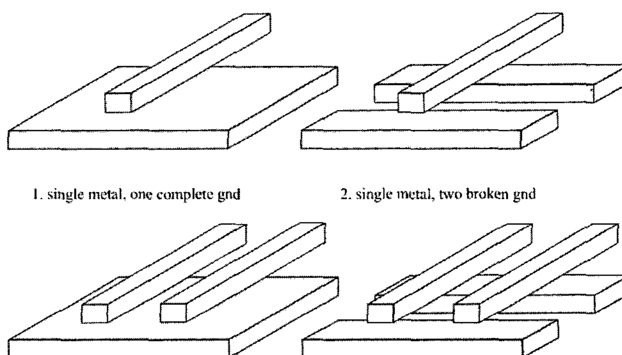


Fig. 9. The four building blocks of our inductance modeling methodology.

further simulations, shown in Figure 11, indicate the self inductances in Case 2 with broken grounds are around 10% larger than that in Case 1, depending on the size of the gap between the two grounds. The larger the gap, the larger the increase in inductance. In Case 1, Case 2 or other cases, our electromagnetic field simulations indicate a decrease in inductance when the operating frequency increases from 1 GHz to 10 GHz, as shown in Figure 10. Our results are consistent with the inductance publications in the academia which interpreted the decrease as the skin effect coupled with the increase in resistance at high-frequencies [4][5]. The skin effect also explains the decrease in inductance in Figure 10 when the width of the transmission lines increases.

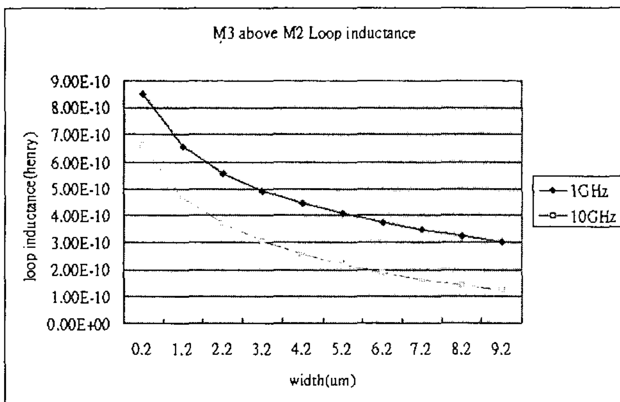


Fig. 10. The decrease of inductance due to either wider width or higher frequency.

For Cases 3 and 4, the resulting inductance matrix for a pair of one-millimeter-long wirebonds, i.e. M1 and M2, is shown below by assuming both wirebonds are transmitting signals. However, if one of the two wirebonds is used as a shielding wire, the resulting loop inductance for the signal wirebond is decreased from 0.462 nH to 0.285 nH per millimeter at 1.0 GHz.

4.62e-10 Henry M1 Self Inductance	1.77e-10 Henry M1 and M2 Mutual Inductance
1.77e-10 Henry M2 and M1 Mutual Inductance	4.62e-10 Henry M2 Self Inductance

IV. Wirebond Inductance Data

Using Figure 9, we simulated various inductance data for circuit design and analysis to achieve high yields.

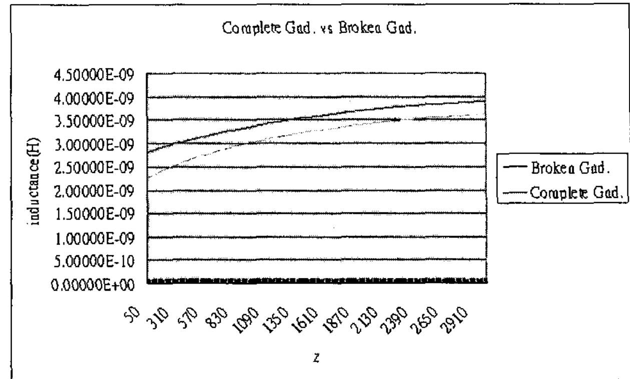


Fig. 11. 3-mm-long wirebond inductance without shielding wire nearby.

For 3-mm-long wirebonds, the inductance values shown in Figure 11 range from 2.3 nH to 3.9 nH. However, after a nearby shielding wire is provided, the inductance values decrease and become strictly bounded in the range of 1.8 nH to 1.9 nH, as shown in Figure 12.

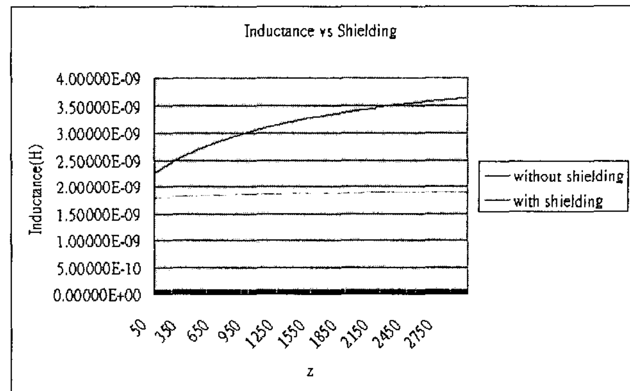


Fig. 12. 3-mm-long wirebond inductance with a shielding wire nearby.

In either Figure 11 or Figure 12, the distances between the wirebond and the ground used by our simulation runs mimic the real-world cases. They range from 50um to 3000um, as shown in Figure 13.

V. Conclusions and Future Work

For SiP and SoC on-chip and off-chip interconnect modeling and circuit-level simulation, we propose using electromagnetic field simulations that can be easily

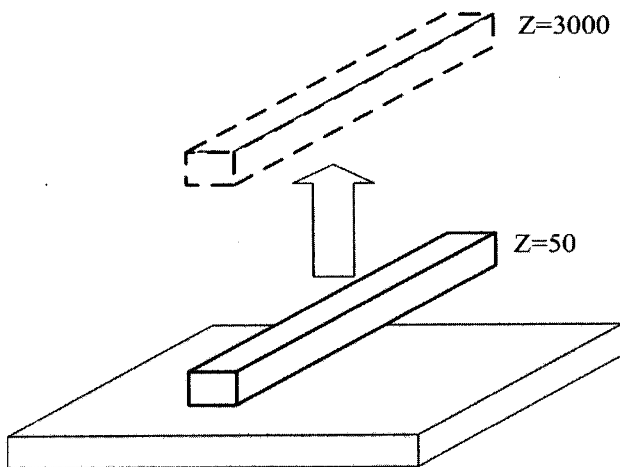


Fig. 13. Wirebonds can be far away from the ground.

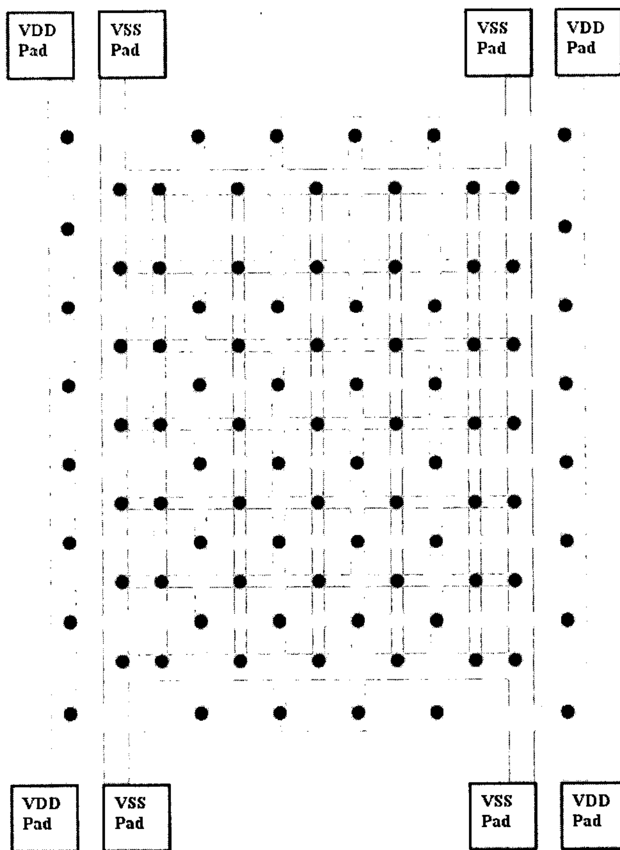


Fig. 14. Power grids used as the reference of on-chip transmission lines.

expanded for real-world wirebond inductance simulations. We have observed the importance of using shielding wires for impedance control as shown in Figures 12. For on-chip transmission lines with wires using the slotted copper metal grounds or power grids, as shown in Figure 14, as the electromagnetic reference, the same principle can also be applied.

To go one step further, an array of inductance tables under different configurations can be constructed through FastHenry, our choice of PEEC inductance calculation. As it is observed that the inductance changes monotonically, we may use interpolation to estimate its value within the range of the inductance tables. Initial results indicate that good approximation is achieved. This approach may help circuit designers working on critical transmission lines. Future research will analyze the inductance tables with numerical methods and generate formulae that may lead to better tools and insights for circuit designers.

VI. ACKNOWLEDGMENTS

The authors want to thank the academic help of Dr. Victor Chang, Dr. Kelvin Doong, Dr. Konrad Young, Mr. Yao-Feng Lin, and Dr. Clinton Chao of TSMC, Hsinchu, Taiwan, during the research of this paper. They also want to thank the academic help of Dr. Yu-Long Chin, Mr. Yun-Chi Chiu, Mr. Tse-Hung Liu, and Mr. Lumdo Chen of UMC, Hsinchu, Taiwan. This research and this paper have been funded by three Taiwan-ROC government research and development funds: ROC-MOEA 94-EC-17-A-01-S1-038, ROC-NSC 94-2220-E-007-013, and ROC-NSC 94-2220-E-007-032.

REFERENCES

[1] Keh-Jeng Chang et al., "Accurate Nanometer Copper Interconnect Inductance Modeling Using Giga-Hertz Wafer Measurement," *Proceedings of 20th VMIC*, Marina del Rey, USA, 2003.

[2] Richard Ness, "Java accelerator combines with memory in one package," www.pd.pennet.com, February 2003.

[3] StarCore LLC, "Embedded Platform SP1202," www.starcore-dsp.com, August 2005.

[4] Min Xu et al., "An Efficient Model for Frequency-Dependent On-Chip Inductance," www.eda.ece.wisc.edu, August 2005.

[5] M. Kamon et al., "FastHenry: A Multipole-Accelerated

3-D Inductance Extraction Program," *IEEE Trans. Microwave Theory Tech.*, vol.42, no.9, pp.1750-1758, 1994.

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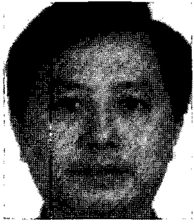

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