

# A High Swing Range, High Bandwidth CMOS PGA and ADC for IF QPSK Receiver Using 1.8V Supply

Woo Yol Lee, Jong Chul Lim, Hee Won Park, Kuk Tae Hong, and Hyeong Soo Lee

**Abstract**—This paper presents a low voltage operating IF QPSK receiver block which is consisted of programmable gain amplifier (PGA) and analog to digital converter. This PGA has 6 bit control and 250MHz bandwidth, 0~20 dB gain range. Using the proposed PGA architecture (low distortion gain control switch block), we can process the continuous fully differential 0.2~2.5Vpp input/output range and 44MHz carrier with 2 MHz bandwidth signal at 1.8V supply voltage. Using the sub-sampling technique (input freq. is 44~46MHz, sampling freq. is 25MHz), we can process the IF QPSK signal (44~46MHz) which is the output of the 6 bit PGA. We can get the SNDR 35dB, which is the result of PGA and ADC at full gain mode. We fabricated the PGA and ADC and the digital signal processing block of the IF QPSK with the 0.18um CMOS MIM process 1.8V Supply.

**Index Terms**—Low distortion gain control switch block, 2.5Vpp, 250MHz bandwidth, Sub-sampling ADC, 1.8V supply

## I. INTRODUCTION

The era of cable TV is expanding in an unprecedented fashion and rapidly growth at the market. The highly integrated single chip receiver is developed to reduce cost, power consumption and size. Although recently IF architecture have been widely used in communication

system to reduce the external component count as shown in Fig.1 The received signal is usually quantized by an analog-to-digital converter(ADC) and the programmable gain amplifier(PGA) is usually placed in front of the ADC to adapt the loss variation of the transmission channel so as to ease the dynamic range requirement for the ADC. It is critical for the PGA to maintain its linearity and low noise over the entire signal bandwidth as well as gain range. The issue point of the low voltage supply and large swing input signal is the swing range of the PGA & ADC. Especially, the input of the PGA is continuous signal and also the output PGA is continuous signal. So, the PGA must have static common mode with complementary input circuit for stable operation at low supply voltage. The gain control block of PGA generates the distortion, so the design of the gain control block is important for the performance of the PGA. Using the proposed resistor string control block, we can reduce the distortion noise. For the IF QPSK architecture to reduce the external component count, the ADC must have the function of IF signal to baseband signal. From the IF signal to baseband signal, the ADC must have sub-sampling technique at input sampling block of the ADC. For the better performance sub-sampling, the sampling block of the ADC must have been used the gate boosting technique. Shown in Fig. 1 is the IF QPSK receiver block. The IF QPSK is consisted of the Tuner, AGC, Mixer, Amp, SAW filter, Amp, PGA, ADC and digital processing block.

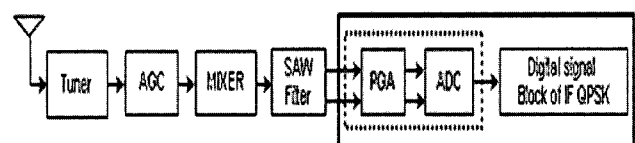


Fig. 1. IF QPSK receiver block.

## II. IF QPSK RECEIVER ENVIRONMENT

The input of PGA is 2.5Vpp (max) and 44 MHz carrier frequency and 2MHz bandwidth continuous differential signal. The power supply of PGA&ADC is 1.8V supply and the input and output range of the PGA is about 2.5Vpp (max). It means that the PGA must have a large swing range and the static common mode feed back circuit at differential input/output amplifier.

The common mode feedback circuit of the PGA has the large operational range. When the AGC and PGA at IF QPSK receiver block is stable, if the gain step between the digital input code of the PGA is large, the slight change of the PGA digital input code, the output of the IF QPSK block may be unstable. The flatness of the input signal bandwidth is very important for the performance of the IF QPSK receiver block. If the PGA has the tilt at the input signal bandwidth, the system has the ghosted signal. It degrades the image of the cable TV. The ADC of the IF QPSK is consisted by 6 bit ADC. The ADC of IF QPSK has the sub-sampling technique. The sub-sampling technique is better conversion performance from the IF signal to the base-band signal.

## III. IF QPSK RECEIVER CIRCUIT DESIGN

### 1. PGA Block Design

Fig. 2 is a conventional fully differential PGA using linear resistors in the feedback network to achieve high linearity[1],[2]. The voltage gain can be adjusted by changing the ratios of  $-R3/RV$ .

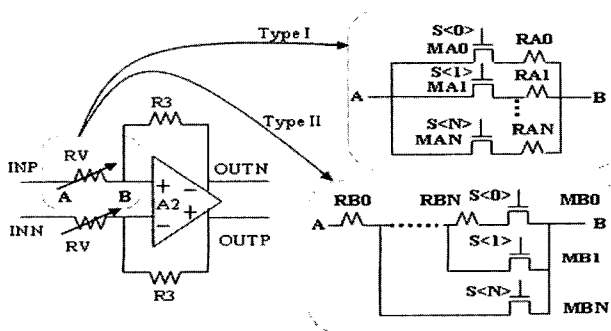


Fig. 2. The conventional PGA and resistor control.

Fig. 2. at the conventional PGA block shows two resistor-control types. At the type I, the variable resistor value(RV) is selected using the select signal  $s<63:0>$ . Also at the type II, the variable resistor value(RV) is selected using the select signal  $s<63:0>$ . The variable resistor value(RV) is consisted of the resistance of the transistor and resistor. The weak point of the conventional PGA is that when the input is engaged, the resistance of the s/w transistor (MA0~MA63 at Fig. 2, MB0~MB63 at Fig. 2) differs at the input voltage range. It means that whether the analog input of the PGA is high of low level, the resistance of RV is differ. This effect added the distortion to the original signal.

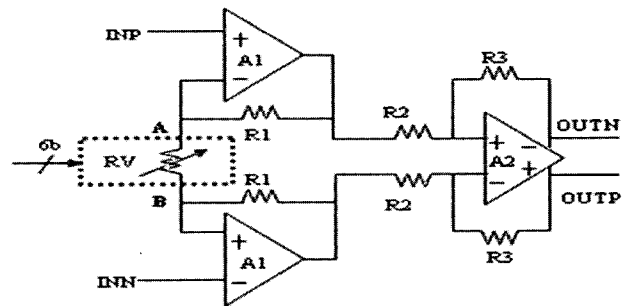


Fig. 3. The proposed PGA block.

If the resistor and transistor is series located for the gain control at Fig. 2, the dependency of signal frequency and input voltage swing level is increased. Also if the resistor and transistor is parallel located for the gain control such as at Fig. 2, the dependency of signal frequency and voltage level is increased. Especially the input frequency is increasing and continuous signal, the degradation is large. So this problem is solved by proposed architecture by Fig. 3, Fig. 4. The proposed PGA is consisted of three blocks. The gain control block and the first amplifier A1, the 2<sup>nd</sup> amplifier A2 at Fig.3. At the resistor control block, the resistance between the node A, B is RV at Fig.4. So the voltage gain of this PGA is  $-(1+2R1/RV)*(R2/R3)$ . The gain control block of the PGA is consisted of the resistor and s/w transistor. When the gain is selected, the only one s/w is opened between the  $S<63-0>$ . At the maximum gain, the switch  $S<63>$  is on and the other all s/w's are off. At the minimum, the gain  $S<0>$  is on and the other all s/w's are off. The following equation is the gain of the conventional PGA and the proposed PGA.

$$R_{on} = L / (K'W(V_{gs} - V_{th} - V_{ds})) \tag{1a}$$

$$A_{v(type I)} = -R_3 / R_v \tag{1b}$$

when  $R_v = R_{on\_MA} + R_{A1}$

$$A_{v(type II)} = -R_3 / R_v \tag{1c}$$

when  $R_v = R_{on\_MB1} + R_{B0} + R_{B1} + \dots + R_{BN-1}$

$$A_{v(proposed)} = -(1 + 2 * R_1 / R_v) * R_2 / R_3 \tag{1d}$$

where  $Max\_gain\ R_v = (R_{on\_MB63} + R_s + R_s) // (R_{63} + R_{62} + \dots + R_{R0} + R_T + R_{0B} + R_{1B} + \dots + R_{63B})$

$$where\ Min\_gain\ R_v = (R_{on\_MB0} + R_s + R_s) // (R_0 + R_T + \dots + R_{0B} + R_{63} + R_{62} + \dots + R_1 + R_{1B} + \dots + R_{62B} + R_{63B}) \tag{1e}$$

The (1a) equation is the on resistance of the MOS transistor in the linear region. The (1b), (1c) equation is the conventional gain of the PGA block. The demerit point of the conventional gain of the PGA is that the variable gain  $R_v$  is affected by input range. It means that there is different  $R_v$  value whether the input swing range is large or not. It degrades the AC characteristics of the PGA. We solved the conventional gain system using the proposed gain control architecture Fig 4.

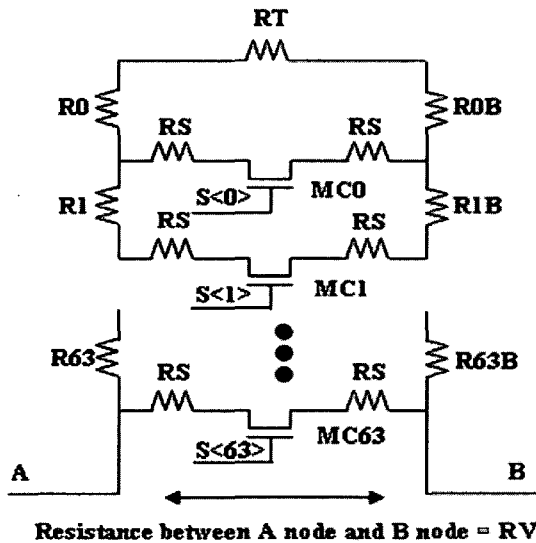


Fig. 4. The proposed gain control resistor block.

The proposed gain control equation is presented by (1d), (1e). The equation (1d) is the maximum gain equation. The equation (1e) is the minimum gain equation. The equation (1d),(1e) show the minimum variation of the  $R_v$  at the comparison of the conventional architecture. At the (1d),(1e) equation, the  $R_{on}$  is series with the  $R_s$  and parallel with  $R_T, R_{[63-0]}, R_{[63-0]B}$ . So, we can get the good linearity and ac characteristics at 44MHz carrier

frequency, 2MHz bandwidth, 2.5Vpp differential input swing range. The A2 amplifier of the PGA at Fig.5 must have the low voltage operation and high speed, high swing differential input/output. Because the PGA block is used only 1.8V supply voltage, the common mode feedback circuit is important also the input circuit block and output circuit block is important. First, the input circuit of the A2 amplifier must have complementary pairs (pmos diff. amplifier/nmos diff. amplifier). The complementary input circuit covers the all range of the input range at low supply voltage.

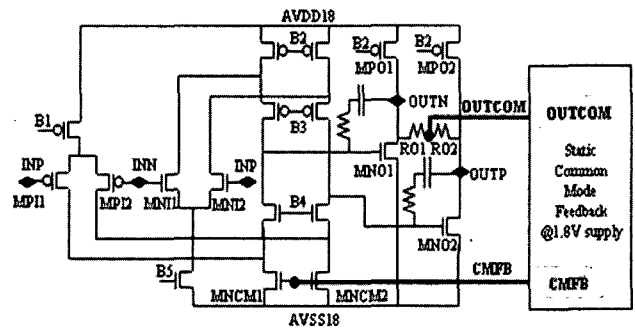


Fig. 5. Differential input/output A2 amplifier for PGA.

Second, the output common mode feedback circuit at Fig. 6. must process the continuous differential output signal and the large operation range. It means that if the common signal of the PGA differential output is low or high, the output common mode voltage must be maintained the half power voltage. It means that the input circuit of the common mode circuit must have the complementary pairs (pmos diff. amplifier and nmos diff. amplifier) at Fig. 6. So, the output common mode feedback circuit always maintains the stable output common mode voltage whether the diff. output common voltage is high or not. Third, for the large output swing range, the output stage is pmos MP01, MP02 and MN01, MN02. And the output of common mode feedback circuit is not 2<sup>nd</sup> stage of A2 amplifier. The output of the common mode feedback circuit is first stage at MNCM1, MNCM2. So, we can have large input/output swing range and high gain and high bandwidth. For the good performance, the bandwidth of the PGA block (1<sup>st</sup> amp and 2<sup>nd</sup> stage amp) must be larger than 250MHz. Generally the bandwidth of PGA must be higher than 5 times that of the input frequency. The bandwidth of the first amp. A1 and the second A2 is about

300 MHz. And the gain of amplifier(A1, A2) is higher than 60 dB for good linearity.

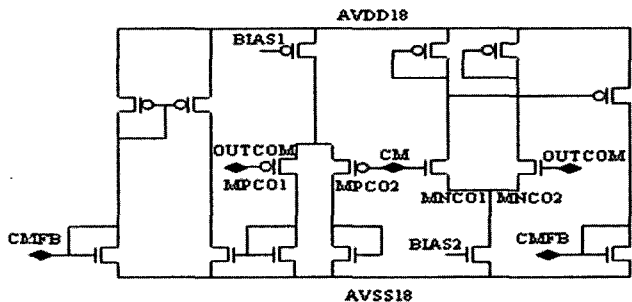


Fig. 6. Proposed static common mode feedback circuit for low voltage operation.

2. ADC Block Design

The QPSK receiver block is needed to analog to digital converter because the IF QPSK signal from PGA must be converted to digital signal for processing. At this paper, 6 bit pipelined analog to digital converter is used. Fig. 7. shows the 6 bit ADC block.

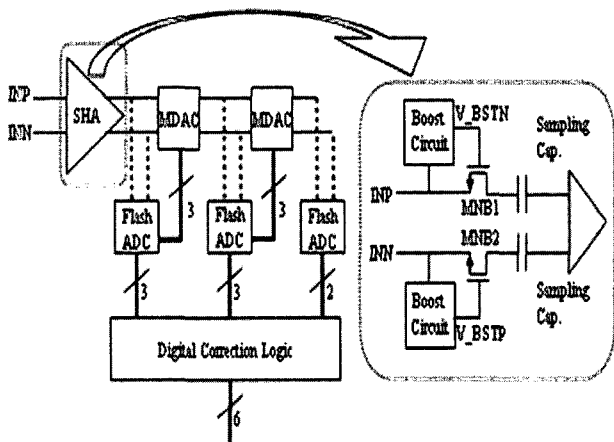


Fig. 7. The sub-sampling 6bit ADC for IF QPSK signal processing.

Because the input of the ADC is IF QPSK signal, the input sampling block of ADC must converted the IF signal(carrier freq. is 44MHz) to the low IF signal(carrier freq. is 6MHz). The input frequency of PGA is 44 MHz carrier signal (2MHz bandwidth) and the clock frequency is 25MHz. At the high speed and high swing input, the variation of the on-resistance of input switch degrades the performance of ADC. So, we must use the boosting scheme [3]. At the Fig. 7 shows the ADC and the gate

boosting circuit. At the Fig. 7 the V\_BSTN, V\_BSTP is the boosting voltage and the on-resistance of the MNB1, MNB2 is constant regardless of the input swing range. It is consisted of the sample and hold amplifier and MDAC, flash ADC and DCL logic.

IV. EXPERIMENTAL RESULTS

The IF QPSK chip with the 6bit PGA and ADC we proposed has been fabricated in a 0.18um 1P6M CMOS MIM process. At the 1.8V supply voltage, we can get the input range which is 0.2Vpp~2.5Vpp without any degradation of the system performance using the proposed the gain control architecture. When we engaged the input signal to the IF QPSK system, Fig. 8. shows the test result of PGA&ADC using the external DAC at the end of the PGA and ADC block. The graph of Fig.8 shows that the gap between the noise level and the signal level is around 32 dB.

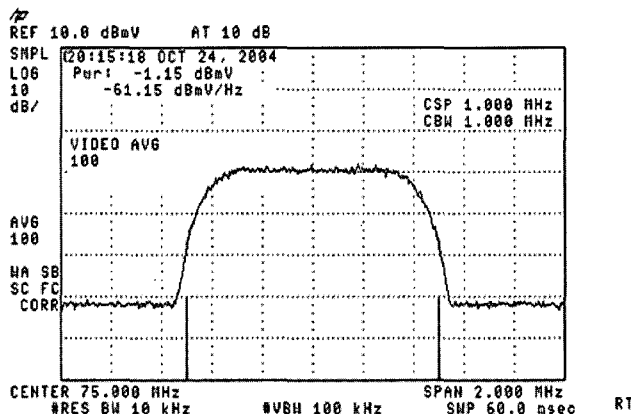


Fig. 8. The result measurement of IF QPSK receiver block.

The sub-sampling ADC has the input frequency is 44MHz and the 2MHz bandwidth. The test result of ADC when the input frequency is 46 MHz and sampling frequency is 25 MHz (sub-sampling) is 35 dB SNDR at the 2.5Vp-p ADC input range.

Fig. 9 shows the system performance using the PGA and ADC block at the data space diagram. The system signal is converged at four points without the scattering. It is good performance for system working. Fig.10. shows the photo diagram of the PGA and ADC block at the IF QPSK chip.

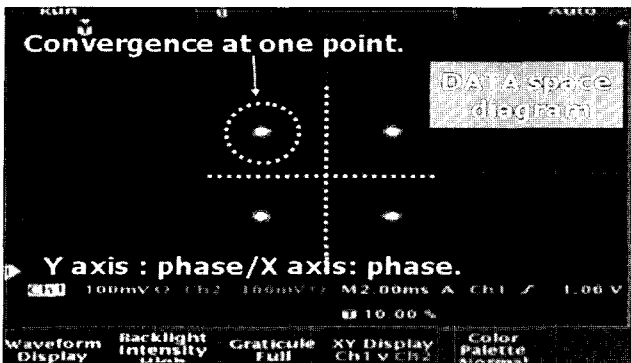


Fig. 9. The data space diagram of IF QPSK receiver.

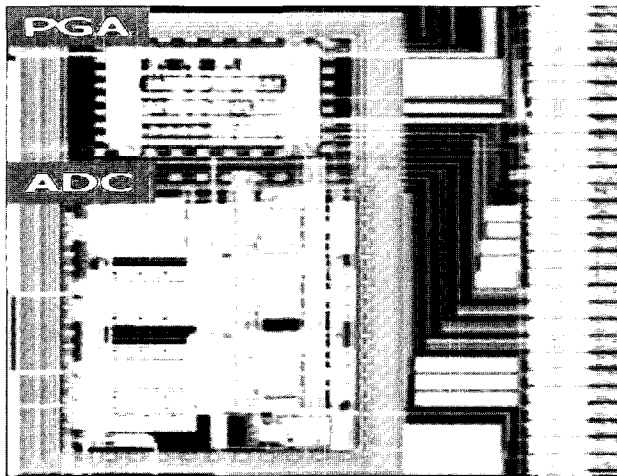


Fig. 10. The photo diagram of the PGA and ADC at the IF QPSK receiver chip.

Table. 1. The summary of chip performance

Parameter	Performance
Technology	0.18 $\mu$ m 1P 6M CMOS MIM process 1.8v
Input freq	44 +/- 2MHz
Supply Voltage	1.8v
Input Voltage range	0.2Vpp~2.5Vpp
PGA gain	0~20dB
PGA&ADC SNDR	35dB@46MHz input freq
Gain step	<0.4dB
Power consumption	55mW@25MHz sampling freq
Chip Area	2000*900 $\mu$ m <sup>2</sup>

## V. CONCLUSIONS

In this paper we realized IF QPSK receiver chip with PGA and 6-bit sub sampling ADC block at the cable TV application. For the proposed architecture, we can have 2.5Vpp input/output voltage range at 1.8V supply and 300

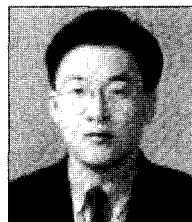
MHz bandwidth without the degradation of the signal. The PGA has the 0dB ~20dB gain range. And the sub-sampling ADC adopted the gate boosting technique at the sampling circuit, The performance of the ADC is good performance at the SNDR. At the data space diagram, we will find the good system performance of the IF QPSK receiver chip

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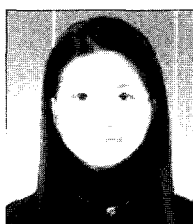
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