論文
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The Electrical Properties of Single-silicon TFT Structure with Symmetric Dual-Gate for kink effect suppression

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Abstract

In this paper, we have simulated a Symmetric Dual-gate Single-Si TFT which has three split floating n+ zones. This structure reduces the kink-effect drastically and improves the on-current. Due to the separated floating n+ zones, the transistor channel region is split into four zones with different lengths defined by a floating n+ region. This structure allows an effective reduction of the kink-effect depending on the length of two sub-channels. The on-current of the proposed dual-gate structure is 0.9㎃ while that of the conventional dual-gate structure is 0.5㎃ at a 12V drain voltage and a 7V gate voltage. This result shows a 80% enhancement in on-current. Moreover we observed the reduction of electric field in the channel region compared to conventional single-gate TFT and the reduction of the output conductance in the saturation region. In addition, we also confirmed the reduction of hole concentration in the channel region so that the kink-effect reduces effectively.

Key Words : Dual-gate TFT, Floating N+ channel, on-current, kink effect, output conductance

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1. Introduction

In general TFTs, the output characteristics exhibit an anomalous increases in the saturation current, often calls kink effect. This added drain current the floating body harder, thereby causing a regenerative action which leads to a premature breakdown. In addition, this result causes an increase of the output conductance. It causes several undesirable effects in the electrical characteristics. The kink effect increases the power dissipation in the digital circuit and slightly degrades the switching characteristics while it reduces the maximum attainable gain as well as the common mode rejection ratio in analog circuit applications.[1] To overcome this kink-effect, several structures have been investigated, including drain offset, multiple gate, lightly doped drain(LDD)[2], and gate overlapped LDD(GOLDD)[3] and split LDD(SLDD). The conventional dual-gate structure has one floating n+ zone so decreases the leakage current which exponentially increases with the drain field but also reduces the on-current simultaneously.

Based on this idea, we proposed the symmetric dual-gate structure with three split floating n+ zones and this structure suppress the kink-effect. We also proposed the three split floating n+ zones in the channel region and improved the on-current compared to the conventional dual-gate TFT.

2. Simulation

We used the SOG wafer for single-crystal silicon TFT. P-type wafer and pyrex 7740 wafer are bonded by anodic bonding method. We fabricated the device by 2-D numerical simulation program ISE-TCAD. Its simulation process are as follows; Single crystal silicon active layer 400 nm in thickness on 100 nm oxide was bonded by anodic bonding method at 380 ℃, 700 V in a EBS-2000A. Floating N+ regions were doped by implanting Phosphorus at 100 keV with dose of 2×10^{15}, activated by annealing at 500 ℃ in nitrogen. The source and drain were doped by implanting P at 130 keV with dose of 4×10^{5}, activated by an anneal 550 ℃ in nitrogen. A 150 nm gate oxide is deposited by LPCVD. Molybdenum was subsequently deposited by sputtering and patterned to form the gate as well as the metal contacts for 700nm of the source and drain. Fig. 1. shows a 100 nm oxided SOG wafer which is fabricated. A cross section of the proposed dual-gate TFT structure is shown as fig 2.

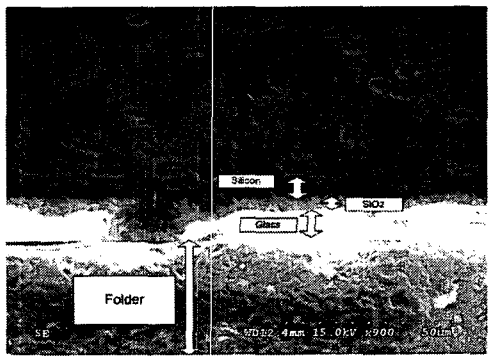


Fig. 1. A 100 nm oxided SOG wafer.

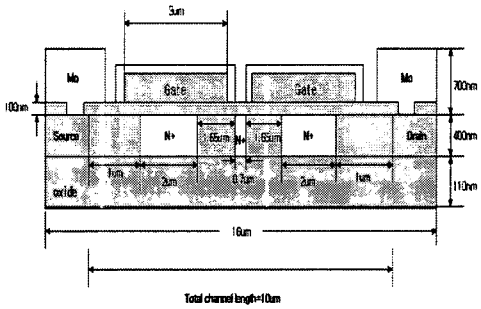


Fig. 2. Symmetric dual-gate TFT with three split floating n+ zones.

3. Results and Discussion

We observed electrical characteristics for proposed TFT. Moreover we achieved the low hole concentration in the channel region with three split floating n+ process. The low electric field at the edge of drain region results in drastic reduction of kink-effect. Moreover this structure improves the on-current compared to the conventional dual-gate TFTs.

3.1. The I-V output characteristics

Fig 3. shows the drain current - drain voltage output characteristics for the conventional single and dual gate TFT and the proposed dual gate TFT at V_G=7 V and V_D=12 V. The Drain voltage range was from 0.1 V to 20 V and gate voltage is fixed at 7 V. Both of the TFTs channel length was 10 um and gate width was 20 um. The drain current of the conventional single gate TFT increases in the saturation continuously. We called this effect which is kink effect and the usual approach to reduce this effect is to limit the impact ionization contribution to decrease the electric field at the drain junction by using dual gate structure. Fig. 3. shows the on-current of the conventional dual gate TFT is lower than that of the single gate TFT because of the low electric field at the drain junction and this is the drawback of the dual gate structure.

The proposed dual gate TFT shows the improvement of the on-current compared with the conventional dual gate TFT as shown Fig 3. The on-current of the proposed dual-gate structure is 0.9 mA while that of the conventional dual-gate structure is 0.5 mA at a 12 V drain voltage and a 7 V gate voltage. This result shows a 80 % enhancement in on-current due to the channel resistance reduction by two floating n+ zones. Fig. 4 shows the I-V output characteristics for the proposed dual-gate TFT at variable gate voltages.

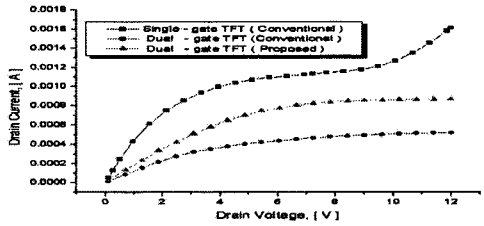


Fig. 3. The I-V characteristics for conventional single-gate, dual-gate and the proposed dual-gate TFT(V_D=12 V, V_G=7 V)

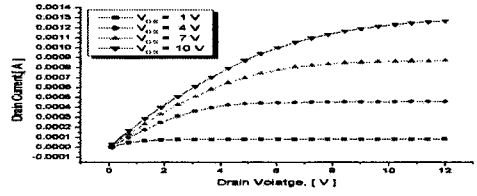


Fig. 4. Simulated I_D_V_D output characteristics of proposed dual-gate TFT (V_D=12 V, W/L=2).

3.2 The Output Conductance

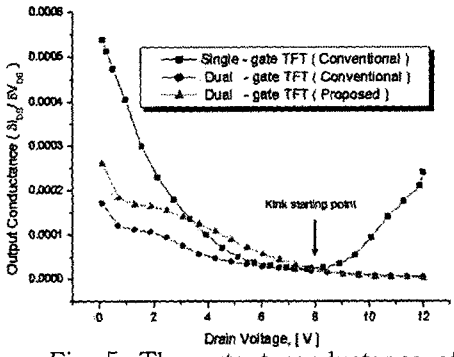


Fig. 5. The output conductance of proposed dual-gate TFT(V_D=12 V, V_G=7 V)

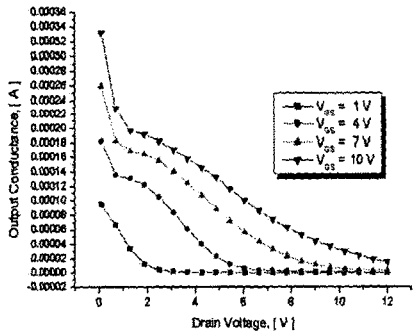
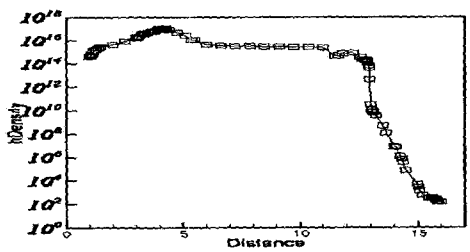


Fig. 6. The output conductance characteristics for different gate voltage of proposed dual-gate TFT(V_D=12 V)

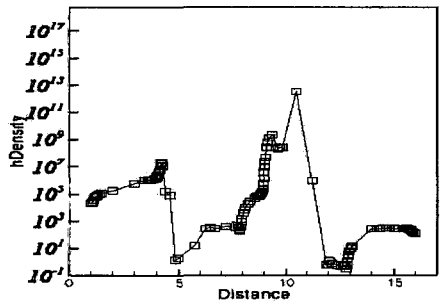
Fig. 5 shows the output conductance of the conventional single gate, the conventional dual gate TFT and the proposed dual gate TFT. The output conductance which increases continuously in the saturation region means that the drain current increases. The kink effect of the proposed dual gate TFT is drastically reduced compared with the conventional single gate TFT and we observed the enhancement of the on-current rather than conventional dual gate TFT as shown Fig. 3. Fig. 6 shows the output conductance characteristics for different gate voltage of the proposed dual gate TFT. The stable output conductance proves the prevention of the kink effect although the gate voltage increases.

3.3 The Hole Concentration Characteristics

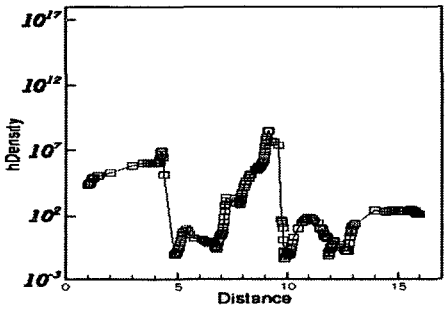
Fig 7. shows the hole concentration of the conventional single gate, the conventional dual gate TFT and the proposed dual gate TFT. The hole concentration is an important parameter in kink effect analysis. In the conventional single gate TFTs, the holes generated by impact ionization at the drain junction can flow toward the source contact in the back-channel region and cause a potential barrier lowering at the source junction(PBT action).[4] The hole concentration of the proposed dual gate TFT at the source contact starting point(5 um) is very low because of the recombination between the floating n+ zones and holes. This result displays the prevention of the hole injection to the source contact so that the preclusion of the injection of electron to the channel as shown Fig 7. We shows the potential barrier in section 3.5 in detail.



(a) The conventional single-gate TFT.



(b) The conventional dual-gate TFT.

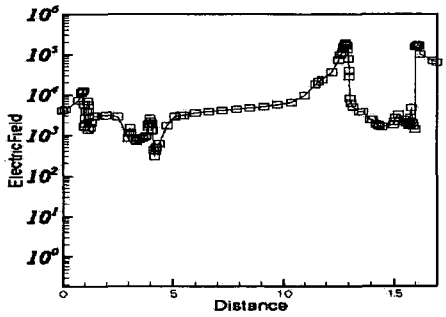


(c) The proposed dual-gate TFT

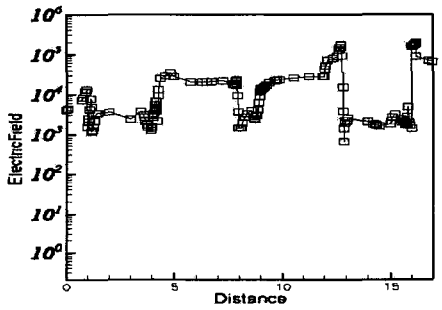
Fig. 7. Hole concentration in the channel region .(cm^{-3})(V_D=12 V, V_G=7 V)

3.4 The 2-Dimensional Electric Field Distribution

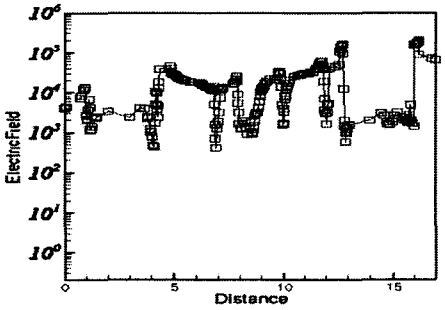
Fig 8. shows the electric field of the conventional single gate, the dual gate TFT and the proposed dual gate TFT. The electric field at a 13um point in the proposed dual gate TFT is very low compared with the conventional single gate TFT. In addition the proposed dual gate achieved the lower electric field than that of the conventional dual gate TFT so the reduction of kink effect was significant. The low electric field in the proposed dual gate TFT is continuous with the hole concentration and the reduction of the PBT action.



(a) The conventional single-gate TFT



(b) The conventional dual-gate TFT



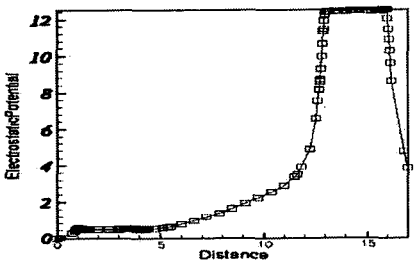
(c) The proposed dual-gate TFT

Fig. 8. The electric field in channel region. (V) (V_D=12 V, V_G=7 V)

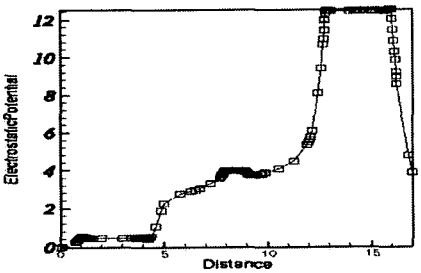
3.5 The 2-Dimensional Potential Barrier Distribution

As we explained in the pre-sections, the injection of electrons to the channel from the source contact cause the lowering the potential barrier and consequently cause an increase of the

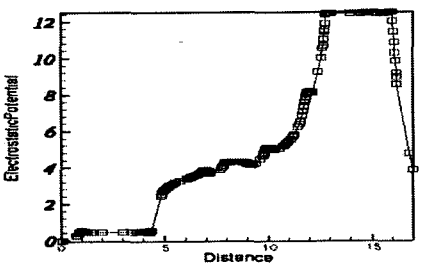
drain current in the saturation region. Fig 9. shows the potential barrier of the conventional single gate, the dual gate TFT and the proposed dual gate TFT. The potential barrier of the proposed dual gate TFT enhanced while that of the conventional TFTs. This result induces the stability of output conductance because of the suppression of kink effect. Fig. 10 shows the potential barrier of cross section of the TFTs and the length and height of the TFTs are indicated.



(a) The conventional single-gate TFT



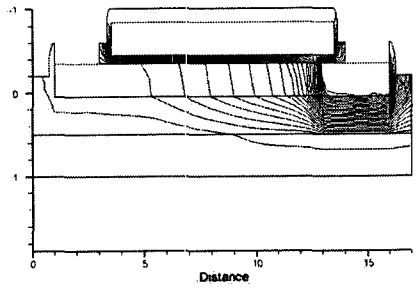
(b) The conventional dual-gate TFT



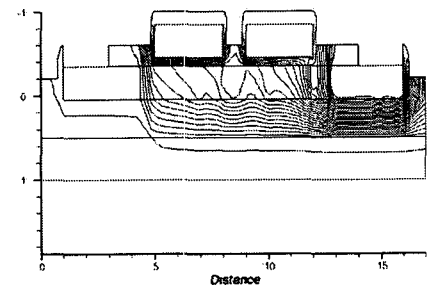
(c) The proposed dual-gate TFT

Fig. 9 The potential barrier distribution

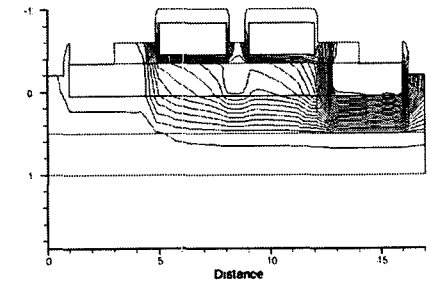
(V_D=1.2V, V_G=7V)



(a) The conventional single-gate TFT



(b) The conventional dual-gate TFT



(c) The proposed dual-gate TFT

Fig. 10. The potential barrier distribution (V_D=12V, V_G=7V)

4. Conclusion

The New Dual-gate TFT structure with three split floating n+ zones allowed us to reduce of kink-effect drastically. We confirmed the stable output conductance. We observed that the reduction of the

hole concentration results in reduction of kink-effect. Moreover the three split floating n+ zones caused the reduction of electric field at the drain/channel contact region to delay the premature breakdown. In addition, this structure showed that the improvement of on-current compared to conventional dual-gate TFT. On-current showed a 80 % enhancement compared with the conventional dual gate TFT. Finally, the simulated single crystal silicon dual gate TFT structure appear very effective in limiting kink-effect. In addition, if doping element changes to the As or An instead of Phosphorus, we expect a more smaller channel length size of the TFT.

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